

A Unified Finite-Element Solution From Zero Frequency to Microwave Frequencies for Full-Wave Modeling of Large-Scale Three-Dimensional On-Chip Interconnect Structures

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Abstract—It has been observed that a full-wave finite-element-based solution breaks down at low frequencies. This hinders its application to on-chip problems in which broadband modeling from direct current to microwave frequencies is required. Although a static formulation and a full-wave formulation can be stitched together to solve this problem, it is cumbersome to implement both static and full-wave solvers and make transitions between these two when necessary. In this work, a unified finite-element solution from zero frequency to microwave frequencies is developed for full-wave modeling of large-scale three-dimensional on-chip interconnect structures. In this solution, a single full-wave formulation is used. No switching to a static formulation is needed at low frequencies. This is achieved by first identifying the reason why a full-wave eigenvalue-based solution breaks down at low frequencies, and then developing an approach to eliminate the reason. The low frequency breakdown problem was found to be attributed to the discrepant frequency dependence of the real part and the imaginary part of the eigenvalues, which leads to an ill-conditioned eigenvalue system at low frequencies. The discrepant frequency dependence of the real part and the imaginary part is further attributed to the different scaling of the transverse and longitudinal fields with respect to frequency in a transmission-line type structure. By extracting transverse and longitudinal fields separately in the framework of a full-wave formulation, we avoid the numerical difficulty of solving an ill-conditioned eigen-system at low frequencies. The validity of the proposed approach is demonstrated by numerical and experimental results.

Index Terms—Electromagnetic analysis, finite element methods, interconnects, low frequency, on-chip.

I. INTRODUCTION

INTEGRATED circuit (IC) design has been guided by circuit theory for more than three decades. The continuous scaling of feature sizes and frequency necessitates electromagnetics (EM)-based analysis. EM-based analysis can be used to guide optical proximity correction to ensure the faithful reproduction of design onto the wafer at 45-nm technology node and beyond; to design high-speed on-chip interconnects; to characterize global electromagnetic coupling through the common substrate and power delivery network; to design radio frequency

(RF) and mixed-signal ICs; and to explore alternative technologies such as on-chip wireless communication. However, on-chip problems present many modeling challenges to electromagnetic analysis [1]. These challenges include the following.

- 1) *Large problem size.* On-chip global interconnect structures such as an on-chip power grid can involve millions of interconnect lines.
- 2) *Conductor loss.* In contrast to traditional full-wave applications in which currents only flow on the surface of the conductors, on-chip wires are transparent to fields and currents.
- 3) *Large number of nonuniform dielectric stacks and strong nonuniformity.* The interconnect systems of processing technologies of 0.13 μm and beyond involve 8+ metal layers. Between the metal layers are a number of interlayer dielectric media. In addition, the metal and dielectric stacks are heterogeneous.
- 4) *The presence of silicon substrate.* On-chip interconnects usually are not backed by ground planes as their packaging or board counterparts. Instead, they are exposed to silicon substrate. The substrate loss can be either low or high depending on the substrate resistivity.
- 5) *Large aspect ratio.* The length of on-chip interconnect lines can be orders of magnitude larger than the cross-sectional dimension.
- 6) *Broadband.* On-chip applications cover broadband frequencies from direct current (dc) to tens of gigahertz.
- 7) *Three-dimensional complexity.* On-chip structures are complicated 3-D in nature. It is difficult to take advantage of symmetry or periodicity to simplify the problems in electromagnetic modeling.

In recent years, in view of the importance and challenges of full-wave electromagnetic analysis in high-frequency IC design, researchers in both circuits and fields have initiated the development of innovative EM solutions for on-chip problems [2]–[15]. Both partial differential equation (PDE) based solutions and integral equation (IE) based solutions have been developed. In [5] and [13], a fast method was developed for full-wave modeling of high-speed interconnect structures. In this method, a number of seeds (a seed has a unique cross section) are first recognized from an interconnect structure. In each seed, the original wave propagation problem is represented as a generalized eigenvalue problem. The complexity of solving 3-D interconnects is then overcome by seeking the solution of a few 2-D seeds, which

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is then postprocessed to obtain the solution of the original 3-D problem through the development of an on-chip mode-matching technique. The procedure is rigorous without making any approximation. The method effectively solves many of the aforementioned on-chip modeling challenges. It only needs to solve a few 2-D structure seeds to obtain the solution of the original 3-D problem, and hence overcoming the challenges of large problem size and 3-D complexity; it discretizes into conductors to model internal fields accurately (it can afford to do so because only a 2-D cross section needs to be discretized), and hence effectively addressing the problems of conductor loss and the presence of silicon substrate; it formulates an eigenvalue problem that comprehends arbitrary dielectric and conductor configuration in the transverse cross section and arbitrary material, and hence effectively modeling strong nonuniformity; it solves the transverse cross section numerically and handles the longitudinal direction analytically, and hence overcoming the problem of large aspect ratio.

However, the aforementioned method [5], [13] has a shortcoming: it breaks down at tens of megahertz in typical on-chip applications. The low-frequency breakdown problem of a full-wave solver has been observed in both integral-equation-based methods [16]–[20] and finite-element-based methods [21]. In the integral-equation-based methods, the problem was shown to be attributed to the discrepant frequency dependence of the solenoidal and irrotational components of the current when frequency ω tends to zero, which leads to the loss of the solenoidal current contribution and a quadratic scaling of matrix condition number with decreasing frequency. The loop-tree and loop-star method was hence used to achieve a natural Helmholtz decomposition of the current to overcome the low-frequency breakdown problem. Another low-frequency technique was also developed by separating the charge and current basis functions in the partial element equivalent circuit (PEEC) method, and by incorporating loss and proper frequency scaling schemes. These techniques are effective for integral-equation-based methods. However, they cannot be directly applied to finite-element-based methods due to different nature of the numerical process. In [21], a static formulation and a full-wave formulation were stitched together to address the low-frequency breakdown problem in a finite-element-based solution. In this paper, a unified finite-element solution from zero frequency to microwave frequencies was developed for finite-element-based full-wave modeling of on-chip structures in the framework of [5], [13]. This solution obviates the need of switching formulations for different ranges of the electromagnetic spectrum. In this solution, it was found that a full-wave eigenvalue-based method breaks down at low frequencies because of the different scaling of the real part and the imaginary part of the eigenvalues with frequency. The real part has little frequency dependence, whereas the imaginary part scales with frequency ω as $O(\omega^{-1})$. This renders the eigenvalue system ill-conditioned at low frequencies. The different frequency scaling of the real and the imaginary parts was further attributed to the different frequency scaling of the transverse and longitudinal fields. The transverse field distribution in a transmission-line type structure has little frequency dependence, whereas the longitudinal one inside conductors scales with



Fig. 1. Illustration of an on-chip interconnect network (Source: Intel).

frequency rapidly due to the effect of skin-depth. The proposed solution hence extracts the transverse and longitudinal fields separately in the framework of a full-wave formulation. As a result, the need for solving an ill-conditioned eigen-system at low frequencies is obviated.

The remainder of this paper is organized as follows. In Section II, a finite-element-based eigenvalue approach for full-wave modeling of on-chip 3-D interconnects is briefly reviewed. In Section III, the low-frequency breakdown problem is analyzed. In Section IV, the proposed unified solution from dc to microwave frequencies is elaborated. In Section V, numerical and experimental results are given to demonstrate the validity of the proposed solution. Section VI relates to our conclusions.

II. BRIEF REVIEW OF THE FINITE-ELEMENT-BASED EIGENVALUE APPROACH FOR FULL-WAVE MODELING OF LARGE-SCALE THREE-DIMENSIONAL ON-CHIP INTERCONNECT STRUCTURES

Consider a typical on-chip interconnect network shown in Fig. 1. It involves 8+ metal layers. Between the metal layers are a number of interlayer dielectric media. The metal layers are generally denoted by M_i ($i = 1, 2, 3, \dots$). The adjacent metal layers are orthogonal to each other. The modeling challenges of this type of structure include conductor loss that leads to fields inside conductors, large number of conductors, large number of nonuniform dielectric stacks, large aspect ratio, 3-D complexity, and broadband from dc to high frequencies. In [5] and [13], an eigenvalue-based approach was proposed to model large-scale 3-D on-chip interconnect structures. In this approach, the interconnect structure is decomposed into a number of seeds. In each seed, the original wave propagation problem is represented as a generalized eigenvalue problem. The resulting eigenvalue representation can comprehend both conductor and dielectric losses. A new mode-matching technique applicable to on-chip interconnects is developed to solve large-scale 3-D problems by using 2-D-like CPU time and memory. In essence, the complexity of 3-D interconnects is overcome by seeking the full-wave eigenvalue solution of a few 2-D problems, which are

then post-processed to obtain the solution of the original 3-D problem.

Inside each structure seed, the electric field \mathbf{E} satisfies the second-order vector wave equation

$$\nabla \times (\mu_r^{-1} \nabla \times \mathbf{E}) - k_0^2 \epsilon_r \mathbf{E} + j\omega \mu_0 \sigma \mathbf{E} = 0 \text{ in } \Omega \quad (1)$$

subject to certain boundary conditions such as

$$\begin{aligned} \hat{n} \times \mathbf{E} &= 0 \text{ on } \Gamma_1 \\ \hat{n} \times (\nabla \times \mathbf{E}) &= 0 \text{ on } \Gamma_2. \end{aligned} \quad (2)$$

In (1), μ_r , ϵ_r , and σ denote the relative permeability, relative permittivity, and conductivity respectively, Ω is the computational domain which is the cross section of a structure seed including both dielectric and conducting regions, Γ_1 is the boundary where the Dirichlet boundary condition is applied, and Γ_2 is the boundary where the Neumann boundary condition is applied. The finite-element solution [22] of (1) and (2) results in a generalized eigenvalue problem, which can be written as

$$\begin{bmatrix} \mathbf{A}_{tt} & 0 \\ 0 & 0 \end{bmatrix} \begin{Bmatrix} e_t \\ e_z \end{Bmatrix} = \frac{\gamma^2}{k_0^2} \begin{bmatrix} \mathbf{B}_{tt} & \mathbf{B}_{tz} \\ \mathbf{B}_{zt} & \mathbf{B}_{zz} \end{bmatrix} \begin{Bmatrix} e_t \\ e_z \end{Bmatrix} \quad (3)$$

in which $e_t = -j\gamma E_t$, $e_z = -jE_z$, where E_t represents the transverse electric field and E_z represents the longitudinal one. Since both dielectric and conductive regions are discretized, \mathbf{A} and \mathbf{B} are complex-valued matrices. Their matrix elements are given by

$$\begin{aligned} \mathbf{A}_{tt,ij} &= \iint_{\Omega} \left[\frac{1}{\mu_r k_0^2} \{ \nabla_t \times \mathbf{N}_i \} \cdot \{ \nabla_t \times \mathbf{N}_j \} - \bar{\epsilon}_r \mathbf{N}_i \cdot \mathbf{N}_j \right] d\Omega \\ \mathbf{B}_{tt,ij} &= \iint_{\Omega} \frac{1}{\mu_r} \mathbf{N}_i \cdot \mathbf{N}_j d\Omega \\ \mathbf{B}_{tz,ij} &= \iint_{\Omega} \frac{1}{\mu_r} \mathbf{N}_i \cdot \nabla_t \xi_j d\Omega \\ \mathbf{B}_{zt,ij} &= \iint_{\Omega} \frac{1}{\mu_r} \nabla_t \xi_i \cdot \mathbf{N}_j d\Omega \\ \mathbf{B}_{zz,ij} &= \iint_{\Omega} \left[\frac{1}{\mu_r} \{ \nabla_t \xi_i \} \cdot \{ \nabla_t \xi_j \} - k_0^2 \bar{\epsilon}_r \xi_i \xi_j \right] d\Omega \end{aligned} \quad (4)$$

in which $\bar{\epsilon}_r$ denotes a complex permittivity that incorporates conductivity σ , \mathbf{N}_i is the edge basis function, and ξ_i is the node basis function. The eigenvalues of (3) correspond to the propagation constants, whereas the eigenvectors characterize the transverse and longitudinal fields. The eigenvalues and eigenvectors are both complex.

Once the field solutions are obtained from (3), circuit parameters such as resistance-inductance-conductance-capacitance (RLGC) and S -parameters can be extracted by using the approach developed in [5] and [13].

III. LOW-FREQUENCY BREAKDOWN PROBLEM

Our numerical experiments show that in general, the solution of (3) breaks down at tens of megahertz in typical on-chip applications. In other words, the solution of (3) fails to produce complete sets of eigenvalues of physical interest. To elaborate, given

a structure of N conductors, at low frequencies, N propagation modes should be found, i.e., N eigenvalues that are physically meaningful should be found from (3). The physically meaningfulness can be judged from the range of the real part, and the sign of the imaginary part as can be seen from (6). If the eigenvalue solution of (3) fails to produce N physically meaningful eigenvalues, then the full-wave solution of (3) breaks down. Given any problem, we perform frequency sweeping from high frequencies to low frequencies. The first frequency at which the solution of (3) fails is the breakdown frequency.

The solution of (3) breaks down at low frequencies because when frequency decreases, the real part of the eigenvalue γ^2/k_0^2 remains as an $O(1)$ quantity, while the imaginary part scales with frequency as $O(1/\omega)$. To explain, consider a single wire embedded in an inhomogeneous stack, assuming the dielectric loss is negligible

$$\frac{\gamma^2}{k_0^2} = \frac{(R + j\omega L)j\omega C}{\omega^2 L_0 C_0} \quad (5)$$

in which R , L , and C are resistance, inductance, and capacitance per unit length, respectively, and L_0 and C_0 are L and C obtained by replacing all the dielectric material with air.

From (5), we have

$$\frac{\gamma^2}{k_0^2} = \frac{-\omega^2 LC + j\omega RC}{\omega^2 L_0 C_0} \quad (6)$$

which yields an $O(1)$ real part that has little frequency dependence and an imaginary part that scales with frequency as $O(\omega^{-1})$.

It is known that for any $m \geq 5$, there is a polynomial $p(z)$ of degree m with rational coefficients that has a real root $p(r) = 0$ with the property that r cannot be written using an expression involving rational numbers, addition, subtraction, multiplication, division, and k th roots [23]. This theorem implies that there could be no computer program that would produce the exact roots of an arbitrary polynomial in a finite number of steps. It follows that the same conclusion applies to the more general problem of computing eigenvalues of matrices [23]. Hence, any eigenvalue solver must be iterative. The $O(\omega^{-1})$ scaling of the eigenvalue's imaginary part in (3) significantly increases the spectral radius of the system when frequency decreases, which makes the iterative solution of (3) very difficult to converge. Hence, although (3) is theoretically valid from dc to high frequencies, it is a numerically difficult problem at low frequencies.

IV. PROPOSED UNIFIED FULL-WAVE SOLUTION FROM ZERO FREQUENCY TO MICROWAVE FREQUENCIES

In practice, it is troublesome to develop two solvers, one for static simulation and the other for full-wave simulation, to model the entire frequency band from dc to microwave frequencies. The purpose here is hence to develop a single full-wave solution to obviate the need of switching formulations. We will start from full-wave formulation (3) and develop a numerical solution to make (3) feasible for low frequencies. Our solution includes three steps: obtain E_t , obtain E_z/γ , and obtain γ , each of which is illustrated in the following subsections.

A. Obtain E_t at Low Frequencies

At low frequencies where static approximation holds true, the transverse electric field is frequency independent. Hence E_t at low frequencies can be obtained at the frequency where full-wave simulation breaks down. In other words, whenever the full-wave simulation breaks down, we record E_t at the frequency a little bit higher than the breakdown frequency and use that E_t for low frequencies.

B. Obtain E_z/γ at Low Frequencies

The second row in (3) suggests that

$$\mathbf{B}_{zt}e_t + \mathbf{B}_{zz}e_z = 0. \quad (7)$$

Hence

$$E_z/\gamma = -\mathbf{B}_{zz}^{-1}\mathbf{B}_{zt}E_t. \quad (8)$$

Although (8) is a field-based equation, it has a concrete circuit meaning. The circuit interpretation of (8) is

$$R + j\omega L = \frac{V_1 - V_2}{I} \quad (9)$$

which reveals the impedance (a resistance in series with an inductance) experienced by a current I given a potential difference $V_1 - V_2$ at the two ends of a wire of unit length. This is because E_t in (8) relates to voltage, γE_t relates to the voltage difference across a unit length, and E_z relates to current. From E_t , one can obtain the voltage at one end of the wire (a terminal) by performing a line integral from the terminal to the ground; from γE_t , one can obtain the voltage difference between the two ends of the wire because the z -dependence of all field components is $e^{-\gamma z}$ in a structure seed; and from E_z , one can obtain the current flowing into the wire by performing an area integral of the conduction current over the wire cross section. Therefore, using (8), (9) can be realized by

$$R + j\omega L = \frac{\gamma V_1}{I} = \frac{V_1}{I/\gamma} = \frac{\int E_t dl}{\iint (j\omega\epsilon + \sigma) (-\mathbf{B}_{zz}^{-1}\mathbf{B}_{zt}E_t) dS}. \quad (10)$$

For a general case of M conductors

$$(R + j\omega L)_{ij} \int \int (j\omega\epsilon + \sigma) (-\mathbf{B}_{zz}^{-1}\mathbf{B}_{zt}E_{m,t}) dS_j \\ = \int E_{m,t} dl_i \quad i, j = 1, 2, 3, \dots, M \quad (11)$$

in which m denotes the index of the m th mode, l_i denotes the integration path from the i th conductor to the ground, and S_j denotes the cross-sectional area of the j th conductor.

Therefore, by evaluating (8), we obtain not only field quantity E_z/γ , but also circuit parameters R and L directly.

C. Obtain γ at Low Frequencies

There are two approaches to obtain γ . The first approach is a pure field-based approach. In this approach, (3) is rewritten as

$$\begin{bmatrix} \mathbf{A}_{tt} & 0 \\ 0 & 0 \end{bmatrix} \begin{Bmatrix} E_t \\ E_z/\gamma \end{Bmatrix} = \frac{\gamma^2}{k_0^2} \begin{bmatrix} \mathbf{B}_{tt} & \mathbf{B}_{tz} \\ \mathbf{B}_{zt} & \mathbf{B}_{zz} \end{bmatrix} \begin{Bmatrix} E_t \\ E_z/\gamma \end{Bmatrix} \quad (12)$$

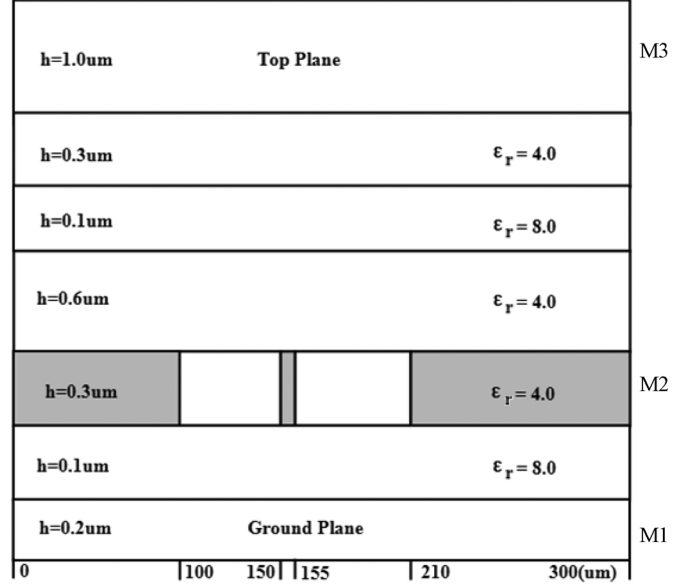


Fig. 2. Illustration of a three-metal-layer on-chip interconnect.

Since both E_t and E_z/γ are known from Steps A and B, γ can be obtained from

$$\frac{\gamma^2}{k_0^2} = \frac{\begin{Bmatrix} E_t \\ E_z/\gamma \end{Bmatrix}^T \begin{bmatrix} \mathbf{A}_{tt} & 0 \\ 0 & 0 \end{bmatrix} \begin{Bmatrix} E_t \\ E_z/\gamma \end{Bmatrix}}{\begin{Bmatrix} E_t \\ E_z/\gamma \end{Bmatrix}^T \begin{bmatrix} \mathbf{B}_{tt} & \mathbf{B}_{tz} \\ \mathbf{B}_{zt} & \mathbf{B}_{zz} \end{bmatrix} \begin{Bmatrix} E_t \\ E_z/\gamma \end{Bmatrix}} \quad (13)$$

in which superscript T denotes a transpose. For each mode, (13) is evaluated once to obtain γ for that specific mode.

The second approach is a circuit-based one. Take a single wire of unit length as an example, assuming that the dielectric loss is negligible

$$I_1 - I_2 = j\omega CV \quad (14)$$

in which C denotes the capacitance per unit length, and I_1 and I_2 are the current at the near- and far-end, respectively. Because each structure seed has a constant cross-section, wave propagating along longitudinal direction is analytical. Therefore, the z -dependence of all field components is $e^{-\gamma z}$. Hence, (14) can be rewritten as

$$\gamma I = j\omega CV. \quad (15)$$

Although I is unknown, I/γ can be obtained by performing an area integral of E_z/γ (known from Step B) over the wire cross section. V can be obtained from E_t (known from Step A) by performing a line integral from the wire to the ground. What remains unknown is C . At static frequencies, transverse electric field does not depend on frequencies, and hence C is frequency independent. Therefore, we can use C generated at the lowest frequency at which full-wave simulation is still valid. In other words, whenever the full-wave simulation breaks down,

TABLE I
COMPARISONS OF *RLC* PARAMETERS OF EXAMPLE 1 (REFERENCE FREQUENCY IS 24.1 MHz)

		Frequency (Hz)									
		1.00e6	2.78e5	7.74e4	2.15e4	5.99e3	1.67e3	4.64e2	1.29e2	3.59e1	1.00e1
R	Fw	1.34e2	1.33e2	1.33e2	1.33e2	1.33e2	1.33e2	1.33e2	1.33e2	1.33e2	1.33e2
	St	1.34e2	1.34e2	1.33e2	1.33e2	1.33e2	1.33e2	1.33e2	1.33e2	1.33e2	1.33e2
L	Fw	1.35e2	2.98e2	3.52e2	3.57e2	3.58e2	3.58e2	3.58e2	3.58e2	3.57e2	3.57e2
	St	1.35e2	2.98e2	3.52e2	3.57e2	3.58e2	3.58e2	3.58e2	3.58e2	3.58e2	3.58e2
C	Fw	4.06e1	4.06e1	4.06e1	4.06e1	4.06e1	4.06e1	4.06e1	4.06e1	4.06e1	4.06e1
	St	4.05e1	4.05e1	4.05e1	4.05e1	4.05e1	4.05e1	4.05e1	4.05e1	4.05e1	4.05e1

(Fw: Full-wave formulation of this work; St: Static formulation; R: ohms/cm; L: nH/cm; C: pF/cm)

TABLE II
COMPARISONS OF *RLC* PARAMETERS OF EXAMPLE 1 (REFERENCE FREQUENCY IS 60 MHz)

		Frequency (Hz)									
		1.00e6	2.78e5	7.74e4	2.15e4	5.99e3	1.67e3	4.64e2	1.29e2	3.59e1	1.00e1
R	Fw	1.34e2	1.34e2	1.33e2	1.33e2	1.33e2	1.33e2	1.33e2	1.33e2	1.33e2	1.33e2
	St	1.34e2	1.34e2	1.33e2	1.33e2	1.33e2	1.33e2	1.33e2	1.33e2	1.33e2	1.33e2
L	Fw	1.35e2	2.98e2	3.52e2	3.57e2	3.58e2	3.58e2	3.58e2	3.58e2	3.57e2	3.54e2
	St	1.35e2	2.98e2	3.52e2	3.57e2	3.58e2	3.58e2	3.58e2	3.58e2	3.58e2	3.58e2
C	Fw	4.05e1	4.05e1	4.05e1	4.05e1	4.05e1	4.05e1	4.05e1	4.05e1	4.05e1	4.05e1
	St	4.05e1	4.05e1	4.05e1	4.05e1	4.05e1	4.05e1	4.05e1	4.05e1	4.05e1	4.05e1

(Fw: Full-wave formulation of this work; St: Static formulation; R: ohms/cm; L: nH/cm; C: pF/cm)

TABLE III
COMPARISONS OF *RLC* PARAMETERS OF EXAMPLE 1 (REFERENCE FREQUENCY IS 100 MHz)

		Frequency (Hz)									
		1.00e6	2.78e5	7.74e4	2.15e4	5.99e3	1.67e3	4.64e2	1.29e2	3.59e1	1.00e1
R	Fw	1.34e2	1.34e2	1.33e2	1.33e2	1.33e2	1.33e2	1.33e2	1.33e2	1.33e2	1.33e2
	St	1.34e2	1.34e2	1.33e2	1.33e2	1.33e2	1.33e2	1.33e2	1.33e2	1.33e2	1.33e2
L	Fw	1.35e2	2.98e2	3.52e2	3.57e2	3.58e2	3.58e2	3.57e2	3.57e2	3.54e2	3.46e2
	St	1.35e2	2.98e2	3.52e2	3.57e2	3.58e2	3.58e2	3.58e2	3.58e2	3.58e2	3.58e2
C	Fw	4.05e1	4.05e1	4.05e1	4.05e1	4.05e1	4.05e1	4.05e1	4.05e1	4.05e1	4.05e1
	St	4.05e1	4.05e1	4.05e1	4.05e1	4.05e1	4.05e1	4.05e1	4.05e1	4.05e1	4.05e1

(Fw: Full-wave formulation of this work; St: Static formulation; R: ohms/cm; L: nH/cm; C: pF/cm)

we record *C* at the frequency a little bit higher than the breakdown frequency and use that *C* for low frequencies.

The field realization of (15) is

$$\gamma^2 = j\omega C \frac{\int E_t dl}{\iint (j\omega\epsilon + \sigma) (-\mathbf{B}_{zz}^{-1} \mathbf{B}_{zt} E_t) dS}. \quad (16)$$

For a general case of *M* conductors

$$\begin{aligned} & \gamma_m^2 \left\{ \iint (j\omega\epsilon + \sigma) (-\mathbf{B}_{zz}^{-1} \mathbf{B}_{zt} E_{m,t}) dS_j \right\}_{j=1:M} \\ & = j\omega [C_{ij}]_{M \times M} \left\{ \int E_{m,t} dl_j \right\}_{j=1:M} \quad i, j = 1, 2, \dots, M \end{aligned} \quad (17)$$

in which $\{\cdot\}$ denotes a vector, and $[\cdot]$ denotes a matrix. The γ_m^2 can then be obtained as

$$\gamma_m^2 = \frac{j\omega \left\{ \int E_{m,t} dl_j \right\}^T [C_{ij}]_{M \times M} \left\{ \int E_{m,t} dl_j \right\}}{\left\{ \int E_{m,t} dl_j \right\}^T \left\{ \iint (j\omega\epsilon + \sigma) (-\mathbf{B}_{zz}^{-1} \mathbf{B}_{zt} E_{m,t}) dS_j \right\}}. \quad (18)$$

The aforementioned two approaches were compared and it was shown that the second approach is more accurate than the first one. This is reasonable because as stated before, all eigenvalue solvers must be iterative. The eigenvectors are hence approximate eigenvectors. In (13), γ is obtained by taking all the components (field quantities) in the eigenvector into consideration; while in (18), γ is obtained by using the dominant components only.

After obtaining E_t , E_z/γ , and γ from the aforementioned three steps, the eigenvalue system in (3) is solved at low frequencies. The rest procedure such as mode-matching and *S*-parameter extraction follows the original procedure developed in [5], [13]. By solving E_t and E_z separately in the framework of a full-wave formulation, we overcome the numerical difficulty of solving an ill-conditioned eigen-system at low frequencies. This agrees with the decoupled nature of E_t and E_z at low frequencies in a transmission-line type structure as can be seen from $\mathbf{E} = -\nabla\phi - j\omega\hat{\mathbf{z}}\mathbf{A}_z$, in which the longitudinal component E_z is due to magnetic field induced by longitudinal current.

TABLE IV
COMPARISONS OF RL PARAMETERS OF EXAMPLE 2

	R11	R12	R13	R21	R22	R23	R31	R32	R33
Fw	2.22e2	3.34e-4	3.30e-4	3.34e-4	1.33e2	3.32e-4	3.30e-4	3.32e-4	3.33e2
St	2.22e2	3.34e-4	3.30e-4	3.34e-4	1.33e2	3.32e-4	3.30e-4	3.32e-4	3.33e2
	L11	L12	L13	L21	L22	L23	L31	L32	L33
Fw	3.60e2	3.40e2	3.20e2	3.40e2	3.57e2	3.40e2	3.20e2	3.40e2	3.59e2
St	3.60e2	3.40e2	3.20e2	3.40e2	3.57e2	3.40e2	3.20e2	3.40e2	3.59e2

(Fw: Full-wave formulation of this work; St: Static-based solution; R: ohms/cm; L: nH/cm)

TABLE V
COMPARISONS OF RLC PARAMETERS OF EXAMPLE 3

		Frequency (Hz)									
		1.00e6	2.78e5	7.74e4	2.15e4	5.99e3	1.67e3	4.64e2	1.29e2	3.59e1	1.00e1
R	Fw	7.08e1	7.04e1	7.02e1	7.02e1	7.02e1	7.02e1	7.02e1	7.02e1	7.02e1	7.02e1
	St	7.08e1	7.04e1	7.02e1	7.02e1	7.02e1	7.02e1	7.02e1	7.02e1	7.02e1	7.02e1
L	Fw	9.26e1	2.25e2	2.80e2	2.86e2	2.86e2	2.86e2	2.86e2	2.86e2	2.86e2	2.85e2
	St	9.26e1	2.25e2	2.80e2	2.86e2	2.86e2	2.86e2	2.86e2	2.86e2	2.86e2	2.86e2
C	Fw	6.58e1	6.58e1	6.58e1	6.58e1	6.58e1	6.58e1	6.58e1	6.58e1	6.58e1	6.58e1
	St	6.56e1	6.56e1	6.56e1	6.56e1	6.56e1	6.56e1	6.56e1	6.56e1	6.56e1	6.56e1

(Fw: Full-wave formulation of this work; St: Static-based solution; R: ohms/cm; L: nH/cm; C: pF/cm)

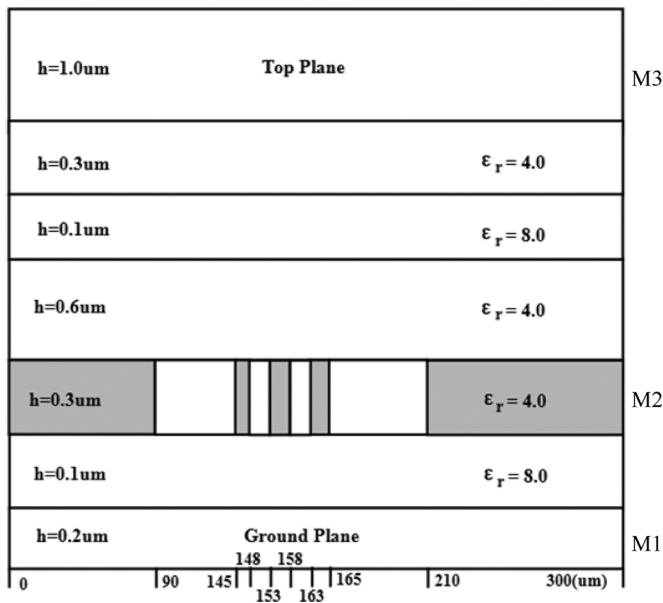


Fig. 3. Illustration of a three-metal-layer on-chip interconnect with three active wires in M2.

V. NUMERICAL RESULTS AND EXPERIMENTAL VALIDATION

To test the validity of the proposed solution, a number of on-chip interconnect structures were simulated, of which two were fabricated on a test chip [24] and two were artificially created test structures.

The first example is an on-chip interconnect structure shown in Fig. 2. It involves one active conductor at the center of M2 layer (shaded layer). Its cross section does not change along the longitudinal direction (out-of-the-paper direction), and hence only one structure seed is involved. Using the proposed broadband solution, we are able to simulate the eigenvalue system (3) from high frequencies down to dc. The

full-wave simulation broke down at ~ 24.1 MHz, at which the low frequency solution was enabled. In Table I, the RLC parameters simulated by the proposed solution were compared with those generated from a static solver using the formulation in [25]. Excellent agreement can be observed. It should be noted that the low frequency solution proposed in this work in the framework of a full-wave formulation is completely different from that given by a static formulation in [25]. But the two lead to the same low frequency results. This demonstrates the validity of the proposed solution.

In Tables II and III, we give the results generated by using the other two breakdown frequencies, 60 and 100 MHz. As can be seen clearly, the accuracy of the proposed approach does not depend on the exactness of the breakdown frequency. This agrees with our theoretical expectation. At low frequencies, there is a range of frequencies, not just one frequency, at which E_t and C have little frequency dependence. Choosing any of these frequencies will produce the same level of accuracy. Since there is no need to enable the low frequency solution when the full-wave solution is still valid, it is natural to choose the frequency at which the full-wave solver breaks down as the reference frequency to obtain E_t and C for the use of Step A and Step C as given in Section IV.

In the second example, three active conductors are placed in M2 layer as shown in Fig. 3, where the detailed geometry and material information is given. In Table IV, the R and L parameters obtained from the proposed solution at 104 Hz are compared with those generated by the static solver. Both self and mutual terms are compared. Excellent agreement can be observed.

The third example is a three-metal-layer on-chip interconnect structure fabricated using silicon processing technology on a test chip. The structure is of $300 \mu\text{m}$ width. It involves a $10\text{-}\mu\text{m}$ -wide strip in M2 layer, one ground plane in M1 layer, and one ground plane in M3 layer. The distance of this strip to the M2 returns at the left and right hand sides is $50 \mu\text{m}$. The strip

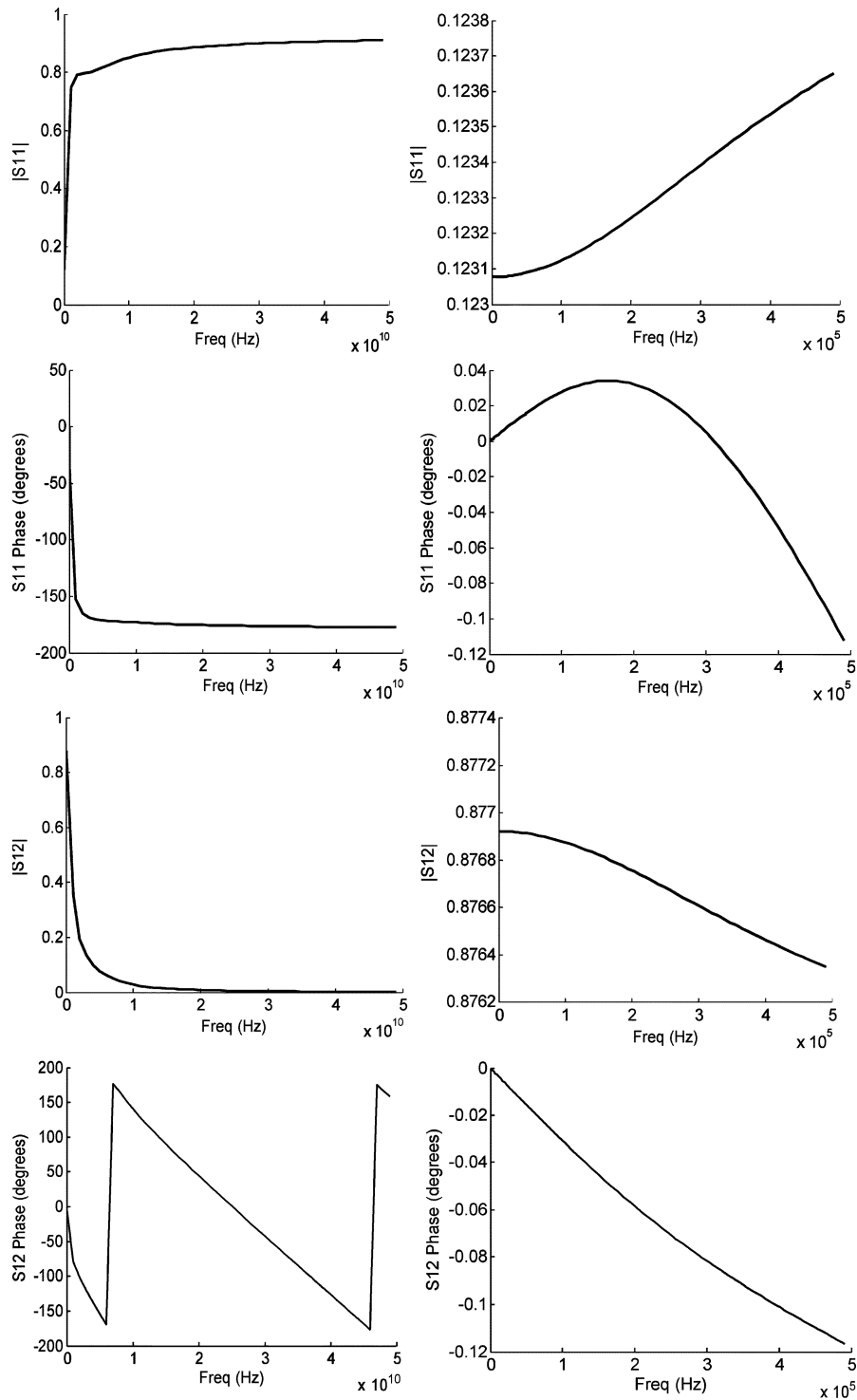


Fig. 4. *S*-parameters of a test-chip interconnect simulated by the proposed solution. (Left column: *S*-parameters in the entire band. Right column: *S*-parameters at low frequencies.)

is 0.285 μm thick and 2000 μm long. The full-wave simulation broke down at ~ 22.1 MHz, at which the low frequency solution was enabled. Table V lists the RLC parameters simulated by the proposed solution in comparison with those generated by a static solution using the formulation in [25]. Again, excellent agreement can be observed. The *S*-parameters of this structure were also simulated, which are shown in Fig. 4. The figures in the left column depict the *S*-parameters in the entire frequency

band, while those in the right column show the detail at low frequencies.

The last example is a 3-D interconnect of length 2000 μm , as shown in Fig. 5. It involves 2000 discontinuities along the longitudinal direction. The M1 and M3 metal layers are populated by orthogonal returns that are perpendicular to M2 wires. These returns are 1 μm wide each and 1 μm wide apart. The crosstalk is observed between two wires embedded in

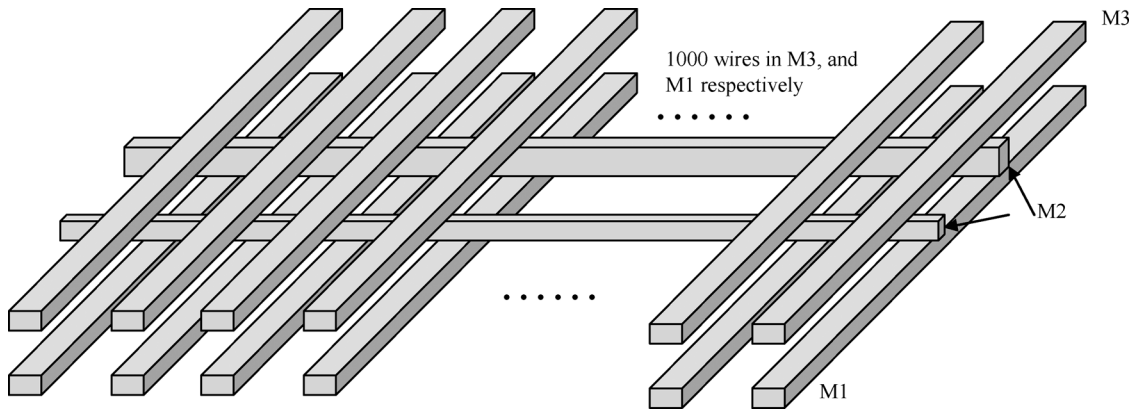


Fig. 5. Geometry of an on-chip 3-D interconnect with orthogonal returns.

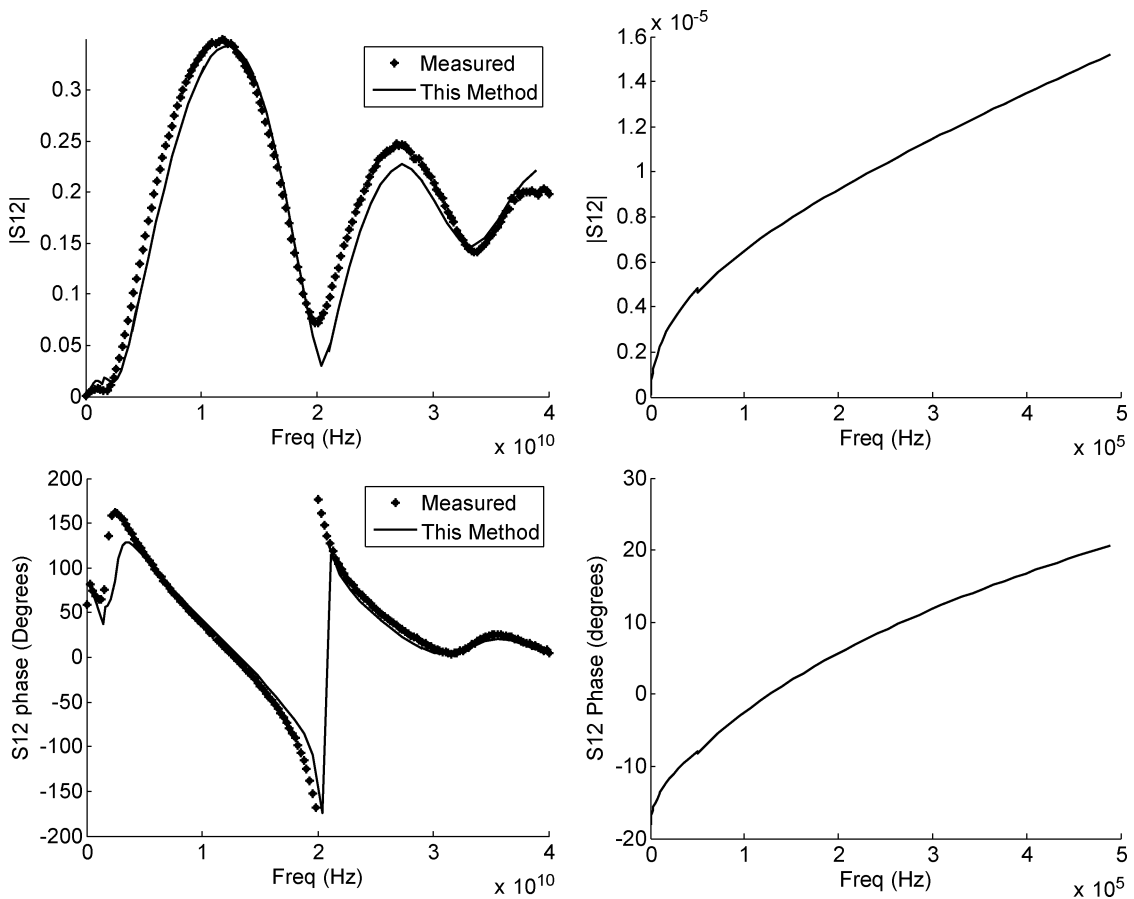


Fig. 6. Crosstalk of a test-chip interconnect simulated by the proposed solution. (Left column: S -parameters in the entire band. Right column: S -parameters at low frequencies.)

the M2 layer. One is of $2.1 \mu\text{m}$ width; the other is of $1.1 \mu\text{m}$ width. The spacing between these two wires is $1.95 \mu\text{m}$. The full-wave simulation broke down at ~ 40 MHz, at which the low frequency solution was enabled. Fig. 6 depicts the simulated crosstalk over the entire frequency band in comparison with the measured data in the left column and the low-frequency detail in the right column. Since the measured data is only available from 45 MHz to 40 GHz, the measured data is not shown in the right column.

VI. CONCLUSION

In this paper, a unified finite-element-based full-wave solution was developed for full-wave modeling of 3-D on-chip interconnects from dc to microwave frequencies. The solution was built upon a single full-wave formulation for both high and low frequencies. It avoids the need of combining static formulations with full-wave formulations and switching between these two when necessary. The three-step numerical procedure can

be easily incorporated into a full-wave simulation flow to extend the full-wave solution to low frequencies. Numerical and experimental results have demonstrated its validity.

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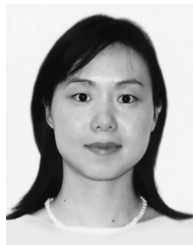
REFERENCES

- [1] D. Jiao, C. Dai, S.-W. Lee, T. R. Arabi, and G. Taylor, "Computational electromagnetics for high-frequency IC design," in *Proc. IEEE Int. Symp. Antennas Propagat.*, Jun. 2004, vol. 3, pp. 3317–3320.
- [2] A. E. Ruehli, "Equivalent circuit models for three-dimensional multi-conductor systems," *IEEE Trans. Microwave Theory Techn.*, vol. 22, no. 3, pp. 216–221, Mar. 1974.
- [3] A. Rong, A. C. Cangellaris, and L. Dong, "Comprehensive broadband electromagnetic modeling of on-chip interconnects with a surface discretization-based generalized PEEC model," in *Proc. IEEE Elec. Perf. Electron. Packag. Conf.*, 2003, pp. 367–370.
- [4] Z. Zhu, B. Song, and J. K. White, "Algorithms in fastimp: A fast and wide-band impedance extraction program for complicated 3-D geometries," *IEEE Trans. Computer-Aided Design*, vol. 24, no. 7, pp. 981–998, Jul. 2005.
- [5] D. Jiao, M. Mazumder, S. Chakravarty, C. Dai, M. Kobrinsky, M. Harnes, and S. List, "A novel technique for full-wave modeling of large-scale three-dimensional high-speed on/off-chip interconnect structures," in *Proc. Int. Conf. Simulation Semicond. Processes Devices*, Boston, MA, 2003, pp. 39–42.
- [6] S. Kapur and D. E. Long, "Large-scale full-wave simulation," in *Proc. DAC*, 2004.
- [7] D. Gope, A. E. Ruehli, C. Yang, and V. Jandhyala, "(S)PEEC: Time- and frequency-domain surface formulation for modeling conductors and dielectrics in combined circuit electromagnetic simulations," *Proc. 41st ACM IEEE Design Automation Conf. (DAC)*, vol. 54, no. 6, pp. 806–809, Jun. 2006.
- [8] P. J. Restle, A. E. Ruehli, S. G. Walker, and G. Papadopoulos, "Full-wave PEEC time-domain method for the modeling of on-chip interconnects," *IEEE Trans. Comput.-Aided Design Integr. Circuits Syst.*, vol. 20, no. 7, pp. 877–886, Jul. 2001.
- [9] F. Ling, V. I. Okhmatovski, W. Harris, S. McCracken, and A. Dengi, "Large-scale broad-band parasitic extraction for fast layout verification of 3-D RF and mixed-signal on-chip structures," *IEEE Trans. Microw. Theory Techn.*, vol. 53, no. 1, pp. 264–273, Jan. 2005.
- [10] M. Song and G. Pan, "Full-wave analysis of coupled lossy transmission lines using multiwavelet-based method of moments," *IEEE Trans. Microwave Theory Techn.*, vol. 53, no. 7, pp. 2362–2370, Jul. 2005.
- [11] A. E. Ruehli, G. Antonini, J. Esch, J. Ekman, A. Mayo, and A. Orlandi, "Nonorthogonal PEEC formulation for time- and frequency-domain EM and circuit modeling," *IEEE Trans. Electromagn. Compat.*, vol. 45, no. 2, pp. 167–176, May 2003.
- [12] D. Jiao, S. Chakravarty, and C. Dai, "A layered finite-element method for electromagnetic analysis of large-scale high-frequency integrated circuits," *IEEE Trans. Antennas Propag.*, vol. 55, no. 2, pp. 422–432, Feb. 2007.
- [13] D. Jiao, J. Zhu, and S. Chakravarty, "A fast frequency-domain eigenvalue-based approach to full-wave modeling of large-scale three-dimensional on-chip interconnect structures," *IEEE Trans. Adv. Packag.*, to be published.
- [14] Z. Cendes and A. Yen, "Mixed electromagnetic and electrical circuit simulation for RFIC characterization," in *Proc. IEEE Antennas Propagation Soc. Int. Symp.*, Monterey, CA, 2004, vol. 3, pp. 3289–3292.
- [15] Z. G. Qian, J. Xiong, L. Sun, I. T. Chiang, W. C. Chew, L. J. Jiang, and Y. H. Chu, "Crosstalk analysis by fast computational algorithms," in *Proc. IEEE 14th Topical Meeting Electr. Performance Electron. Packag.*, Oct. 2005, pp. 367–370.
- [16] J. S. Zhao and W. C. Chew, "Integral equation solution of Maxwell's equations from zero frequency to microwave frequencies," *IEEE Trans. Antennas Propag.*, vol. 48, no. 10, pp. 1635–1645, Oct. 2000.
- [17] A. Rong and A. C. Cangellaris, "Electromagnetic modeling of interconnects for mixed-signal integrated circuits from dc to multi-ghz frequencies," in *IEEE MTT-S Dig.*, 2002, vol. 3, pp. 1893–1896.
- [18] D. Gope, A. Ruehli, and V. Jandhyala, "Solving low frequency EM-CKT problems using the PEEC method," in *Proc. IEEE Electr. Perf. Electron. Packag. Conf.*, Austin, TX, Oct. 2005, pp. 351–354.
- [19] A. E. Yilmaz, J.-M. Jin, and E. Michielssen, "A low-frequency extension of the time-domain adaptive integral method," in *Electr. Performance Electron. Packag.*, Austin, TX, Oct. 24–26, 2005, pp. 359–362.
- [20] Y. Chu and W. C. Chew, "A surface integral equation method for solving complicated electrically small structures," in *Proc. IEEE Topical Meeting Electr. Performance Electron. Packag.*, 2003, pp. 341–344.
- [21] S. Lee, K. Mao, and J. Jin, "A complete finite element analysis of multilayer anisotropic transmission lines from dc to terahertz frequencies," *IEEE Trans. Adv. Packag.*, to be published.
- [22] J. M. Jin, *The Finite Element Method in Electromagnetics*, 2nd ed. New York: Wiley, 2002.
- [23] L. N. Trefethen and D. Bau, III, *Numerical Linear Algebra*. Philadelphia, PA: SIAM, 1997.
- [24] M. J. Kobrinsky, S. Chakravarty, D. Jiao, M. C. Harnes, S. List, and M. Mazumder, "Experimental validation of crosstalk simulations for on-chip interconnects using s-parameters," *IEEE Trans. Adv. Packag.*, vol. 28, no. 1, pp. 57–62, Feb. 2005.
- [25] F. Bertazzi, G. Ghione, and M. Goano, "Efficient quasi-tem frequency-dependent analysis of lossy multiconductor lines through a fast reduced-order FEM model," *IEEE Trans. Microwave Theory Techn.*, vol. 51, no. 9, pp. 2029–2035, Sep. 2003.



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