A Fast Frequency-Domain Eigenvalue-Based Approach to Full-Wave Modeling of Large-Scale Three-Dimensional On-Chip Interconnect Structures

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***Abstract*—As on-chip circuits have scaled into the deep submicron regime, electromagnetics-based analysis has increasingly become essential for high-performance integrated circuit (IC) design. Not only fast, but also high-capacity electromagnetic solutions are demanded to overcome the large problem size facing on-chip design community. In this paper, we present a novel, high-capacity, and fast approach to the full-wave modeling of 3-D on-chip interconnect structures. In this approach, the interconnect structure is decomposed into a number of seeds. In each seed, the original wave propagation problem is represented as a generalized eigenvalue problem. The resulting eigenvalue representation can comprehend both conductor and dielectric losses, arbitrary dielectric and conductor configuration in the transverse cross section, and arbitrary material. A new mode-matching technique applicable to on-chip interconnects is developed to solve large-scale 3-D problems by using 2-D-like CPU time and memory. A junction matrix acceleration technique is proposed to speed up the mode matching process. A fast frequency sweep technique is employed to obtain the response over the entire frequency band by solving at one or a few frequency points only. An extraction technique is developed to obtain *S*-parameters from the solution of the eigenvalue system. The entire procedure is numerically rigorous without making any theoretical approximation. Experimental and numerical results demonstrate its accuracy and efficiency.**

***Index Terms*—Eigenvalue, electromagnetics, fast frequency sweep, full wave, interconnects, large scale, mode matching, on chip, *S*-parameters, three-dimension.**

I. Introduction

With continued breakthrough in processing technology, over one billion transistors can now be integrated on a single chip. All these transistors are connected via interconnect lines. Interconnect design becomes one of the biggest design challenges in today's and next generation very large scale integration (VLSI) design. To address the increased complexity, over the past three decades, interconnect design methodology has experienced a series of transitions: from lumped resistance (R), lumped resistance and capacitance (RC), distributed RC, to distributed resistance, inductance, and capacitance (RLC) models. As the clock frequency of microprocessors entered the gigahertz regime, since it is necessary to analyze the chip response to harmonics 5 times the clock frequency, semiconductor industry started to validate RLC-based interconnect extraction at tens of gigahertz. Good agreement has been observed between measured data and static RLC-based modeling on purely 2-D test chip structures [1]. However, significant mismatch was observed at multigigahertz frequencies on 3-D interconnect structures [1]. In contrast, full-wave electromagnetics-based modeling accurately captured the measured behavior over the entire frequency band [1]. The mismatch between RLC models and measurements was shown to be attributed to the decoupled $\mathbf{E}$ and $\mathbf{H}$ in static modeling, and the capacitance and inductance were extracted in an independent fashion. This finding demonstrated the importance of electromagnetic (EM) analysis in high-frequency on-chip interconnect design. However, on-chip interconnect structures present many modeling challenges that are less pronounced in board and package level interconnects, which hinders the direct use of many traditional full-wave modeling techniques in realistic on-chip design. These challenges include high conductor loss, large aspect ratio, large number of conductors, the presence of silicon substrate, and strong nonuniformity [2].

A few techniques have been developed in recent years to address the full-wave modeling of on-chip interconnects. A 2-D finite difference time domain (FDTD) approach [3]–[9] has been developed for the full-wave modeling of on-chip transmission line structures. For 3-D interconnect structures, an FDTD solver was recognized as computationally expensive. This is not only because the large number of unknowns resulted from 3-D volumetric discretization, but also because the small geometrical sizes of the on-chip problems and the rapid field variation inside conductors. Different from FDTD, the partial element equivalent circuit (PEEC) method is an integral equation based method [10]–[16]. PEEC was first utilized to solve quasi-static problems. It was then extended to full-wave analysis [15]. Recently, surface-based PEEC methods have also been developed which reduce significantly the number of unknowns involved in a volume integral equation based PEEC method [13], [14]. Since integral equation based methods deal with dense matrices, a direct solver would require $O(N^3)$ operations and $O(N^2)$ storage in dealing with N number of unknowns, which is computationally expensive. The surface-based PEEC is under way to be accelerated by fast algorithms such as the fast multipole method, fast Fourier transform (FFT)-based

Manuscript received November 15, 2007; revised February 05, 2008. First published August 19, 2008; current version published November 28, 2008. This work was supported by Intel Corporation. This work was recommended for publication by Associate Editor J. Tan upon evaluation of the reviewers comments.

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Digital Object Identifier 10.1109/TADVP.2008.927813

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method, adaptive integral method, and fast QR-based methods [17]–[21]. Another surface integral equation based formulation was developed in [24]. A fast precorrected FFT scheme was formulated to accelerate the iterative solution of the dense matrix equation. The multilayered dielectric has not yet been accounted for. Integral equation based methods have also been developed in [22]–[26] for the application to on-chip problems. It is expected that an integral equation based solution that takes all the on-chip intricacies into consideration, and accelerated by the fast algorithms will soon be completed.

However, ultra large scale integrated circuit (IC) design results in numerical problems of ultra large scale, requiring billions of parameters to describe them accurately. To solve N number of parameters, the optimal computational complexity one can hope for is linear complexity $O(N)$. However, even $O(N)$ is inadequate in practice since N is too large in practical integrated systems. Therefore, it is of paramount importance to develop high-capacity electromagnetic solutions that can overcome the $O(N)$ problem size to achieve $O(M)$ with $M \ll N$, also in a rigorous fashion. In this paper, we propose a fast frequency-domain eigenvalue-based method for full-wave modeling of large-scale 3-D on-chip interconnect structures. Initial study of this method has been briefed in [27]. In this method, the complexity of 3-D interconnects is overcome by seeking the full-wave solution of a few 2-D problems, which are then postprocessed to obtain the solution of the original 3-D problem. In this paper, we will introduce segmentation of the interconnect structure and identification of the structure seeds, detail the eigenvalue-based formulation, present a new on-chip mode-matching technique that was not described in [27], introduce a junction matrix acceleration technique, present a fast frequency sweep analysis, and demonstrate the accuracy and high capacity of the proposed method by a number of numerical and experimental results.

II. Formulation

A. Segmentation of the Interconnect Structure and Identification of the Structure Seeds

To model a 3-D interconnect structure, first we slice it into segments. Each segment has a constant cross section. The segmentation direction, i.e., the longitudinal direction, is chosen from the x-, y-, and z-directions to minimize the number of unknowns in the transverse cross section. This is because the transverse cross section is numerically solved while the longitudinal direction is analytically processed in the proposed method.

After the segmentation, a set of unique structure seeds are identified. Take a typical Manhattan-type bus structure made of six metal layers as an example. Fig. 1(a)–(c) depicts its top view, end view (cross-sectional view), and side view respectively. Without loss of generality, assuming the bus is segmented along z-direction. This results in a large number of segments in a large-scale on-chip structure. However, the number of unique structure seeds is only a few. For a typical bus structure shown in Fig. 1, the number of structure seeds is only eight. This can be seen more clearly from Fig. 1(b). In each cross section, conductors in parallel layers (M2, M4, and M6 which are parallel to z) remain unchanged whereas the orthogonal lines in M1, M3, and M5 can be present or absent. This generates eight structure

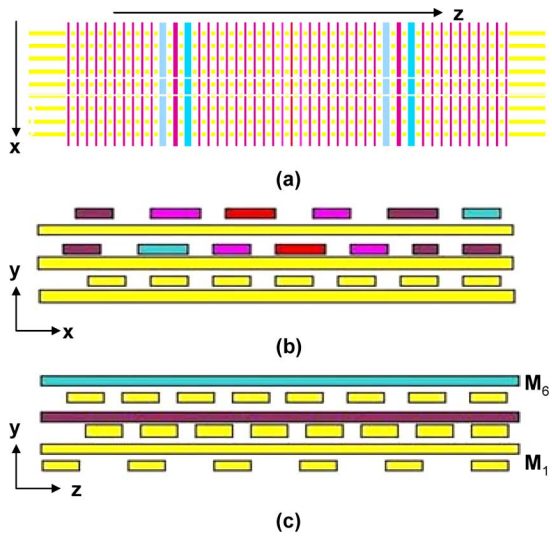

Fig. 1. Three-dimensional interconnect structure. (a) Top view. (b) End view. (c) Side view.

seeds. If we use three digits to describe each structure seed, the eight structure seeds can be represented by $000, 001, \ldots, 111$, respectively. The first, second, and third digits correspond to M5, M3, and M1 layers, respectively. For each digit, value 0 denotes the absence of the orthogonal lines in that layer, whereas value 1 denotes its presence. If the orthogonal lines are aligned in each layer, the total number of unique structure seeds is only 2. One refers to the presence of all of the orthogonal conductors. The other denotes their absence. The structure seeds are repeated in different lengths along the longitudinal direction, constructing the entire structure.

Note that the width (along x) and the spacing (along x) of the M2, M4, and M6 wires can be arbitrary. The width (along z) and the spacing (along z) of the M1, M3, and M5 wires can also be arbitrary. The width and spacing are not required to be equal to generate eight structure seeds. If M2, M4, and M6 wires have different lengths (along z), or M1, M3, and M5 wires have different lengths (along x), the number of structure seeds will be increased. However, the number of seeds is generally much smaller than that of segments in realistic on-chip interconnect structures.

The aforementioned scheme of segmentation and identification of structure seeds applies to interconnects with vias. For simplicity, consider a two-metal-layer power grid structure. This structure involves an orthogonal layer in M1 (orthogonal to z), and a parallel layer in M2 (parallel to z). Different from a bus-type structure, the orthogonal line in a power grid can be a VCC (power), a VSS (ground), or can be absent. As shown in Fig. 2, this structure involves only 3 structure seeds regardless of the width and spacing of M2-layer wires. In Fig. 2, VCCs are represented by shaded wires. The unshaded ones are VSSs. Vias can only exist between like wires.

B. Eigenvalue-Based Solution

Inside the interconnect structure, the electric field $\mathbf{E}$ satisfies the second-order vector wave equation

$$\nabla \times (\mu_r^{-1} \nabla \times \mathbf{E}) - k_0^2 \varepsilon_r \mathbf{E} + j\omega\mu_0\sigma\mathbf{E} = 0 \text{ in } \Omega \quad (1)$$

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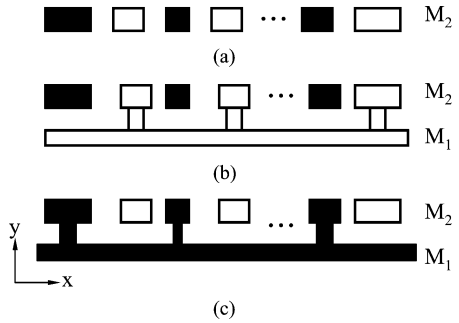

Fig. 2. Structure seeds in a two-metal-layer power grid. (a) Seed 1. (b) Seed 2 (orthogonal wire is a VSS wire). (c) Seed 3 (orthogonal wire is a VCC wire).

subject to certain boundary conditions such as

$$\hat{n} \times \mathbf{E} = 0 \quad \text{on } \Gamma_1$$
$$\hat{n} \times (\nabla \times \mathbf{E}) = 0 \quad \text{on } \Gamma_2. \tag{2}$$

In (1), μ_r, ε_r, and σ denote the relative permeability, relative permittivity, and conductivity, respectively, Ω is the computational domain which is the cross section of a structure seed including both dielectric and conducting regions, Γ_1 is the boundary where the Dirichlet boundary condition is applied, Γ_2 is the boundary where the Neumann boundary condition is applied. The truncation boundary is generally placed far away from the structure to minimize the impact of the truncation on the fields inside the computational domain. Either Dirichlet or Neumann boundary condition can be imposed on the truncation boundary without loss of accuracy when the truncation boundary is placed far away. The distance of the truncation boundary to the structure can be adaptively determined by varying the distance until the field solution does not change with the distance.

The incorporation of conductivity σ in (1) allows for the accurate modeling of both conductor and dielectric losses. This is of great importance for the accurate simulation of on-chip interconnects in which skin effects are dominant. By applying variational principle [28], it can be demonstrated that solving the boundary-value problem defined by (1) and (2) is equivalent to seeking the stationary point of the following functional [28], [29]

$$F(\mathbf{E}) = \frac{1}{2} \int \int_{\Omega} [\mu_r^{-1} (\nabla \times \mathbf{E}) \cdot (\nabla \times \mathbf{E})^* - k_0^2 \bar{\varepsilon}_r \mathbf{E} \cdot \mathbf{E}^*] d\Omega \tag{3}$$

where $\bar{\varepsilon}_r$ refers to the complex relative permittivity which comprises ε_r and σ.

Each structure seed has a constant cross section, and hence, wave propagating along longitudinal direction is analytical. Therefore, the z-dependence of all field components is $e^{-\gamma z}$, in which γ is the propagation constant. It is a complex number due to the conductor loss. With $e^{-\gamma z}$-type dependence, (3) can be rewritten as

$$F(\mathbf{E}) = \frac{1}{2} \int \int_{\Omega} [\mu_r^{-1} (\nabla_t \times \mathbf{E}_t) \cdot (\nabla_t \times \mathbf{E}_t)^* - k_0^2 \bar{\varepsilon}_r \mathbf{E} \cdot \mathbf{E}^* + \mu_r^{-1} (\nabla_t E_z + \gamma \mathbf{E}_t) \cdot (\nabla_t E_z + \gamma \mathbf{E}_t)^*] d\Omega \tag{4}$$

where ∇_t denotes the transverse del operator, $\mathbf{E}_t$ represents the transverse component of the electric field, and $\mathbf{E}_z$ signifies the z-component of the field.

To seek the solution of the above variational problem, the computational domain Ω is subdivided into small triangular elements. The transverse field within each element is expanded into edge basis functions $\boldsymbol{N}_i$ [28, pp. 276–279]

$$\mathbf{E}_t^e = \sum_{i=1}^{n} e_{ti}^e \mathbf{N}_i^e \tag{5}$$

where n denotes the number of basis functions per element, and e_{ti} denotes the corresponding expansion coefficient. The longitudinal field is represented by node basis functions ξ_i [28, pp. 95–97] as

$$E_z^e = \sum_{i=1}^{n} e_{zi}^e \xi_i^e \tag{6}$$

in which e_{zi} is the corresponding expansion coefficient. The discretization of the variational problem (4) by using (5) and (6) results in a generalized eigenvalue problem

$$\begin{bmatrix} \mathbf{A}_{tt} & 0 \\ 0 & 0 \end{bmatrix} \begin{Bmatrix} e_t \\ e_z \end{Bmatrix} = \gamma^2 \begin{bmatrix} \mathbf{B}_{tt} & \mathbf{B}_{tz} \\ \mathbf{B}_{zt} & \mathbf{B}_{zz} \end{bmatrix} \begin{Bmatrix} e_t \\ e_z \end{Bmatrix} \tag{7}$$

in which $\mathbf{A}$ and $\mathbf{B}$ are complex-valued matrices. Their matrix elements are given by

$$\mathbf{A}_{tt,ij} = \int \int_{\Omega} \left[\frac{1}{\mu_r} \{\nabla_t \times \mathbf{N}_i\} \cdot \{\nabla_t \times \mathbf{N}_j\} - k_0^2 \bar{\varepsilon}_r \mathbf{N}_i \cdot \mathbf{N}_j \right] d\Omega$$
$$\mathbf{B}_{tt,ij} = \int \int_{\Omega} \frac{1}{\mu_r} \mathbf{N}_i \cdot \mathbf{N}_j d\Omega$$
$$\mathbf{B}_{tz,ij} = \int \int_{\Omega} \frac{1}{\mu_r} \mathbf{N}_i \cdot \nabla_t \xi_j d\Omega$$
$$\mathbf{B}_{zt,ij} = \int \int_{\Omega} \frac{1}{\mu_r} \nabla_t \xi_i \cdot \mathbf{N}_j d\Omega$$
$$\mathbf{B}_{zz,ij} = \int \int_{\Omega} \left[\frac{1}{\mu_r} \{\nabla_t \xi_i\} \cdot \{\nabla_t \xi_j\} - k_0^2 \bar{\varepsilon}_r \xi_i \xi_j \right] d\Omega. \tag{8}$$

Obviously, the eigenvalues of (7) correspond to the propagation constants, whereas the eigenvectors characterize the transverse and longitudinal fields. Once (7) is solved, the electric field in each structure seed can be obtained as

$$\mathbf{E} = \sum_{m=1}^{n} [\alpha_m \mathbf{e}_m(x,y) e^{-\gamma_m z} + \beta_m \mathbf{e}_m(x,y) e^{\gamma_m z}] \tag{9}$$

which is a superposition of all of the forward and backward propagation modes that can be supported by the structure. It should be noted that the $\mathbf{E}$ field in (9) has all three components $\mathbf{E}_x, \mathbf{E}_y$, and $\mathbf{E}_z$.

Equation (7) can be denoted as

$$\mathbf{A}x = \lambda \mathbf{B}x. \tag{10}$$

It is solved by using an Arnoldi-based krylov subspace projection method [30]. To expedite the convergence, (10) is divided by k_0^2 at both sides. In addition, it is transformed to the following eigenvalue problem through a shift-invert operation:

$$(\mathbf{A} - \tau \mathbf{B})^{-1} \mathbf{B}x = \frac{1}{\lambda - \tau} x \tag{11}$$

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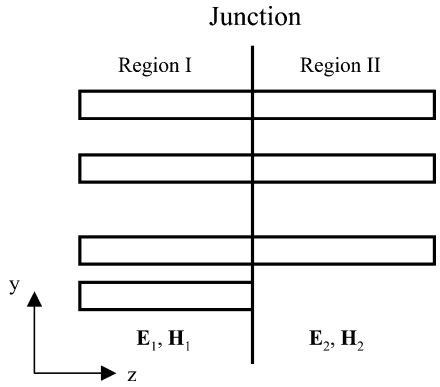

Fig. 3. Junction discontinuity in a 3-D interconnect structure (side view).

in which τ is chosen from the propagation constants of typical on-chip interconnect structures.

It is worth mentioning that the eigen-system (7) only needs to be solved for each unique structure seed, the number of which is many orders of magnitude less than that of the segments. This, in part, contributes to the efficiency of the proposed method.

C. On-Chip Mode-Matching Technique

The unknown coefficients α_m, and β_m in (9) are determined by imposing field continuity condition at each junction. As an example, consider an arbitrary junction along z in Fig. 3, which separates regions I and II. Fig. 3 is a y–z plane view of this junction. In region I, there are M1, M2, M4, and M6 layers, whereas in region II, M2, M4, and M6 are present. The electric field in region I can be represented as

$$\mathbf{E}_1 = \sum_{m=1}^{M} \xi_{1m} \mathbf{e}_{1m}(x,y) \tag{12}$$

in which $\xi_{1m} = \alpha_{1m} e^{-\gamma_{1m} z} + \beta_{1m} e^{\gamma_{1m} z}$, and M denotes the number of modes in region I. Similarly, the electric field in region II can be written as

$$\mathbf{E}_2 = \sum_{m=1}^{N} \xi_{2m} \mathbf{e}_{2m}(x,y) \tag{13}$$

in which $\xi_{2m} = \alpha_{2m} e^{-\gamma_{2m} z} + \beta_{2m} e^{\gamma_{2m} z}$, and N denotes the number of modes in region II. To impose field continuity condition at each junction, we develop a mode matching technique that is effective for on-chip interconnects as follows.

First, we construct the following two continuity conditions:

$$\sum_{m=1}^{M} \xi_{1m} \mathbf{e}_{1m,t}(x,y) = \sum_{m=1}^{N} \xi_{2m} \mathbf{e}_{2m,t}(x,y) \tag{14}$$

$$\sum_{m=1}^{M} \eta_{1m} \mathbf{J}_{1m,z}(x,y) = \sum_{m=1}^{N} \eta_{2m} \mathbf{J}_{2m,z}(x,y) \tag{15}$$

in which

$$\begin{aligned} \eta_{im} &= \alpha_{im} e^{-\gamma_{im} z} - \beta_{im} e^{\gamma_{im} z},\ i = 1,2 \\ \mathbf{J}_{im,z} &= j\omega\varepsilon \mathbf{e}_{im,z} + \sigma \mathbf{e}_{im,z},\ i = 1,2. \end{aligned} \tag{16}$$

Equation (14) enforces the tangential continuity of the electric field at the junction, whereas (15) enforces the normal continuity of the current. Next, we test (14) by $\{\boldsymbol{e}_{1n,t}(x,y), n = 1,2,3,\ldots M\}$, we obtain M equations

$$\begin{aligned} &\sum_{m=1}^{M} \xi_{1m} \langle \mathbf{e}_{1m,t}(x,y), \mathbf{e}_{1n,t}(x,y) \rangle \\ &= \sum_{m=1}^{N} \xi_{2m} \langle \mathbf{e}_{2m,t}(x,y), \mathbf{e}_{1n,t}(x,y) \rangle. \end{aligned} \tag{17}$$

Then we test (15) by $\{\boldsymbol{J}_{2n,z}(x,y), n = 1,2,3,\ldots N\}$, we obtain the other N equations

$$\begin{aligned} &\sum_{m=1}^{M} \eta_{1m} \langle \mathbf{J}_{1m,z}(x,y), \mathbf{J}_{2n,z}(x,y) \rangle \\ &= \sum_{m=1}^{N} \eta_{2m} \langle \mathbf{J}_{2m,z}(x,y), \mathbf{J}_{2n,z}(x,y) \rangle. \end{aligned} \tag{18}$$

Equations (17) and (18) yield $(M+N)$ equations at the junction. Combining this set of equations at each junction with the loading conditions, the unknown coefficients α_m, and β_m can be determined, and hence the field anywhere inside the interconnect structure is solved.

One thing worth mentioning is that we can also test (14) by eigen-modes in region II, $\{\mathbf{e}_{2n,t}(x,y), n = 1,2,3,\ldots N\}$; and (15) by eigen-modes in region I, $\{\mathbf{J}_{1n,z}(x,y), n = 1,2,3,\ldots M\}$. However, this testing is necessary but not sufficient for the specific junction shown in Fig. 3. To be sufficient, when testing $\mathbf{E}$, we choose testing modes from the segment that involves more conductors; when testing $\mathbf{J}$, we choose them from the one that involves fewer conductors. This is because the field continuity condition at the junction needs to be satisfied at both low and high frequencies. At high frequencies, on-chip wires behave more like conductors in traditional full-wave applications because the skin depth approaches to zero. It is known that the tangential $\mathbf{E}$ must vanish on a perfect conducting surface. Although the conductor in real applications is not perfect, the zero tangential $\mathbf{E}$ is still a very good approximation at high frequencies. Therefore, this type of hard boundary conditions needs to be enforced at the junction by choosing testing modes from the segment that involves more conductors when testing $\mathbf{E}$.

The number of modes is chosen based on the convergence of the numerical solution. If only dominant modes (quasi-TEM) are important (i.e., other evanescent modes are attenuated very rapidly) in the frequency band of interest, (14) and (15) can be simplified to

$$\begin{aligned} &\sum_{m=1}^{M} \xi_{1m} \int \mathbf{e}_{1m,t}(x,y) \cdot d\mathbf{l}_i \\ &\quad = \sum_{m=1}^{N} \xi_{2m} \int \mathbf{e}_{2m,t}(x,y) \cdot d\mathbf{l}_i,\ i = 1,2,\ldots M \\ &\sum_{m=1}^{M} \eta_{1m} \int \mathbf{J}_{1m,z}(x,y) \cdot d\mathbf{A}_j \\ &\quad = \sum_{m=1}^{N} \eta_{2m} \int \mathbf{J}_{2m,z}(x,y) \cdot d\mathbf{A}_j,\ j = 1,2,\ldots N \end{aligned} \tag{19}$$

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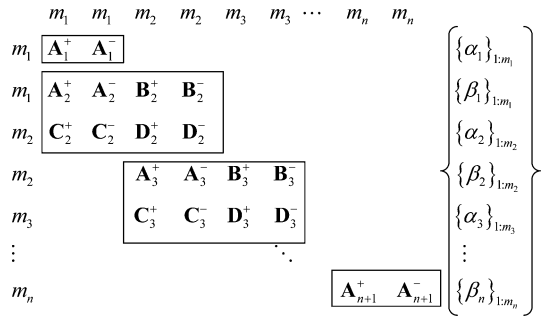

Fig. 4. Illustration of the junction matrix.

in which $\boldsymbol{l}_i$ is the path from the ith conductor to the ground, and $\mathbf{A}_j$ is the cross-sectional area of the jth conductor. The ground is the physical ground present in the structure, for example, the bottom of the silicon substrate. For the realistic on-chip interconnect structures we have tested, it is observed that the number of propagation modes is orders of magnitude smaller than the number of unknowns in a transverse cross section. In addition, the number of propagation modes that can be observed in the current operating frequency band is limited.

D. Junction-Matrix Acceleration Technique

Matching the field continuity at the junction will result in a matrix, from which the unknown coefficients α_m, and β_m are determined. We denote this matrix as a junction matrix. Due to the large number of junctions in a realistic on-chip interconnect structure, the dimension of the junction matrix can be very large. Take an interconnect of n segments as an example, its junction matrix resulted from (17) and (18) is shown in Fig. 4, in which m_i denotes the number of modes in the ith segment, $\{\alpha_i\}$ and $\{\beta_i\}$ denote the transmission, and reflection coefficients, respectively, in the ith segment. The dimension of $\{\alpha_i\}$ as well as $\{\beta_i\}$ is m_i.

Each boxed matrix in Fig. 4 corresponds to the matrix equations formed at one junction by using (17) and (18). The matrices formed at the first and the last junction only involve unknown coefficients of one segment. Therefore, their dimensions are different from those of the other boxed matrices. In a boxed matrix $j(j = 2, \ldots, n)$, $\mathbf{A}_j^+$ denotes the submatrix associated with $\{\alpha_{j-1}\}$ which are the transmission coefficients in the $(j$-1)th segment; $\mathbf{A}_j^-$ is the submatrix associated with $\{\beta_{j-1}\}$ which are the reflection coefficients in the $(j$-1)th segment; $\mathbf{B}_j^+$ is the submatrix associated with $\{\alpha_j\}$; and $\mathbf{B}_j^-$ is the submatrix associated with $\{\beta_j\}$. Take the second boxed matrix in Fig. 4 as an example, the eight submatrices can be written as

$$\begin{aligned}
\mathbf{A}_2^+ &= \langle \mathbf{e}_{1n,t}(x,y), \mathbf{e}_{1m,t}(x,y)\rangle e^{-\gamma_{1m} z_1}, \\
&\quad n = 1, \ldots m_1,\ m = 1, \ldots m_1 \\
\mathbf{A}_2^- &= \langle \mathbf{e}_{1n,t}(x,y), \mathbf{e}_{1m,t}(x,y)\rangle e^{\gamma_{1m} z_1}, \\
&\quad n = 1, \ldots m_1,\ m = 1, \ldots m_1 \\
\mathbf{B}_2^+ &= \langle \mathbf{e}_{1n,t}(x,y), \mathbf{e}_{2m,t}(x,y)\rangle e^{-\gamma_{2m} z_1}, \\
&\quad n = 1, \ldots m_1,\ m = 1, \ldots m_2 \\
\mathbf{B}_2^- &= \langle \mathbf{e}_{1n,t}(x,y), \mathbf{e}_{2m,t}(x,y)\rangle e^{\gamma_{2m} z_1}, \\
&\quad n = 1, \ldots m_1,\ m = 1, \ldots m_2
\end{aligned} \tag{20a}$$

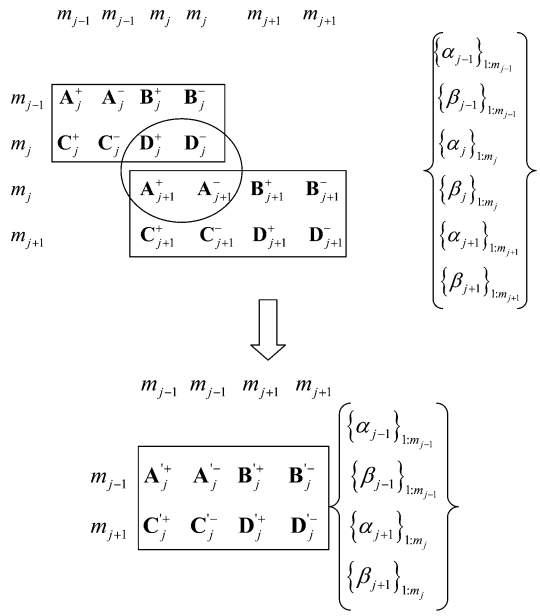

Fig. 5. Illustration of the matrix reduction.

and

$$\begin{aligned}
\mathbf{C}_2^+ &= \langle \mathbf{J}_{2n,z}(x,y), \mathbf{J}_{1m,z}(x,y)\rangle e^{-\gamma_{1m} z_1}, \\
&\quad n = 1, \ldots m_2,\ m = 1, \ldots m_1 \\
\mathbf{C}_2^- &= -\langle \mathbf{J}_{2n,z}(x,y), \mathbf{J}_{1m,z}(x,y)\rangle e^{\gamma_{1m} z_1}, \\
&\quad n = 1, \ldots m_2,\ m = 1, \ldots m_1 \\
\mathbf{D}_2^+ &= \langle \mathbf{J}_{1n,z}(x,y), \mathbf{J}_{2m,z}(x,y)\rangle e^{-\gamma_{2m} z_1}, \\
&\quad n = 1, \ldots m_2,\ m = 1, \ldots m_2 \\
\mathbf{D}_2^- &= -\langle \mathbf{J}_{2n,z}(x,y), \mathbf{J}_{2m,z}(x,y)\rangle e^{\gamma_{2m} z_1}, \\
&\quad n = 1, \ldots m_2,\ m = 1, \ldots m_2.
\end{aligned} \tag{20b}$$

The junction matrix is of dimension $\sum_{i=1}^{n} 2m_i \times \sum_{i=1}^{n} 2m_i$. It is sparse. Though sparse, its computation remains expensive when the size is large. To solve this problem, the following technique is developed.

Instead of solving the matrix as a whole, we reduce it to a matrix that only involves unknown coefficients α_i and β_i in the first and last segment, where the circuit parameters are extracted. Consider a submatrix formed at the j- and $(j+1)$th junctions, which involves unknowns in the $(j$-1)-, j-, and $(j+1)$th segments. This matrix can be reduced to involve unknowns in the $(j$-1)th and $(j+1)$th segments only, as shown in Fig. 5. The reduction cost is simply the inversion of the circled matrix. Its dimension is $2m_j$, in which m_j is the number of modes in the jth segment.

The reduction is achieved by first solving $\{\alpha_j\}$ and $\{\beta_j\}$ in terms of $\{\alpha_{j-1}\}, \{\beta_{j-1}\}, \{\alpha_{j+1}\}$, and $\{\beta_{j+1}\}$; and then transforming the original matrix accordingly by eliminating $\{\alpha_j\}$ and $\{\beta_j\}$. Mathematically, it can be performed as follows. First, we evaluate the following matrices:

$$\begin{aligned}
\mathbf{T} &= -\begin{bmatrix} \mathbf{D}_j^+ & \mathbf{D}_j^- \\ \mathbf{A}_{j+1}^+ & \mathbf{A}_{j+1}^- \end{bmatrix}^{-1} \begin{bmatrix} \mathbf{C}_j^+ & \mathbf{C}_j^- & 0 & 0 \\ 0 & 0 & \mathbf{B}_{j+1}^+ & \mathbf{B}_{j+1}^- \end{bmatrix} \\
\tilde{\mathbf{B}} &= [\mathbf{B}_j^+ \quad \mathbf{B}_j^-]\mathbf{T} \\
\tilde{\mathbf{C}} &= [\mathbf{C}_{j+1}^+ \quad \mathbf{C}_{j+1}^-]\mathbf{T}.
\end{aligned} \tag{21}$$

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in which $\mathbf{T}$ satisfies

$$\begin{Bmatrix} \alpha_j \\ \beta_j \end{Bmatrix} = \mathbf{T} \begin{Bmatrix} \alpha_{j-1} \\ \beta_{j-1} \\ \alpha_{j+1} \\ \beta_{j+1} \end{Bmatrix} \tag{21a}$$

We then denote $\tilde{\mathbf{B}}$ and $\tilde{\mathbf{C}}$ as

$$\begin{aligned} \tilde{\mathbf{B}} &= [\tilde{\mathbf{B}}_j^+ \quad \tilde{\mathbf{B}}_j^- \quad \tilde{\mathbf{B}}_{j+2}^+ \quad \tilde{\mathbf{B}}_{j+2}^-] \\ \tilde{\mathbf{C}} &= [\tilde{\mathbf{C}}_j^+ \quad \tilde{\mathbf{C}}_j^- \quad \tilde{\mathbf{C}}_{j+2}^+ \quad \tilde{\mathbf{C}}_{j+2}^-]. \end{aligned} \tag{22}$$

The reduced matrix can then be obtained from the original one as the following:

$$\begin{aligned} &\mathbf{A}'^+_j = \mathbf{A}^+_j + \tilde{\mathbf{B}}^+_j, \mathbf{A}'^-_j = \mathbf{A}^-_j + \tilde{\mathbf{B}}^-_j \\ &\mathbf{B}'^+_j = \tilde{\mathbf{B}}^+_{j+2}, \mathbf{B}'^-_j = \tilde{\mathbf{B}}^-_{j+2} \\ &\mathbf{C}'^+_j = \tilde{\mathbf{C}}^+_j, \mathbf{C}'^-_j = \tilde{\mathbf{C}}^-_j \\ &\mathbf{D}'^+_j = \mathbf{D}^+_{j+1} + \tilde{\mathbf{C}}^+_{j+2}, \mathbf{D}'^-_j = \mathbf{D}^-_{j+1} + \tilde{\mathbf{C}}^-_{j+2}. \end{aligned} \tag{23}$$

By repeatedly applying the aforementioned reduction procedure, we obtain a matrix that only involves unknowns in the first and last segment, which can be readily solved.

E. Fast Frequency Sweep Technique

Equation (7) can be denoted as

$$\mathbf{A}(k)\{e(k)\} = \lambda(k)\mathrm{B}(k)\{e(k)\} \tag{24}$$

where k is the wave number, and $\{\cdot\}$ denotes a vector. The dimension of $\{e(k)\}$ is the size of matrices $\mathbf{A}$ and $\mathbf{B}$. Because (24) is frequency dependent, it has to be solved at each discrete frequency point, which is time consuming. Here, we employ asymptotic waveform evaluation (AWE) method [31]–[35] to alleviate this problem. AWE has been applied to accelerate the method-of-moment and finite-element solution of scattering, radiation, waveguide, and circuit problems. It has not been applied to the fast frequency sweep analysis of on-chip interconnect problems yet. Here, we first expand $\lambda(k)$ and $\{e(k)\}$ into Taylor series

$$\begin{aligned} \lambda(k) &= \sum_{n=0}^{Q} \lambda_n (k - k_0)^n \\ \{e(k)\} &= \sum_{n=0}^{Q} \{m_n\}(k - k_0)^n \end{aligned} \tag{25}$$

where k_0 is the expansion point, λ_n and $\{m_n\}$ denote the unknown coefficients of $\lambda(k)$ and $\{e(k)\}$, respectively, and Q denotes the order of the expansion. Matrix $\mathbf{A}(k)$ and $\mathbf{B}(k)$ are also expanded into Taylor series with the same order Q. It is worth mentioning that to expedite the convergence of the eigenvalue solution, (10) is divided by k_0^2 at both sides. As a result, higher-order derivatives with respect to k can exist.

Substituting (25) into (24) and matching the coefficients of the equal powers of $(k - k_0)$ on both sides lead to a set of equations relating $\{m_n\}$ and λ_n. By imposing the orthogonality condition

$$\{m_0\}^T[\mathbf{A}^{(0)} - \lambda_0\mathbf{B}^{(0)}]\{m_i\} = 0,\ i > 0 \tag{26}$$

we obtain the following recursive formulation for $\{m_n\}$ and λ_n, shown in (27) at the bottom of the page, where $\mathbf{A}^{(i)}$ and $\mathbf{B}^{(i)}$ denote the ith derivative of $\mathbf{A}$ and $\mathbf{B}$ at the expansion point k_0. Since the bandwidth of Taylor expansion is limited, we convert Taylor series into a Padé rational function, which has a larger radius of convergence. The Padé expansion is as follows:

$$\begin{aligned} \{e(k)\} &= \frac{\sum_{i=0}^{L}\{a_i\}(k - k_0)^i}{1 + \sum_{j=1}^{M}\{b_j\}(k - k_0)^j} \\ \lambda(k) &= \frac{\sum_{i=0}^{L} c_i(k - k_0)^i}{1 + \sum_{j=1}^{M} d_j(k - k_0)^j} \end{aligned} \tag{28}$$

where $L + M = Q$. From (25) and (28), the unknown coefficients a_i, b_j, c_i, d_j can be obtained by matching the coefficients of the equal powers of $k - k_0$ [32].

F. Circuit-Parameter Extraction Technique

Solution of the fields enables the calculation of circuit parameters. When the transmission line model is valid, the RLGC parameters can be extracted in the following fashion. First, we obtain the eigen-voltage and eigen-current of each conductor for each mode by performing the following line or area integrals:

$$\begin{aligned} \nu_{m,i} &= \int \mathbf{e}_{m,t}(x,y) \cdot dl_i \quad i = 1, 2, \ldots, n \\ \iota_{m,i} &= \oiint [j\omega\varepsilon e_{m,z}(x,y) + \sigma e_{m,z}(x,y)] dS_i \end{aligned} \tag{29}$$

where m denotes the index of mode; i denotes the index of conductor; $\boldsymbol{e}_{m,t}(x,y)$ and $\boldsymbol{e}_{m,z}(x,y)$ represent the tangential, and longitudinal electric field of the mth eigen-mode respectively. When transmission line model holds true, in the transverse plane that is perpendicular to the wave propagation direction, the potential is almost the same at each point on the conductor cross section. This is the reason the capacitance per unit length of a transmission line can be extracted by solving Poisson's equation. Therefore, when performing the line integral of (29) to evaluate voltage, one end point is selected at the physical ground, and the other end point can be arbitrarily selected on the conductor cross section.

Substituting (29) and propagation constant γ_m into the telegraph equation

$$\begin{aligned} \gamma_m\{\nu_{m,i}\} &= [R + j\omega L]_{i,j}\{\iota_{m,j}\} \\ \gamma_m\{\iota_{m,i}\} &= [G + j\omega C]_{i,j}\{\nu_{m,j}\} \\ &\qquad i = 1, 2, \ldots n;\ j = 1, 2, \ldots n;\ m = 1, 2, \ldots M \end{aligned} \tag{30}$$

we obtain the RLGC matrices. Note that in contrast to the RLGC matrices obtained via quasi-static solvers that employ a decou-

$$\begin{aligned} \lambda_n &= \frac{\{m_0\}^T \cdot \left(\sum_{i=0}^{n-1} \mathbf{A}^{(n-i)}\{m_i\} - \sum_{i=1}^{n-1}\sum_{j=0}^{n-i} \lambda_j \mathbf{B}^{(n-i-j)}\{m_i\} - \sum_{i=0}^{n-1} \lambda_i \mathbf{B}^{(n-i)}\{m_0\}\right)}{\{m_0\}^T \mathbf{B}^{(0)}\{m_0\}} \\ \{m_n\} &= (\mathbf{A}^{(0)} - \lambda_0\mathbf{B}^{(0)})^{-1} \cdot \left(\sum_{i=1}^{n-1}\sum_{j=0}^{n-i} \lambda_j \mathbf{B}^{(n-i-j)}\{m_i\} + \sum_{i=0}^{n} \lambda_i \mathbf{B}^{(n-i)}\{m_0\} - \sum_{i=0}^{n-1} \mathbf{A}^{(n-i)}\{m_i\}\right) \end{aligned} \tag{27}$$

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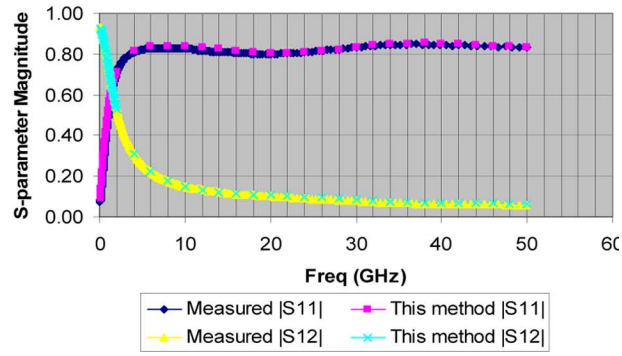
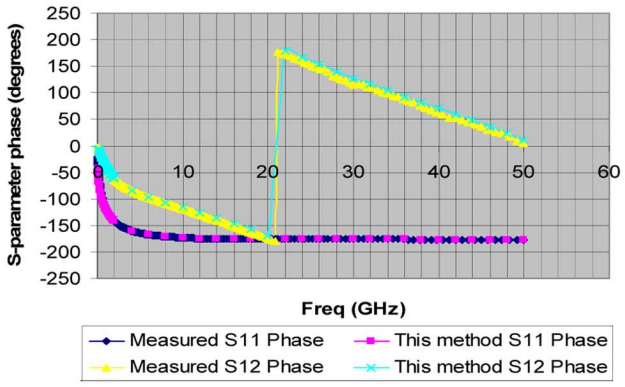
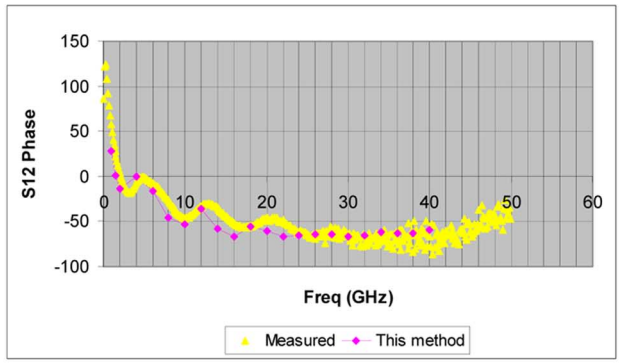


(a)

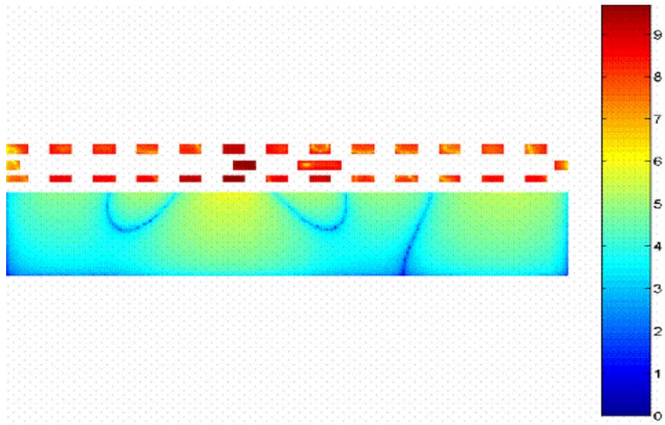


(b)

Fig. 6. *S*-parameters of a 3-D on-chip interconnect. (a) Magnitude. (b). Phase. (From [27]).



(a)



(b)

Fig. 7. Three-dimensional on-chip crosstalk structure. (a) Phase of S12. (b) Slice of current distribution. (From [27]).

pled electric and magnetic field model, here, any coupling between $\mathbf{E}$ and $\mathbf{H}$, no matter how weak, is captured accurately.

For 3-D interconnect structures or interconnects working at high frequencies, *S*-parameters become a necessity for an accurate description of their electrical behavior. To extract them, we first construct the total voltage and current of each conductor at the ports by performing the following integrals:

$$V_i = \sum_{m=1}^{M}[(\alpha_m e^{-\gamma_m z} + \beta_m e^{\gamma_m z}) \int \mathbf{e}_{m,t}(x,y)\cdot dl_i]$$

$$I_i = \sum_{m=1}^{M}[(\alpha_m e^{-\gamma_m z} - \beta_m e^{\gamma_m z}) \oiint (j\omega\varepsilon e_{m,z} + \sigma e_{m,z}) dS_i]$$

$$i = 1, 2, \ldots n;\ j = 1, 2, \ldots n;\ m = 1, 2, \ldots M. \quad (31)$$

Since in circuit applications, *S*-parameters of interest are those of dominant modes, i.e., quasi TEM modes. For these modes, the $\mathbf{E}$ distribution in the transverse plane obeys that of a static field, and hence the voltage obtained by using the line integral of (31) is not sensitive to the choice of integration path.

After extracting the total voltage and current of each conductor, we load each conductor by the reference impedance (usually 50Ω in industry standard), and excite the conductor in turn, which can be mathematically represented as

$$\begin{cases} V_i + Z_{\text{ref}} I_i = 1, & i = 1, 2, \ldots, n \\ V_j + Z_{\text{ref}} I_j = 0, & j = 1, 2, \ldots, n, j \neq i \end{cases}. \quad (32)$$

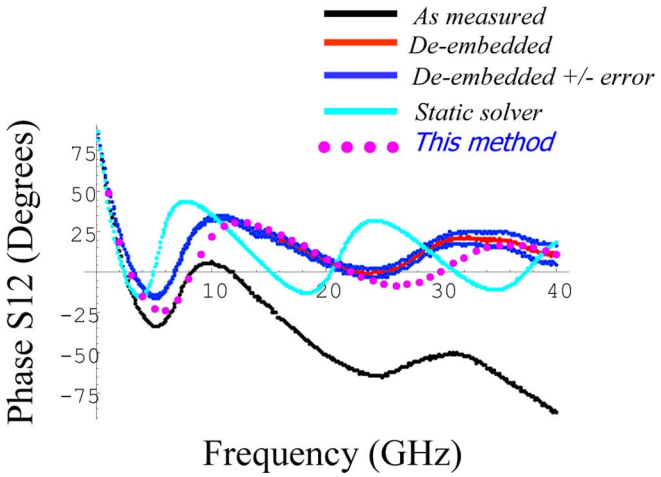


Fig. 8. Crosstalk phase of a 3-D interconnect structure with orthogonal returns.

The loading condition in (32) together with the boundary condition at each junction yield the solution of unknown coefficients α_m, and β_m, and hence, the total voltage and current of each conductor. As a result, the *S*-parameters can be obtained as follows:

$$S_{ij} = \frac{V_j - Z_{\text{ref}} I_j}{V_i + Z_{\text{ref}} I_i}, i = 1, 2, \ldots, n;\ j = 1, 2, \ldots n. \quad (33)$$

III. Numerical Results

To test the accuracy of the proposed algorithm, we simulated a set of interconnect structures that were fabricated on a test chip

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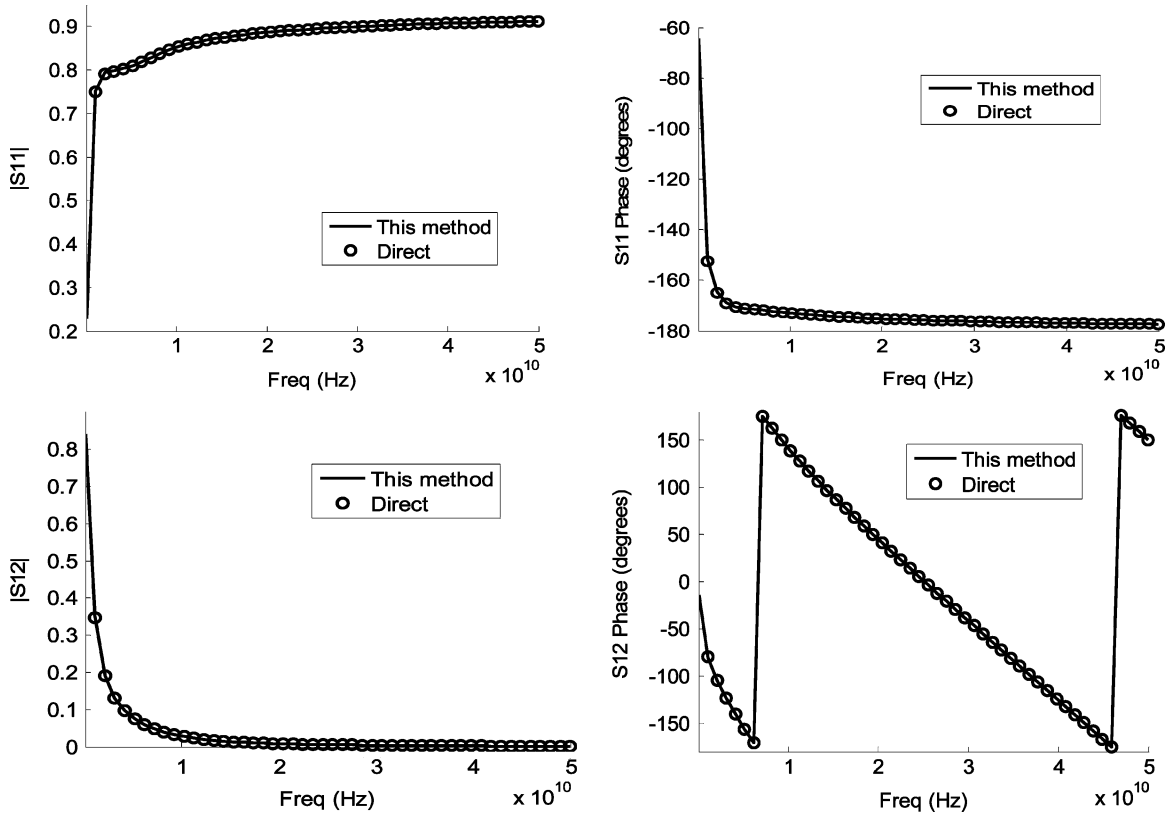

Fig. 9. *S*-parameters of an on-chip interconnect simulated by the proposed method. (In the legend, this method refers to the direct method accelerated by fast techniques).

using conventional silicon processing techniques. High resolution cross-sectional scanning electron microscopy and optical microscopy were used to measure the relevant dimensions of the fabricated structures. Parasitics signals were removed from the measured *S*-parameters using a de-embedding approach [1], [36]. In Fig. 6, we compare measured and simulated *S*-parameters of an on-chip three-metal-layer interconnect structure. It involves a 10-μm-wide strip in metal 2 (M2) layer, one ground plane in metal 1 (M1) layer, and one ground plane in metal 3 (M3) layer. There are returns in M2 layers, but they are far from the strip. The strip is of a length of 2000 μm. The *S*-parameters were measured at the near and far end of the strip line. As can be seen from Fig. 6, the agreement of *S*-parameters is excellent in both magnitude and phase.

Fig. 7(a) shows the simulated crosstalk of another 2000-μm long on-chip interconnect versus the measured data. The crosstalk was measured at the near ends of the two centered interconnect lines in M2 layer as shown in Fig. 7(b). Again, it can be observed that the *S*-parameters are in very good agreement. Fig. 7(b) also shows the current distribution on a cross section at 40 GHz with the excited signal on the left in the M2 layer. The current induced on surrounding conductors exhibits a complex pattern, which reflects the mutual coupling among these conductors. In addition, we observe current induced in the lossy silicon substrate. The nulls observed in the substrate are due to the destructive interaction between reflected and transmitted waves.

Next, we simulated a crosstalk structure with 2000 orthogonal interconnects in M1 and M3 layers. The crosstalk was measured at the near ends of two adjacent lines residing in the M2 layer. Due to a nondisclosure agreement, the detail of the structure is not reported here. Fig. 8 depicts the phase of S12 obtained by the proposed full-wave modeling method in comparison with the measured data and that obtained by a static solver. Clearly, the static solvers exhibit a significant disagreement with the measured data especially at high frequencies, whereas the full-wave data produced by the present method exhibits an excellent agreement. In Fig. 8, raw measured data without de-embedding is also given, which indicates the difficulty of on-chip measurements. The true signal can be significantly contaminated by parasitic signals which need to be de-embedded correctly.

To demonstrate the efficiency and accuracy of the proposed fast frequency sweep technique and junction matrix acceleration technique, we considered a three-metal-layer on-chip interconnect structure. The structure is of 300 μm width. It involves a 10-μm-wide strip in M2 layer, one ground plane in M1 layer, and one ground plane in M3 layer. The distance of this strip to the M2 returns at the left and right hand sides are 50 μm, respectively. The strip is 0.285 μm thick and 2000 μm long. With a frequency step of 1 GHz, it takes the direct method 34.9 s to obtain the solution over 50 MHz $\sim$ 50 GHz frequency band. With two expansion points at 12.5 and 37.5 GHz, and a sixth-order Padé expansion $(Q = 6, L = 3, M = 3)$, the proposed method yields an accurate solution over the whole band in 2.9 s. The speedup is 12 times. Fig. 9 shows the *S*-parameters simulated by the proposed techniques in comparison with the direct method, which reveals an excellent agreement. Since this structure only involves one segment along the longitudinal direction, the speedup is solely attributed to the fast frequency sweep technique. Next, we consider a 3-D on-chip interconnect that involves 2000 segments along the longitudinal direction. The M1 and M3 metal layers are

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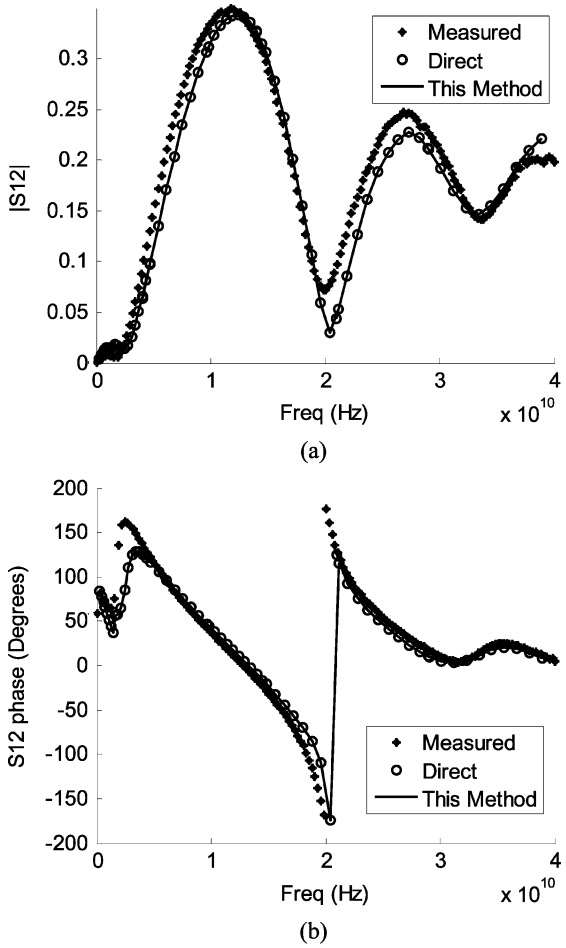

Fig. 10. Crosstalk of a 3-D interconnect of length 2000 μm with orthogonal returns. (a) Magnitude. (b) Phase.

populated by orthogonal returns. These returns are 1 μm wide each and 1 μm wide apart. The length of the structure is 2000 μm. The crosstalk is observed between two wires embedded in the M2 layer. One is of 2.1 μm width; the other is of 1.1 μm width. The spacing between these two wires is 1.95 μm. The distance to the M2 returns of both wires is 10.3 μm. Fig. 10 depicts the simulated *S*-parameters in comparison with the results obtained from the direct method. With a frequency step of 1 GHz, the direct simulation takes 981 s to simulate the entire frequency band, whereas the proposed fast techniques speed it up by more than 39 times. The measured crosstalk is also given in Fig. 10. Clearly, the proposed method accurately predicted the measured behavior.

IV. Conclusion

This paper presents a fast and high-capacity full-wave modeling technique for large-scale 3-D on-chip interconnects. This technique formulates a generalized eigenvalue representation of the original wave propagation problem that can comprehend arbitrary dielectric and conductor configurations in the transverse cross section, both conductor and dielectric losses, and arbitrary materials. A new on-chip mode matching technique is developed to solve large-scale 3-D problems with 2-D-like computational expenses. If one has computational resources to solve one 2-D structure seed, with the proposed method, he is able to solve the entire 3-D interconnect structure. The solution obtained from the proposed scheme satisfies both Maxwell's equations and boundary conditions, and hence constitutes a rigorous solution. The boundary condition in the transverse cross section is satisfied by the finite element procedure; while the boundary condition along the longitudinal direction is satisfied by the mode-matching process. A junction matrix acceleration technique is developed to speed up the numerical mode matching process. A fast frequency sweep technique is employed to avoid repeating the computation at each discrete frequency point. A comprehensive characterization of the interconnect is conducted, which includes *S*-parameters, full-wave RLGC, propagation constants, characteristic impedances, voltage, current, and field distributions. Experimental and numerical results demonstrate its validity.

Acknowledgment

The authors would like to thank Dr. M. J. Kobrinsky at Intel Corporation for providing measured data.

References

[1] M. J. Kobrinsky *et al.*, "Experimental validation of crosstalk simulations for on-chip interconnects at high frequencies using s-parameters," in *IEEE 12th Topical Meeting Electr. Performance Electron. Packag. (EPEP)*, 2003, pp. 329–332.

[2] D. Jiao, C. Dai, S. W. Lee, T. R. Arabi, and G. Taylor, "Computational electromagnetics for high-frequency IC design," in *IEEE Int. Symp. Antennas Propag.*, 2004, pp. 3317–3320.

[3] Z. Y. Yuan, Z. F. Li, and M. L. Zou, "Computer-aided analysis of on-chip interconnects near semiconductor substrate for high-speed VLSI," *IEEE Trans. Computer-Aided Design Integr. Circuits Syst.*, vol. 19, no. 9, pp. 990–998, Sep. 2000.

[4] F. Arndt, V. J. Brankovis, and D. V. Krupezevic, "An improved FDTD full-wave analysis for arbitrary guiding structures using a two-dimensional mesh," in *IEEE MTT-S Microwave Symp. Dig.*, Albuquerque, NM, Jun. 1992, pp. 389–392.

[5] A. C. Cangellaris, "Numerical stability and numerical dispersion of a compact 2-D/FDTD method used for the dispersion analysis of waveguides," *IEEE Microw. Guided Wave Lett.*, vol. 3, no. 1, pp. 3–5, Jan. 1993.

[6] V. J. Brankovic, D. V. Krupezevic, and F. Arndt, "An efficient two-dimensional graded mesh finite-difference time-domain algorithm for shielded or open waveguide structure," *IEEE Trans. Microw. Theory Tech.*, vol. 40, no. 12, pp. 2272–2277, Dec. 1992.

[7] C. Reig, E. A. Navarro, and V. Such, "Calculation of the characteristic impedance of microstrip using a full-wave 2-D FDTD scheme," *Microwave Opt. Tech. Lett.*, vol. 16, pp. 58–60, Sep. 1997.

[8] A. Asi and L. Shafai, "Dispersion analysis of anisotropic inhomogeneous waveguides using compact 2-D-FDTD," *Electron. Lett.*, vol. 28, no. 15, pp. 1451–1452, Jul. 1992.

[9] S. Xiao, R. Vahldieck, and H. Jin, "Full-wave analysis of guided wave structures using a novel 2-D FDTD," *IEEE Microwave Guided Wave Lett.*, vol. 2, pp. 165–167, May 1992.

[10] A. E. Ruehli, "Equivalent circuit models for three-dimensional multiconductor systems," *IEEE Trans. Microwave Theory Tech.*, vol. M-22, no. 3, pp. 216–221, Mar. 1974.

[11] A. E. Ruehli, G. Antonini, J. Esch, J. Ekman, A. Mayo, and A. Orlandi, "Nonorthogonal PEEC formulation for time- and frequency-domain EM and circuit modeling," *IEEE Trans. Electromagn. Compat.*, vol. 45, no. 2, pp. 167–176, May 2003.

[12] Y. Wang, V. Jandhyala, and C. J. Shi, "Coupled electromagnetic-circuit simulation of arbitrarily-shaped conducting structures," in *IEEE 12th Topical Meeting Electr. Performance Electron. Packag. (EPEP)*, 2001, pp. 233–236.

[13] A. Rong, A. C. Cangellaris, and L. Dong, "Comprehensive broadband electromagnetic modeling of on-chip interconnects with a surface discretization-based generalized PEEC model," in *IEEE 12th Topical Meeting Electr. Performance Electron. Packag. (EPEP)*, 2003, pp. 367–370.

[14] D. Gope , A. E. Ruehli, C. Yang, and V. Jandhyala , "(S)PEEC: Time- and frequency-domain surface formulation for modeling conductors and dielectrics in combined circuit electromagnetic simulations," *IEEE Trans. Microw. Theory Tech.*, vol. 54, no. 6, pp. 2453–2464, Jun. 2006.

[15] P. J. Restle, A. E. Ruehli, S. G. Walker, and G. Papadopoulos, "Full-wave PEEC time-domain method for the modeling of on-chip interconnects," *IEEE Trans. Computer-Aided Design Integr. Circuits Syst.*, vol. 20, no. 7, pp. 877–886, Jul. 2001.

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[16] R. Jiang, W. Fu, and C. C. Chen, "EPEEC: Comprehensive spice-compatible reluctance extraction for high-speed interconnects above lossy multilayer substrates," *IEEE Trans. Computer-Aided Design Integr. Circuits Syst.*, vol. 24, no. 10, pp. 1562–1571, Oct. 2005.
[17] *Fast and Efficient Algorithms in Computational Electromagnetics*, W. C. Chew, J. M. Jin, E. Michielssen, and J. M. Song, Eds. Norwood, MA: Artech House, 2001, p. 931.
[18] J. R. Phillips and J. K. White, "A precorrected-FFT method for electrostatic analysis of complicated 3-D structures," *IEEE Trans. Computer-Aided Design Integr. Circuits Syst.*, vol. 16, no. 10, pp. 1059–1072, Oct. 1997.
[19] E. Bleszynski, M. Bleszynski, and T. Jarozewicz, "AIM: Adaptive integral method for solving large-scale electromagnetic scattering and radiation problems," *Radio Sci.*, vol. 31, pp. 1225–1251, Sep.–Oct. 1996.
[20] S. Kapur and D. E. Long, "IES3: A fast integral equation solver for efficient 3-dimensional extraction," in *Proc. Int. Conf. Comput. Aided Design*, San Jose, CA, Nov. 1997, pp. 448–455.
[21] A. Ruehli, D. Gope, and V. Jandhyala, "Block partitioned gauss-seidel PEEC solver accelerated by qr-based coupling matrix compression techniques," in *IEEE 13th Topical Meeting Electr. Performance Electron. Packag. (EPEP)*, 2004, pp. 325–328.
[22] Z. G. Qian, J. Xiong, L. Sun, I. T. Chiang, W. C. Chew, L. J. Jiang, and Y. H. Chu, "Crosstalk analysis by fast computational algorithms," in *IEEE 14th Topical Meeting Electr. Performance Electron. Packag.*, 2005, pp. 367–370.
[23] A. E. Yilmaz, J. M. Jin, and E. Michielssen, "A parallel FFT-accelerated transient field-circuit simulator," *IEEE Trans. Microwave Theory Tech.*, vol. 53, no. 9, pp. 2851–2865, Sep. 2005.
[24] Z. H. Zhu, B. Song, and J. K. White, "Algorithms in fastimp: A fast and wideband impedance extraction program for complicated 3-D geometries," *IEEE Trans. Computer-Aided Design Integrated Circuits Syst.*, vol. 24, no. 7, pp. 981–998, Jul. 2005.
[25] F. Ling, V. I. Okhamtovski, W. Harris, S. McCracken, and A. Dengi, "Large-scale broad-band parasitic extraction for fast layout verification of 3-D RF and mixed-signal on-chip structures," *IEEE Trans. Microw. Theory Tech.*, vol. 53, no. 1, pp. 264–273, Jan. 2005.
[26] S. Kapur and D. E. Long, "Large-scale full-wave simulation," *Proc. Design Automation Conf.*, pp. 806–809, 2004.
[27] D. Jiao, M. Mazumder, S. Chakravarty, C. Dai, M. J. Kobrinsky, M. C. Harmes, and S. List, "A novel technique for full-wave modeling of large-scale three-dimensional high-speed on/off-chip interconnect structures," in *Int. Conf. Simulation Semicond. Processes Devices*, Sep. 3–5, 2003, pp. 39–42.
[28] J. M. Jin, *The Finite Element Method in Electromagnetics*, 2nd ed. New York: Wiley, 2002, p. 442.
[29] J. Tan and G. Pan, "A new edge element analysis of dispersive waveguiding structures," *IEEE Trans. Microw. Theory Tech.*, vol. 43, no. 11, pp. 2600–2607, Nov. 1995.
[30] R. B. Lehoucq, "Analysis and implementation of an implicitly restarted arnoldi iteration," Ph.D. dissertation, Rice Univ., Houston, TX, 1995.
[31] L. T. Pillage and R. A. Rohrer, "Asymptotic waveform evaluation for timing analysis," *IEEE Trans. Computer-Aided Design*, vol. 9, no. 4, pp. 352–366, Apr. 1990.
[32] D. Jiao and J. M. Jin, , W. C. Chew, J. M. Jin, E. Michielssen, and J. M. Song, Eds., "Asymptotic waveform evaluation for broadband calculations," in *Fast and Efficient Algorithms in Computational Electromagnetics*. Norwood, MA: Artech House, 2001, ch. 15, pp. 699–727.
[33] E. K. Miller, "Model-based parameter estimation in electromagnetics: Part II–Applications to EM observables," *Appl. Computat. Electromagn. Soc. Newsletter*, vol. 11, no. 1, pp. 35–56, 1996.
[34] S. V. Polstyanko, R. Dyczij-Edlinger, and J. F. Lee, "Fast frequency sweep technique for the efficient analysis of dielectric waveguides," *IEEE Trans. Microwave Theory Tech.*, vol. 45, no. 7, pp. 1118–1126, Jul. 1997.
[35] C. J. Reddy, M. D. Deshpande, C. R. Cockrell, and F. B. Beck, "Fast RCS computation over a frequency band using method of moments in conjunction with asymptotic waveform evaluation technique," *IEEE Trans. Antennas Propagat.*, vol. 46, no. 8, pp. 1229–1233, Aug. 1998.
[36] M. J. Kobrinsky, S. Chakravarty, D. Jiao, M. C. Harmes, S. List, and M. Mazumder, "Experimental validation of crosstalk simulations for on-chip interconnects using s-parameters," *IEEE Trans. Adv. Packag.*, vol. 28, no. 1, pp. 57–62, Feb. 2005.

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