ECE 255 **ELECTRONIC ANALYSIS AND DESIGN** **Fall 2009**

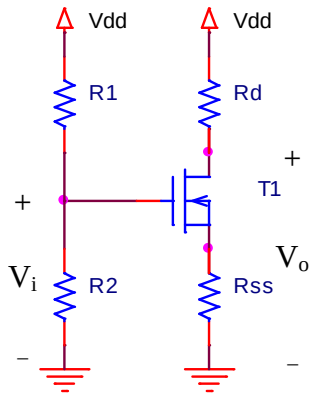
Homework 5 Due: Monday, October 26

5:00 p.m. MSEE 180 Drop Box

1) Select element values for the circuit shown to maintain $4 \le I_D \le 6$ mA for transfer functions ranging from

$$I_D = 20\left(1+\frac{V_{GS}}{4}\right)^2 \text{ mA} \quad \text{to} \quad I_D = 7.2\left(1+\frac{V_{GS}}{1.44}\right)^2 \text{ mA},$$

assuming that $V_{DD} = 16$ V.



2) Show your calculation to determine the largest value of R_D that can be used in the circuit that you biased in Problem 1 that will guarantee operation in the Beyond-Pinch-Off region.

3) Determine the maximum and minimum values of the transconductance, g_m, for the bias circuit that you designed in Problem 1.

4) For the circuit shown in Problem 1, set $R_D = 1$ kΩ and place a large capacitor, C, in parallel with R_{SS} (providing an a.c. short circuit of R_{SS}). Determine the value of both the minimum and maximum values of the magnitude of the voltage gain $|A_{Vi}| = \left|\frac{V_o}{V_i}\right|$.

5) Remove the large capacitor, C, and repeat the calculations for $|A_{Vi}|$.

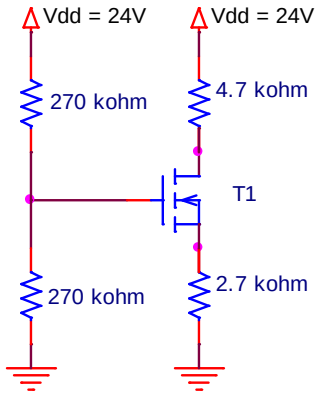
6) Design a four resistor bias circuit for a *p*-channel depletion-mode MOSFET that will ensure operation with $|I_D| = 4 \pm 0.5$ mA and $V_{SD} = 7 \pm 1$ V for transistors having $5 \le |I_{DSS}| \le 10$ mA and $3 \le V_P \le 6$ V. Assume that the larger pinch-off voltage is associated with the larger drain saturation current. The only negative supply voltage available is − 18 V.

7) Determine the maximum and minimum values of the transconductance, g_m, for the bias circuit that you designed in Problem 6.

8) For the circuit designed in Problem 6, place a large capacitor, C, in parallel with R_{SS} (providing an a.c. short circuit of R_{SS}). Determine the value of both the minimum and maximum values of the voltage gain $\left|A_{Vi}\right| = \left|\frac{V_o}{V_i}\right|$.

9) An FET in an electronic kit is to be biased as in the circuit shown below with the specified component values. The FET is characterized by $V_T = 3\ \text{V}$, $K = 9\ \text{mA}$, and a Beyond-Pinch-Off characteristic given by $I_D = K\left(\frac{V_{GS}}{V_T} - 1\right)^2$.

Find I_D and V_{DS} at the planned operating point.



10) In constructing the kit discussed in Problem 9, the upper end of the bias resistor, R_1, (the end that should be connected to V_{DD}), is mistakenly connected to the drain of the FET instead of the voltage source, V_{DD}. Find the operating point.