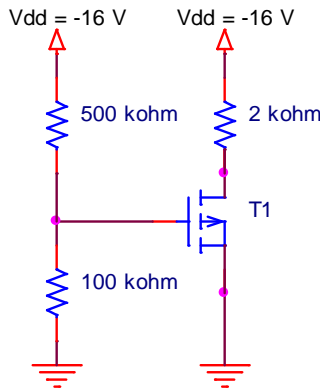
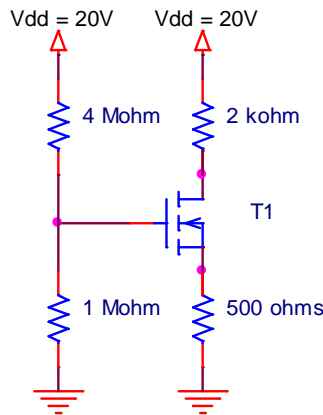


- 1) Let $V_{DD} = -16\text{ V}$ and $R_1 = 500\text{ k}\Omega$ in the bias circuit shown below. The MOSFET is described by the nonlinear relationship $I_D = -30\left(\frac{V_{GS}}{3} + 1\right)^2\text{ mA}$. Find I_D and V_{DS} .



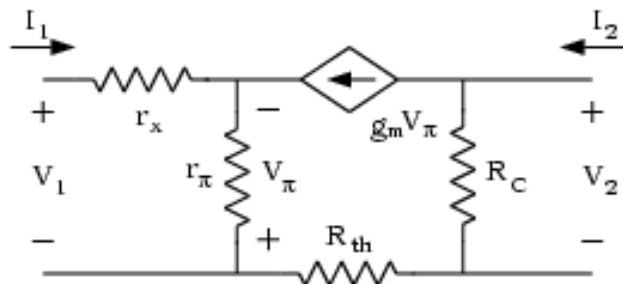
- 2) The FET shown in the figure below happens to be modeled more closely by the nonlinear trigonometric relationship $I_D = 9 - 9\cos\left[\left(\frac{\pi}{3}\right)V_{GS} - \frac{\pi}{3}\right]\text{ mA}$, than by a parabola when operating in the Beyond-Pinch-Off region. Find the operating point.



- 3) Any linear 2-port circuit can be characterized by the following pair of equations:

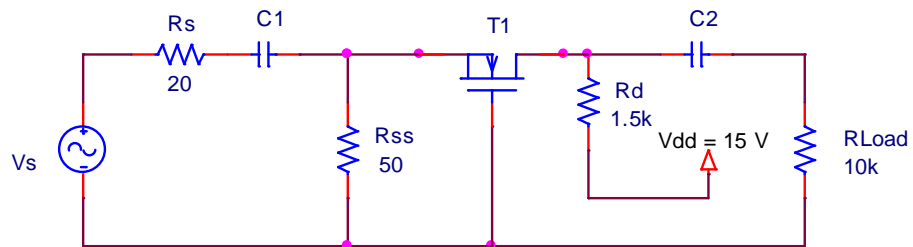
$$V_1 = h_{11} I_1 + h_{12} V_2$$

$$I_2 = h_{21} I_1 + h_{22} V_2$$



For the circuit shown above determine the h-parameter h_{11} and the h-parameter h_{12} .

- 4) A Common-Gate Amplifier, of the form shown below, uses a transistor having the characteristic $I_D = 12 \left(1 + \frac{V_{GS}}{2} \right)^2$ mA, and has the following element values: $R_{Load} = 10\text{ k}\Omega$, $R_D = 1.5\text{ k}\Omega$, $R_S = 20\text{ }\Omega$, $R_{SS} = 50\text{ }\Omega$, and $V_{DD} = 15\text{ V}$. If C_1 and C_2 are large, find Z_{in} , and Z_{out} .



The FET in this circuit is said to be self-biased since the gate bias resistors (not explicitly shown) are $R_1 = \infty$ and $R_2 = 0$.

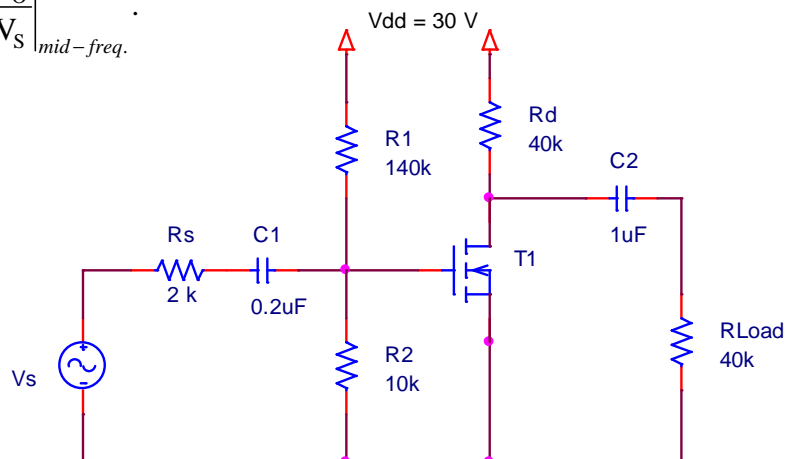
- 5) For the Common-Gate Amplifier shown in Problem 4, assuming C_1 and C_2 are large, find A_{V_i} and A_{V_s} .

- 6) Design a Common-Gate Amplifier to have a mid-frequency gain, $|A_{V_s}| = \left| \frac{V_o}{V_s} \right| \geq 20$. Use

$$R_S = 50\text{ }\Omega, R_{Load} = 5\text{ k}\Omega, I_{DSS} = 20\text{ mA}, \text{ and } V_P = -2\text{ V}.$$

- 7) The amplifier shown below employs a transistor having $V_T = 1\text{ V}$, and $I_D = 2\text{ mA}$ at $V_{GS} = 3\text{ V}$.

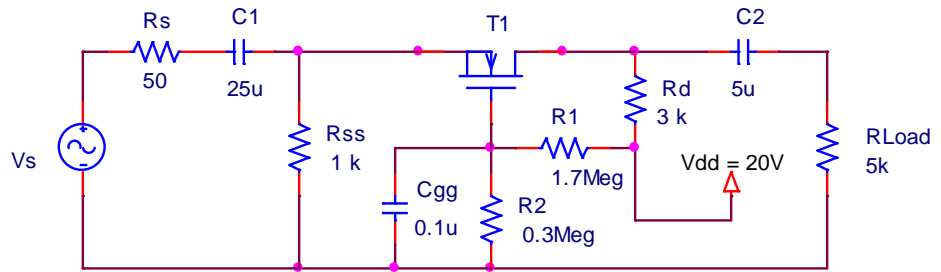
$$\text{Determine } |A_{V_s}|_{mid-freq.} = \left| \frac{V_o}{V_s} \right|_{mid-freq.}.$$



- 8) For the amplifier shown in Problem 7 determine the -3 dB point (half-power point, the point where the magnitude of the gain falls to 70.7% of the mid-frequency value) of each capacitor C_1 and C_2 acting alone (as though it were the only capacitor in the circuit).

9) For the Common-Gate Amplifier shown below, determine $\left|A_{V_s}\right|_{mid-freq.} = \left|\frac{V_o}{V_s}\right|_{mid-freq.}$.

Given that $I_{DSS} = 9 \text{ mA}$, $V_p = -3 \text{ V}$.



10) For the amplifier shown in Problem 9 determine the -3dB point (half-power point, the point where the magnitude of the gain falls to 70.7% of the mid-frequency value) of each capacitor C_1 , C_2 , and C_{gg} acting alone (as though it were the only capacitor in the circuit).