

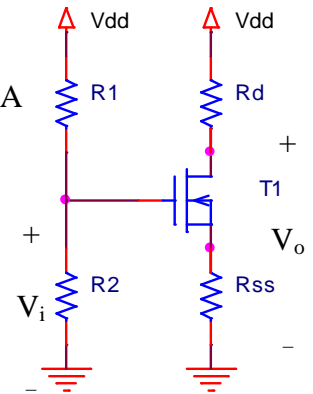
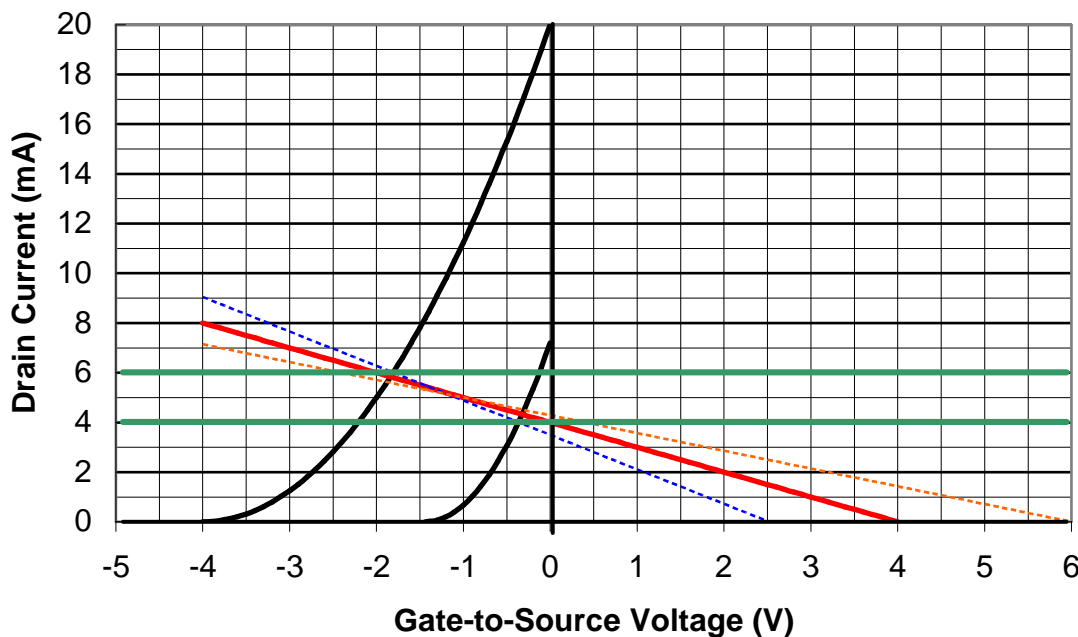
Problem 1

Select element values for the circuit shown below to maintain $4 \leq I_D \leq 6 \text{ mA}$ for

transfer functions ranging from $I_D = 20 \left(1 + \frac{V_{GS}}{4} \right)^2 \text{ mA}$ to $I_D = 7.2 \left(1 + \frac{V_{GS}}{1.44} \right)^2 \text{ mA}$

assuming that $V_{DD} = 16 \text{ V}$.

Shown below are the two limiting transfer functions.



Since the only requirement was $4 \leq I_D \leq 6 \text{ mA}$ there are many possible solutions. My first guess is represented by the solid **red line** where $V_G = 4 \text{ V}$ and $R_{SS} = 1 \text{ k}\Omega$. Another easy solution is given by the broken **orange line** which goes through the point $I_D = 5 \text{ mA}$ and $V_{GS} = -1 \text{ V}$ and has $V_G = 6 \text{ V}$.

For the orange line $R_{SS} = \frac{\Delta V_{GS}}{\Delta I_D} = \frac{7 \text{ V}}{5 \text{ mA}} = 1.4 \text{ k}\Omega$. The limiting load line, shown as the broken

blue line, can be determined from the extreme operating points which are $V_{GS} = -1.8091 \text{ V}$ @ 6 mA and $V_{GS} = -3.667 \text{ V}$ @ 4 mA . The load line running through these points has an intercept $V_G = 2.518 \text{ V}$ and slope corresponding to $R_{SS} = 721.2 \Omega$. To satisfy the design requirements, V_G and R_{SS} must be at least as large (or larger) than the limiting values.

Completing the design using the **red load line**: given that $V_{DD} = 16 \text{ V}$ we can let $R_2 = 100 \text{ k}\Omega$. Then $R_1 = 300 \text{ k}\Omega$ to provide a gate voltage of $V_G = 4 \text{ V}$. R_{SS} was already assumed to be $1 \text{ k}\Omega$. The only restriction on choosing R_D is that it can not be so large as to put the FET into the ohmic region of operation. Let $R_D = 1 \text{ k}\Omega$, then $V_{DG} \geq 6 \text{ V}$ and either transistor will be safely in the B.P.O. region.

Problem 2

Show your calculation to determine the largest value of R_D that can be used in the circuit that you biased in Problem 1 that will guarantee operation in the Beyond-Pinch-Off region.

The limiting case is determined by the operating point with the highest current (assuming that this operating point is also associated with the device with the largest $|V_P|$, which is almost always the case).

The gate-to-source voltage at the highest possible current is determined from $6 = 20 \left(1 + \frac{V_{GS}}{4} \right)^2$,

therefore, $V_{GS} = 4 \left(-1 \pm \sqrt{\frac{6}{20}} \right) \Rightarrow V_{GS} = -1.809$ or -6.191 V. Clearly the first value is correct.

For the limiting case in Problem 1 (**the blue line**) to be in the B.P.O region, $|V_{GD}| \geq |V_P|$;

consequently, $V_{DS} = V_{GS} - V_{GD} = -1.81 + 4 = 2.19$ V $= V_{DD} - I_D (R_D + R_{SS})$

and $R_D = \frac{V_{DD} - 2.19}{I_D} - R_{SS} = \frac{16 - 2.19}{6 \text{ m}} - 712.2 = 1589 \Omega$

For the design represented by the **red line**, analysis yields a maximum value of drain current, I_D ,

determined from: $I_D = 20 \left(1 + \frac{V_G - I_D R_{SS}}{4 \text{ V}} \right)^2$ mA where $V_G = 4$ V and $R_{SS} = 1$ k Ω .

expanding: $16 I_D = 20(4 + 4 - I_D)^2 \Rightarrow .8 I_D = (4 + 4 - I_D)^2 \Rightarrow I_D^2 - 16.8 I_D + 64 = 0$

$I_D = \frac{16.8 \pm \sqrt{16.8^2 - 256}}{2} = 5.84$ mA $\Rightarrow V_{GS} = V_G - I_D R_{SS} = -1.84$ V

$V_{DS} = V_{GS} - V_{GD} = -1.84 + 4 = 2.16$ V $= V_{DD} - I_D (R_D + R_{SS}) \Rightarrow R_D = 1.37$ k Ω

Problem 3

Determine the maximum and minimum values of the transconductance, g_m , for the bias circuit that you designed in Problem 1.

if $I_D = K \left(1 + \frac{V_{GS}}{-V_P} \right)^2$ mA then $g_m = \left. \frac{dI_D}{dV_{GS}} \right|_Q = \frac{2 \times K}{-V_P} \left(1 + \frac{V_{GS}}{-V_P} \right) = \frac{2 \times K}{-V_P} \sqrt{\frac{I_D}{K}}$

The range of values of g_m for the transistor with the smaller $|V_P|$ is limited by the extreme points: $[V_{GS} = -1.1068$ V @ 6 mA] and $[V_{GS} = -3.3667$ V @ 4 mA]

$g_m|_{I_D=4 \text{ mA}} = \frac{2 \times 7.2}{1.44} \sqrt{\frac{4}{7.2}} = 7.45$ mS and $g_m|_{I_D=6 \text{ mA}} = \frac{2 \times 7.2}{1.44} \sqrt{\frac{6}{7.2}} = 9.13$ mS

The range of values of g_m for the transistor with the larger $|V_P|$ is limited by the extreme points: $[V_{GS} = -1.8091$ V @ 6 mA] and $[V_{GS} = -2.2111$ V @ 4 mA]

$g_m|_{I_D=4 \text{ mA}} = \frac{2 \times 20}{4} \sqrt{\frac{4}{20}} = 4.47$ mS and $g_m|_{I_D=6 \text{ mA}} = \frac{2 \times 20}{4} \sqrt{\frac{6}{20}} = 5.48$ mS

Your values will depend on your design but will fall in the ranges

$4.47 \text{ mS} < g_{m(\text{min})} < 5.48 \text{ mS}$ and $7.45 \text{ mS} < g_{m(\text{max})} < 9.13 \text{ mS}$

Problem 4

For the circuit shown in Problem 1, set $R_D = 1 \text{ k}\Omega$ and place a large capacitor, C , in parallel with R_{SS} (providing an a.c. short circuit of R_{SS}). Determine the value of both the minimum and maximum

values of the voltage gain $|A_{Vi}| = \left| \frac{V_o}{V_i} \right|$.

Since $|A_{Vi}| = \left| \frac{V_o}{V_i} \right| = g_m R_D$ the exact values will depend on your design values of g_m , but will be in

the ranges $4.47 < |A_{Vi(\min)}| < 5.48$ and $7.45 < |A_{Vi(\max)}| < 9.13$

Problem 5

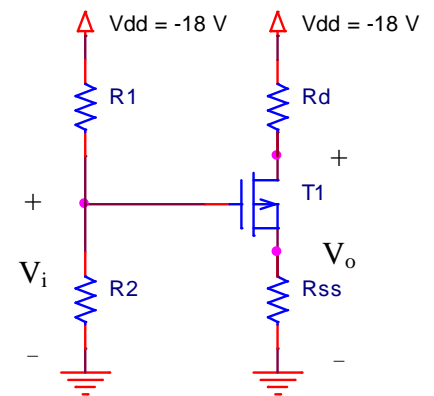
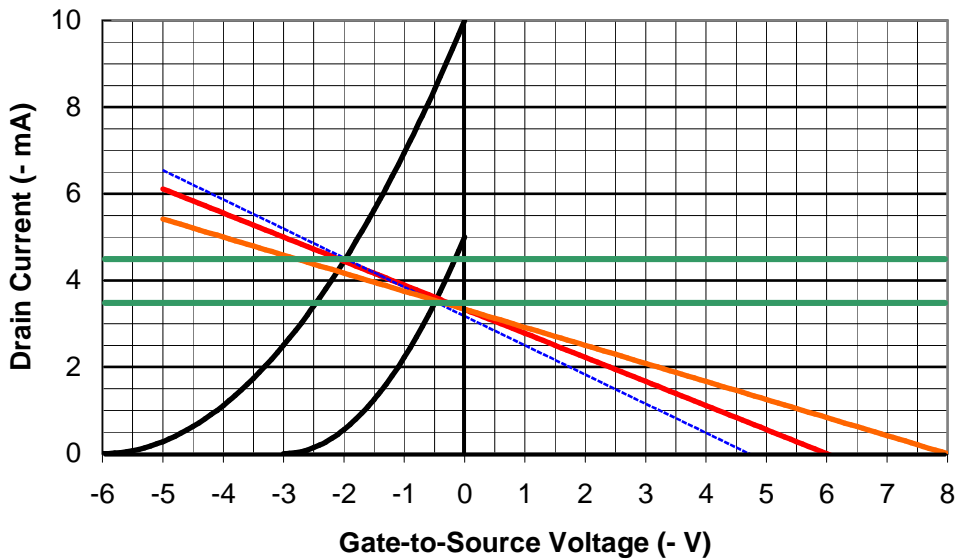
Remove the large capacitor, C , and repeat the calculations for $|A_{Vi}|$.

In this case $|A_{Vi}| = \left| \frac{V_o}{V_i} \right| = \frac{g_m R_D}{1 + g_m R_{SS}}$ the exact values will depend on your design values of g_m and selection of R_{SS} .

Problem 6

Design a four resistor bias circuit for a p -channel depletion-mode MOSFET that will ensure operation with $|I_D| = 4 \pm 0.5 \text{ mA}$ and $V_{SD} = 7 \pm 1 \text{ V}$ for transistors having $5 \leq |I_{DSS}| \leq 10 \text{ mA}$ and $3 \leq V_p \leq 6 \text{ V}$. Assume that the larger pinch-off voltage is associated with the larger drain saturation current. The only negative supply voltage available is -18 V .

Shown below are the two limiting transfer functions.



We can determine extreme operating points for each of the limiting characteristics and find the minimum acceptable value of R_{SS} or just make a quick sketch and guess appropriate values for V_G and R_{SS} – either way, the important step is verifying the final design.

For the transistor with the larger I_{DSS} we have $I_D = \frac{I_{DSS}}{V_P^2} (V_{GS} - V_P)^2 = -4.5 = \frac{-10}{6^2} (V_{GS} - 6)^2$

$$\text{Therefore } V_{GS} = 6 \left(1 \pm \sqrt{\frac{4.5}{10}} \right) V = 6(1 \pm 0.6708) V \Rightarrow V_{GS} = 1.9751 V$$

For the transistor with the smaller I_{DSS} we have $I_D = \frac{I_{DSS}}{V_P^2} (V_{GS} - V_P)^2 = -3.5 = \frac{-5}{3^2} (V_{GS} - 3)^2$

$$\text{Therefore } V_{GS} = 3 \left(1 \pm \sqrt{\frac{3.5}{5}} \right) V = 3(1 \pm 0.8367) V \Rightarrow V_{GS} = 0.490 V$$

The minimum value for the source resistor and gate voltage are then found to be:

$$R_{SS}(\text{min}) = \frac{\Delta V_{GS}}{\Delta I_D} = \frac{(1.9751 - 0.490) V}{(4.5 - 3.5) \text{ mA}} = 1.4851 \text{ k}\Omega$$

and $V_G(\text{min}) = 0.490 V - (1.4851 \text{ k}\Omega)(3.5 \text{ mA}) = -4.708 V$

The limiting load-line is shown as a broken **blue line** in the plot above.

First try: Let $V_G = -6 V$ and $R_{SS} = 1.8 \text{ k}\Omega$ as shown by the **red line** in the plot above. This load-line satisfies the condition $|I_D| = 4 \pm 0.5 \text{ mA}$, but does it work with the condition on V_{SD} ?

To find the operating points we solve $I_D = \frac{I_{DSS}}{V_P^2} (V_{GS} - V_P)^2 = \frac{I_{DSS}}{V_P^2} [(V_G - R_{SS}I_D) - V_P]^2$ for I_D using the Quadratic Formula.

For the device with the smaller I_{DSS} , the operating point is $I_D = -3.588 \text{ mA}$.

We want to have $V_{SD} = 8 V$ (its maximum value) when the smaller current is flowing.

$$\text{Therefore, } R_D = \frac{18 - 8}{3.588} - 1.8 = 2.787 - 1.8 = .987 \text{ k}\Omega$$

For the device with the larger I_{DSS} , the operating point is $I_D = -4.444 \text{ mA}$

$$\text{At this operating point } V_{SD} = 18 - (1.8 + .987)4.444 = 18 - 2.787(4.444) = 5.615 V \quad \text{oops}$$

We are below the lower limit for V_{SD} .

Let's try again – this time reducing the range of drain current.

Let $V_G = -8 V$ and $R_{SS} = 2.4 \text{ k}\Omega$ as shown by the **orange line** in the plot above.

For the device with the smaller I_{DSS} , the operating point is $I_D = -3.533 \text{ mA}$.

We want to have $V_{SD} \leq 8 V$ when the smaller current is flowing.

$$\text{Therefore, } R_D = \frac{18 - 8}{3.533} - 2.4 = 2.831 - 2.4 = .431 \text{ k}\Omega$$

For the device with the larger I_{DSS} , the operating point is $I_D = -4.211 \text{ mA}$

$$\text{At this operating point } V_{SD} = 18 - (2.4 + .431)4.211 = 18 - 2.831(4.211) = 6.079 V \quad \text{OK – but close}$$

Finish by selecting R_1 and R_2 . Let $R_2 = 100 \text{ k}\Omega$, then $V_G = -8 = \frac{100}{100 + R_2}(-18) \Rightarrow R_2 = 125 \text{ k}\Omega$

Problem 7

Determine the maximum and minimum values of the transconductance, g_m , for the bias circuit that you designed in Problem 6.

$$\text{if } I_D = \frac{I_{DSS}}{V_P^2} (V_{GS} - V_P)^2 \text{ mA} \quad \text{then} \quad g_m = \left. \frac{dI_D}{dV_{GS}} \right|_Q = \frac{2 \times I_{DSS}}{V_P^2} (V_{GS} - V_P) = \frac{2 \times I_{DSS}}{V_P} \left(-\sqrt{\frac{I_D}{I_{DSS}}} \right)$$

The range of values of g_m for the transistor with the smaller $|V_P|$ is limited by the extreme points: $[V_{GS} = .154 \text{ V @ } -4.5 \text{ mA}]$ and $[V_{GS} = .490 \text{ V @ } -3.5 \text{ mA}]$

$$g_m|_{I_D=-3.5\text{mA}} = \frac{2 \times 5}{3} \sqrt{\frac{3.5}{5}} = 2.79 \text{ mS} \quad \text{and} \quad g_m|_{I_D=-4.5\text{mA}} = \frac{2 \times 5}{3} \sqrt{\frac{4.5}{5}} = 3.16 \text{ mS}$$

The range of values of g_m for the transistor with the larger $|V_P|$ is limited by the extreme points: $[V_{GS} = 1.975 \text{ V @ } -4.5 \text{ mA}]$ and $[V_{GS} = 2.450 \text{ V @ } -3.5 \text{ mA}]$

$$g_m|_{I_D=-3.5\text{mA}} = \frac{2 \times 10}{6} \sqrt{\frac{3.5}{10}} = 1.97 \text{ mS} \quad \text{and} \quad g_m|_{I_D=-4.5\text{mA}} = \frac{2 \times 10}{6} \sqrt{\frac{4.5}{10}} = 2.24 \text{ mS}$$

Your values will depend on your design but will fall in the ranges

$$1.97 \text{ mS} < g_{m(\text{min})} < 2.24 \text{ mS} \quad \text{and} \quad 2.79 \text{ mS} < g_{m(\text{max})} < 3.16 \text{ mS}$$

Problem 8

For the circuit designed in Problem 6, place a large capacitor, C , in parallel with R_{SS} (providing an a.c. short circuit of R_{SS}). Determine the value of both the minimum and maximum values of the voltage gain

$$|A_{Vi}| = \left| \frac{V_o}{V_i} \right|$$

Since $|A_{Vi}| = \left| \frac{V_o}{V_i} \right| = g_m R_D$ the exact values will depend on your design values of g_m and R_D .

$$\text{Using } R_D = .43 \text{ k}\Omega \quad .85 < |A_{Vi(\text{min})}| < .96 \quad \text{and} \quad 1.12 < |A_{Vi(\text{max})}| < 1.36$$

{Not a great amplifier!}

Problem 9

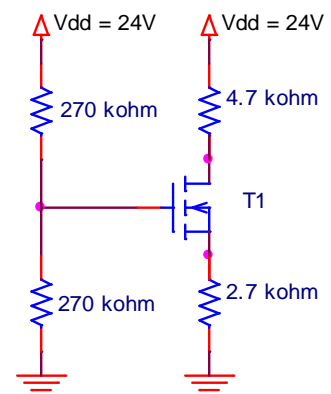
An FET in an electronic kit is to be biased as in the circuit shown below with the specified component values. The FET is characterized by $V_T = 3 \text{ V}$, $K = 9 \text{ mA}$, and a Beyond-Pinch-Off

$$\text{characteristic given by } I_D = K \left(\frac{V_{GS}}{V_T} - 1 \right)^2$$

Find I_D and V_{DS} at the planned operating point.

$$V_G = \frac{270}{270+270} 24 = 12 \text{ V} \quad \text{and} \quad I_D = K \left[\frac{(V_G - R_{SS} I_D)}{V_T} - 1 \right]^2$$

$$I_D = 2.72 \text{ mA}, \quad V_{GS} = 4.66 \text{ V}, \quad \text{and} \quad V_{DS} = 3.87 \text{ V}$$



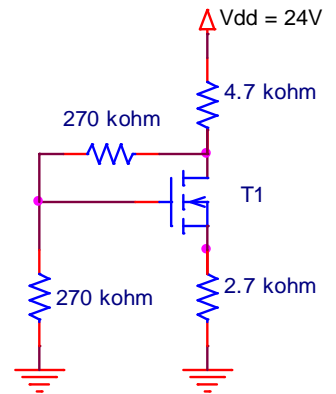
Problem 10

In constructing the kit discussed in Problem 9, the upper end of the bias resistor, R_1 , (the end that should be connected to V_{DD}), is mistakenly connected to the drain of the FET instead of the voltage source, V_{DD} . Find the operating point.

Where to start?
$$I_D = K \left(\frac{V_{GS}}{V_T} - 1 \right)^2 \quad V_G = \frac{R_2}{R_1 + R_2} V_D$$

$$V_{GS} = V_G - R_{SS} I_D \quad V_D = V_{DD} - R_D \left(I_D + \frac{V_D}{R_1 + R_2} \right)$$

Well, we now have four equations in four unknowns, I_D , V_D , V_G , and V_{GS} .



Let's make it a bit easier. We know the bias current must be small compared to I_D .

So, $V_D \approx V_{DD} - R_D I_D$ and $V_G = \frac{V_{DD} - R_D I_D}{2}$ and $V_{GS} = \frac{V_{DD} - R_D I_D}{2} - R_{SS} I_D$

or $V_{GS} = \frac{V_{DD} - (R_D + 2R_{SS}) I_D}{2}$

$$I_D = K \left(\frac{V_{DD} - (R_D + 2R_{SS}) I_D}{2V_T} - 1 \right)^2 = 9 \left(\frac{24 - 10.1 I_D}{6} - 1 \right)^2$$

$$(10.1)^2 I_D^2 - (2 \times 18 \times 10.1 + 4) I_D + 18^2 = 0 \Rightarrow I_D = 1.537 \text{ mA}, V_{GS} = 4.240 \text{ V}, \text{ and } V_{DS} = 12.63 \text{ V}.$$

{ Without neglecting the bias current: $I_D = 1.523 \text{ mA}$, $V_{GS} = 4.234 \text{ V}$, and $V_{DS} = 12.58 \text{ V}$. }