

Design of a Precision Gain Amplifier

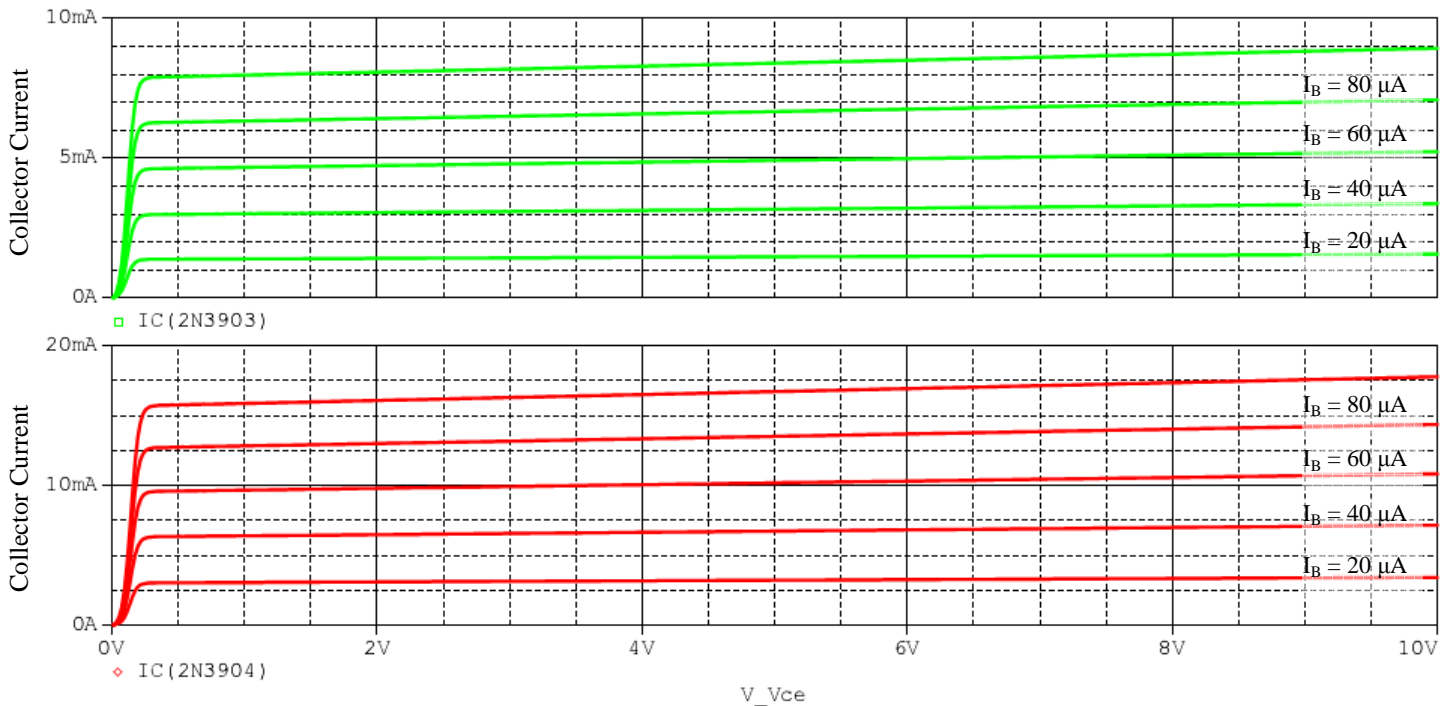
(Pre-lab for ECE 208 Experiment #5)

This exercise will use the PSpice models for Q2N3903 and Q2N3904 *nnp* bipolar junction transistors. The model parameters from Cadence PSpice are given below.

```
.model Q2N3903 NPN(Is=6.734f Xti=3 Eg=1.11 Vaf=74.03 Bf=335.2 Ne=1.208
+ Ise=6.734f Ikf=60.26m Xtb=1.5 Br=.8073 Nc=2 Isc=0 Ikr=0 Rc=1
+ Cjc=3.638p Mjc=.3085 Vjc=.75 Fc=.5 Cje=4.493p Mje=.2593 Vje=.75
+ Tr=243.9n Tf=300.8p Itf=.4 Vtf=4 Xtf=2 Rb=10)
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.model Q2N3904 NPN(Is=6.734f Xti=3 Eg=1.11 Vaf=74.03 Bf=416.4 Ne=1.259
+ Ise=6.734f Ikf=66.78m Xtb=1.5 Br=.7371 Nc=2 Isc=0 Ikr=0 Rc=1
+ Cjc=3.638p Mjc=.3085 Vjc=.75 Fc=.5 Cje=4.493p Mje=.2593 Vje=.75
+ Tr=239.5n Tf=301.2p Itf=.4 Vtf=4 Xtf=2 Rb=10)
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- To verify that your models are correct, plot the output characteristics for $I_B = 20, 40, 60, 80,$ and $100 \mu\text{A}$ for $0 \leq V_{CE} \leq 10 \text{ V}$ for both *nnp* bipolar junction transistors to obtain the plots shown below on a single page. Include these plots in your report.



The objective is to design a single-transistor amplifier that will meet the following specifications whether a 2N3903 or 2N3904 transistor is used in the circuit.

Specifications

Voltage gain: $|A_{V_s}| = \left| \frac{V_{out}}{V_{source}} \right| = 10 \pm 0.5$

Input impedance: $Z_{in} > 10 \text{ k}\Omega$ (at mid-frequencies) Output impedance: $Z_{out} \approx 2.2 \text{ k}\Omega$

Output voltage swing: $v_{out}(\text{min}) = 2 V_{PP}$

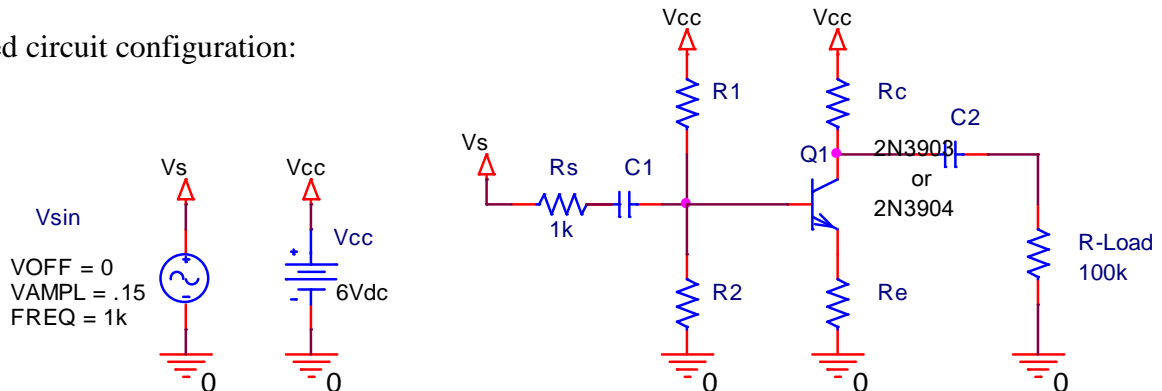
We would actually like to have an output voltage swing of $3 V_{PP}$ without distortion.

Minimum 3 dB Bandwidth: 30 Hz to 100 kHz

Constraints

Power supply:	$V_{CC} = 6\text{ V}$
Source resistance:	$R_S = 1\text{ k}\Omega$
Load resistance:	$R_{Load} = 100\text{ k}\Omega$
Capacitor restriction:	Maximum of three external capacitors having total capacitance $\leq 100\text{ }\mu\text{F}$ and chosen from the list of standard values given on page 1166 of the text.
Resistor restriction:	Use nominal 5% values for all resistors (series and parallel combinations are not permitted), see table of standard values on page 1164 of the text.

Suggested circuit configuration:



NOTE: See sections 13.1, 13.2, and 13.5 of the text for information on transistor amplifiers and sections 13.6 and 13.7 for a detailed discussion of this circuit configuration.

A WORD TO THE WISE: Spend a few moments trying to achieve a clear view of your objectives, recognize all of the important obstacles, and formulate a coherent plan for obtaining your objective. In particular, take note of the data sheet on the last page. Among the items of special interest are the values of h_{FE} which span the range from 35 (min for 2N3903 @ 1 mA) to 270 (max for 2N3904 @ 1mA) and the range of V_{BE} .

2. Preliminary design (neatly handwritten)

- Draw a schematic of the circuit that you intend to use (whether or not it is identical to the one above) in the space provided on the cover sheet (attached).
 - Label all components with the labels (designations) that you will use in your hand calculations.
- * (c) Select an operating point and provide a clear, concise, and compelling explanation of how and why you selected that particular operating point on the cover sheet. Note that trial and error, it seemed like a good idea at the time, Joe told me it might work, etc. do not qualify as satisfactory explanations.
- Show complete hand calculations to justify the values of R_1 , R_2 , R_E , R_C , and any other components that affect the operating point. List the final results of your hand calculations (i.e., the final component values, which must also be real 5% values) on the cover page.

3. Simulation of preliminary design

- Create a simulation schematic of your circuit using a 2N3903 and a second, identical, schematic of your circuit using a 2N3904 and run an operating point simulation on both (either simultaneously or sequentially).
- Enable the bias voltage display and the bias current display so that the all bias point information is displayed on your schematics. Move the bias point display boxes, if necessary, to ensure that

they do not overlap or conceal any component designations. Include these schematics, which also display the bias point information, in your report.

- * (c) Provide a written comment on the cover sheet regarding the success (or failure) of your preliminary bias point calculations. If your simulation agrees with your calculations, a simple statement to that effect is sufficient. If your simulation does not produce the predicted operating point, identify the weakness in your analysis and modify your analysis.
- (d) If and only if your preliminary design did not achieve the operating point you predicted, repeat item 3b and include the new calculations in your report.

4. Selection of external (coupling) capacitors (neatly handwritten)

- * (a) Calculate and include in your report, your calculations for the value of each external capacitor that will cause the -3dB point (the point where the gain will fall to 70.7% of its mid-frequency value) due to each capacitor to be at 30 Hz.
- (b) Select capacitor values (in accord with the capacitor restrictions) that will be used in your final amplifier design to ensure that $f_L < 30$ Hz and record these values on the cover page.

5. A.C. simulation of the complete amplifier

- (a) Create a simulation schematic of your circuit using a 2N3903 and a second, identical schematic of your circuit using a 2N3904; including the external capacitors calculated in part 4, and an ac signal source (VAC) of amplitude 1 mV (in place of V_{sin} in the figure above). Perform an ac simulation on both circuits (either simultaneously or sequentially) over the range of at least 10 Hz to 1 MHz to show that both the gain and frequency response requirements are satisfied by both circuits. Include the plot(s) showing the performance of both amplifiers in your report.
- (b) Using the circuits simulated in 5a, plot the input impedance for both circuits over the frequency range of at least 10 Hz to 1 MHz to show that the input impedance specifications are satisfied. Include these plots in your report.

6. Transient simulation of the complete amplifier

- (a) Using the same circuits used in part 5, and replacing the ac signal source (VAC) with a sinusoidal source (VSIN) having an amplitude of 0.2 V and frequency of 1 kHz, perform a transient simulation of both circuits and produce plots of the output voltage as a function of time for the time interval 0 to 10 ms.
- (b) Using the cursor, mark a peak (maximum value) and trough (minimum value) on each of the two waveforms of item 6a. These points must be marked using the cursor, not handwritten. Include these plots in your report.
- (c) Using the values marked by the cursor on the plots of item 6b, calculate the peak-to-peak voltage of each waveform and determine the gain and record these results on the cover page.
- (d) Provide the complete Spice output file corresponding to the schematics used for Part 6 (the transient response simulation).
(You may remove page breaks, blank lines, and reduce font size to no smaller than 8 points if you wish to conserve paper; however, do not alter any text in the output file.)

* Pay special attention to these items.

** Save a copy of your report and hand calculations for use in your ECE 208 Formal Lab Report.

Minimum report requirements:

- 1) Completed cover page showing preliminary design results (cover page is provided below), including:
 - a) Hand-drawn schematic with all components identified with the designation used in your preliminary design calculations.
 - b) The operating point that you intend to achieve.
 - c) A clear, concise, and compelling explanation of how and why you selected that particular operating point.
 - d) Values calculated in your preliminary design of all resistive elements used to establish the chosen operating point (single 5% resistor values only).
 - e) Comments on the success (or failure) of your preliminary bias point calculations.
 - f) Values of the resistors used in your final design (even if identical to the original design).
 - g) Standard values for the external capacitors you determined to ensure $f_L < 30$ Hz.
 - h) Values of the voltage gain $|A_{Vs}|$ calculated from the transient simulation.
- 2) Neatly prepared hand calculation of the component values required to achieve your operating point.
- 3) Neatly prepared hand calculation of the capacitor values required to ensure $f_L < 30$ Hz.
- 4) One single page produced directly from the PROBE display (using “Add Plot”) showing the output characteristics of the two transistors from Part 1.
Be sure that the traces are clearly visible and that you retain the trace definitions that the Probe program generates and displays below the plots.
- 5) PSpice simulation schematic displaying the bias point voltages and currents for both transistors.
- 6) Output plots showing the A.C. frequency response for both transistors (10 Hz to 1 MHz).
- 7) Output plots showing the input impedance of your amplifier for both transistors (10 Hz to 1 MHz).
- 8) Output plots showing the transient response of your amplifiers to a 200 mV, 1 kHz sine wave, including the cursor marked peak and trough of each output waveform.
- 9) The complete Spice output file corresponding to the schematic used for Part 6 (the transient response simulation).
(You may remove page breaks, blank lines, and reduce font size to no smaller than 8 points if you wish to conserve paper; however, do not alter any text in the output file)

Although you are encouraged to work with your classmates, each student is required to create their own simulation and produce their own plots and other results from their own unique simulations. Potential sanctions are provided on the course website.

Name _____

ECE 255
Fall 2009

ELECTRONIC ANALYSIS AND DESIGN
PSpice Design 2– Preliminary and Final Design Results

Hand-drawn schematic:

Intended operating point for preliminary design: $I_C =$ _____, $V_{CE} =$ _____

Explanation of why this operating point was chosen:

Component values from preliminary design:

$R_C =$ _____, $R_E =$ _____, $R_1 =$ _____, $R_2 =$ _____, () = _____

Comments on the success (or failure) of your preliminary bias point calculations.

Whether or not redesign was required, list the final values used in your simulation:

$R_C =$ _____, $R_E =$ _____, $R_1 =$ _____, $R_2 =$ _____, () = _____

Component values for external capacitors used:

$C_1 =$ _____, $C_2 =$ _____, () = _____

Final mid-frequency voltage gain $|A_{Vs}|$

2N3903 _____ 2N3904 _____

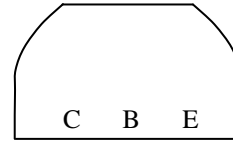
DATA SHEET FOR 2N3903 AND 2N3904

NPN Silicon General Purpose Switching and Amplifier Transistors

-----ABSOLUTE MAXIMUM RATINGS -----

at 25° C Free-Air Temperature (unless noted)

Collector-Base Voltage	60 V
Collector-Emitter Voltage (Base open)	40 V
Emitter-Base Voltage	6 V
Total Dissipation (25 C Free-Air) See Note 1	360 mW
Collector Current	200 mA
Junction Temperature (Operating)	+150 C
Lead Temperature 1/6 inch from case for 10 sec	+260 C
Storage Temperature Range	-55 C to +150 C



BOTTOM VIEW

ELECTRICAL CHARACTERISTICS at T_{air} = 25 C (unless otherwise noted)

Parameter	Symbol	Test Conditions	2N3903		2N3904		Unit
			Min	Max	Min	Max	
Collector-Base Breakdown Voltage	V _{CBO} (BR)	I _C = 10 μA, I _E = 0	60	–	60	–	V
Collector-Emitter Breakdown Voltage	V _{CEO} (BR)	I _C = 1 mA, I _B = 0 (Note 2)	60	–	60	–	V
Emitter-Base Breakdown Voltage	V _{EBO} (BR)	I _E = 10 μA, I _C = 0	6	–	6	–	V
Collector Cutoff Current	I _{CO}	V _{CE} = 30 V, V _{BE} = -3 V	–	50	–	50	nA
Base Cutoff Current	I _{BO}	V _{CE} = 30 V, V _{BE} = -3 V	–	50	–	50	nA
Static Forward Current Transfer Ratio	h _{FE}	V _{CE} = 1 V, I _C = 100 μA	20	–	40	–	–
		V _{CE} = 1 V, I _C = 1 mA	35	–	70	270	–
		V _{CE} = 1 V, I _C = 10 mA (Note 2)	50	150	100	300	–
		V _{CE} = 1 V, I _C = 50 mA (Note 2)	30	–	60	–	–
		V _{CE} = 1 V, I _C = 100 mA (Note 2)	15	–	30	–	–
Collector-Emitter Saturation Voltage	V _{CE} (SAT)	I _C = 10 mA, I _B = 1 mA (Note 2)	–	0.2	–	0.2	V
		I _C = 50 mA, I _B = 5 mA (Note 2)	–	0.2	–	0.2	V
Base-Emitter Saturation Voltage	V _{BE} (SAT)	I _C = 10 mA, I _B = 1 mA (Note 2)	0.65	0.85	0.65	0.85	V
		I _C = 50 mA, I _B = 5 mA (Note 2)	–	0.95	–	0.95	V
Small Signal Parameters							
Small Signal Current Gain	h _{fe}	V _{CE} = 10 V, I _C = 1 mA, f = 1 kHz	50	200	60	230	–
		V _{CE} = 20 V, I _C = 10 mA, f = 100 MHz	–	2.5	–	3.0	–
Voltage Feedback Ratio	h _{re}	V _{CE} = 10 V, I _C = 1 mA, f = 1 kHz	0.1	5	0.5	8.0	x10 ⁻⁴
Input Resistance	h _{ie}	V _{CE} = 10 V, I _C = 1 mA, f = 1 kHz	0.5	8	1.0	10	kΩ
Output Admittance	h _{oe}	V _{CE} = 10 V, I _C = 1 mA, f = 1 kHz	1.0	40	1.0	40	μhos
Output Capacitance	C _{ob}	V _{CB} = 5.0 V, I _E = 0, f = 1 MHz	–	4.0	–	4.0	pF
Input Capacitance	C _{ib}	V _{EB} = 0.5 V, I _C = 0, f = 1 MHz	–	8.0	–	8.0	pF
Cutoff Frequency	f _T	V _{CE} = 20 V, I _C = 10 mA, f = 100 MHz	–	250	–	300	MHz