

Design of a Common Source Amplifier
(Pre-lab for ECE 208 Experiment X)

This exercise will use the PSpice model for the J2N3819 *n*-channel junction field effect transistor. The model parameters for a J2N3819 (from Cadence PSpice) are given below.

```
.model J2N3819 NJF(Beta=1.304m Betatce=-.5 Rd=1 Rs=1 Lambda=2.25m Vto=-3
+ Vtotc=-2.5m Is=33.57f Isr=322.4f N=1 Nr=2 Xti=3 Alpha=311.7u
+ Vk=243.6 Cgd=1.6p M=.3622 Pb=1 Fc=.5 Cgs=2.414p Kf=9.882E-18
+ Af=1)
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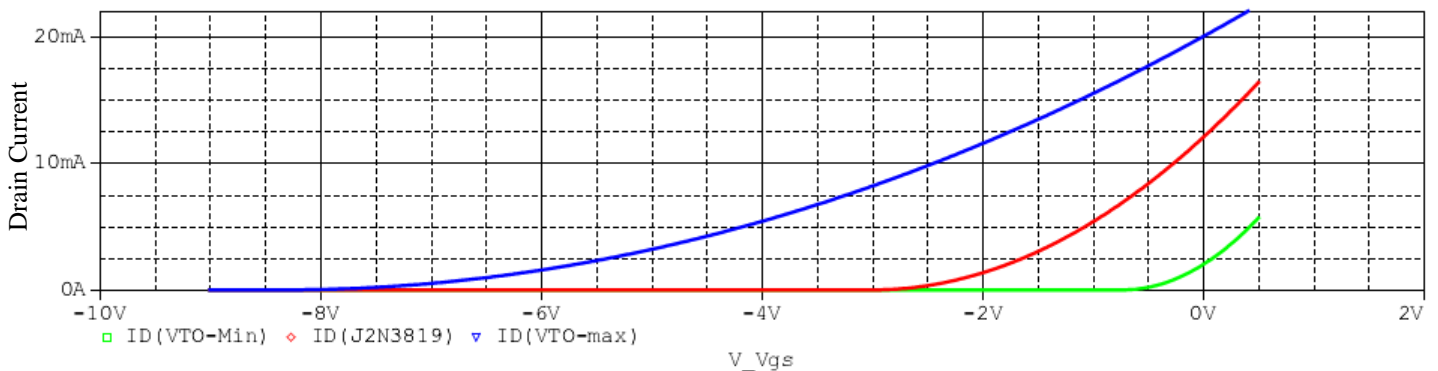
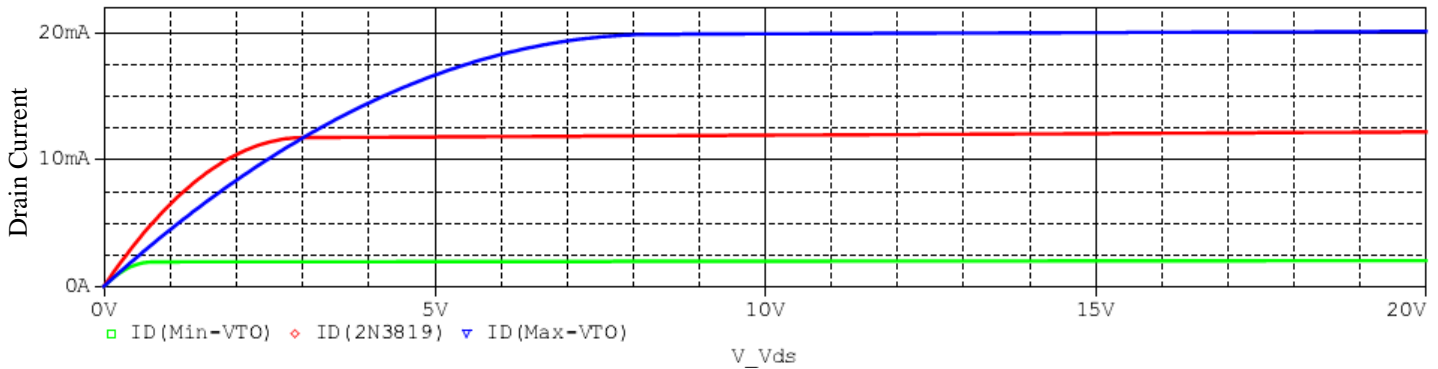
In addition to the build-in model, you will be using two additional JFET models that you will create to match the maximum and minimum device characteristics given on the 2N3819 data sheet which is attached. Specifically, you will determine the values for Beta and VTO appropriate for the Min and Max values of the Drain-to-Source Saturation Current, I_{DSS} , and Gate-to-Source Voltage, V_{GS} .

The equation governing operation in the Beyond-Pinch-Off region is: $I_D = \beta(V_{GS} - V_{TO})^2 (1 + \lambda V_{DS})$

- Determine values for Beta and VTO appropriate to complete the following table and list those values (accurate to four significant digits) on the cover page (attached) of your report.

	I_{DSS} $V_{DS} = 15\text{ V}$	V_{GS} @ $I_D = 200\ \mu\text{A}$ $V_{DS} = 15\text{ V}$	Lambda	Beta	VTO
Min $ V_P $	2.0 mA	-0.5 V	0.003 V^{-1}		
Max $ V_P $	20 mA	-7.5 V	0.001 V^{-1}		

- Using the Jbreak elements create two models (one for Min $|V_P|$ and the other for Max $|V_P|$) using the three PSpice parameters from the table above. To verify that your models are correct, plot the output characteristics for $V_{GS} = 0$ and transfer characteristics for each of the three models to obtain the plots shown below. Include these plots in your report.



The objective is to design a single-transistor amplifier that will meet the following specifications whether the 2N3819 transistor or either of the two extreme case models are used in the circuit.

Specifications

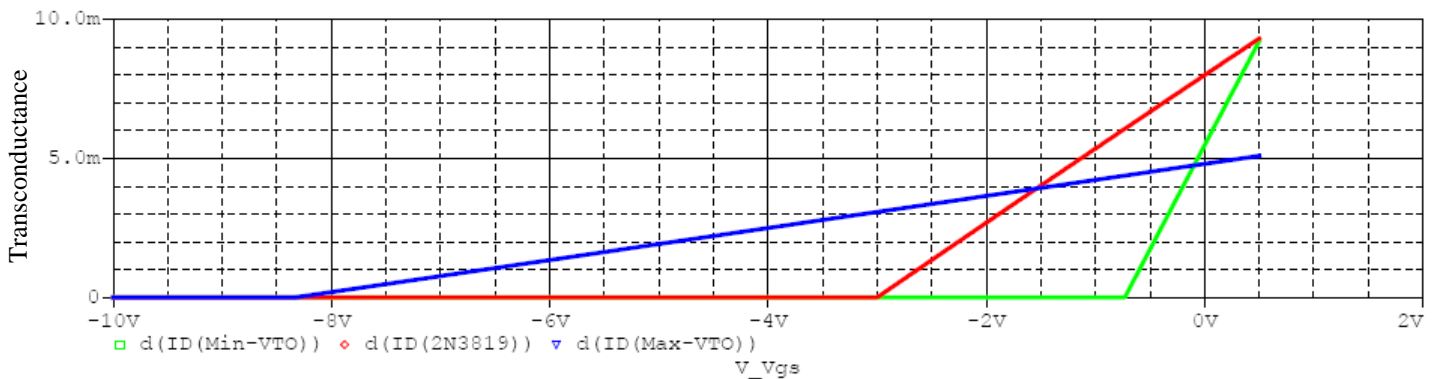
- Voltage gain: $|A_{V_s}| = \left| \frac{V_{out}}{V_{source}} \right| > 10$
- Input impedance: $Z_{in} > 100 \text{ k}\Omega$ (at mid-frequencies)
- Output impedance: $Z_{out} < 10 \text{ k}\Omega$
- Output voltage swing: $v_{out}(\text{min}) = 2 V_{pp} (\pm 1 \text{ V})$
- Bias current: $I_D > 0.4 \text{ mA}$ at quiescent point (Q -point) to enhance linearity
- Minimum 3 dB Bandwidth: 10 Hz to 100 kHz

Constraints

- Power supply: $V_{DD} = 25 \text{ V}$
- Source resistance: $R_S = 1 \text{ k}\Omega$
- Load resistance: $R_{Load} = 100 \text{ k}\Omega$
- Capacitor restriction: Maximum of three external capacitors having total capacitance $\leq 100 \mu\text{F}$ and chosen from the list of standard values given on page 1166 of the text.
- Resistor restriction: Use nominal 5% values for all resistors (series and parallel combinations are not permitted), see table of standard values on page 1164 of the text.

Before you begin the design, there is one other critical parameter of the JFET's that needs to be considered – the transconductance, g_m .

- Determine the transconductance for each of the three JFET's to be used in the amplifier design and produce a plot similar to the one shown below. Include a plot of transconductance in your report, either as a separate plot or together with the load line plots discussed in connection with the preliminary design in Part 5d.

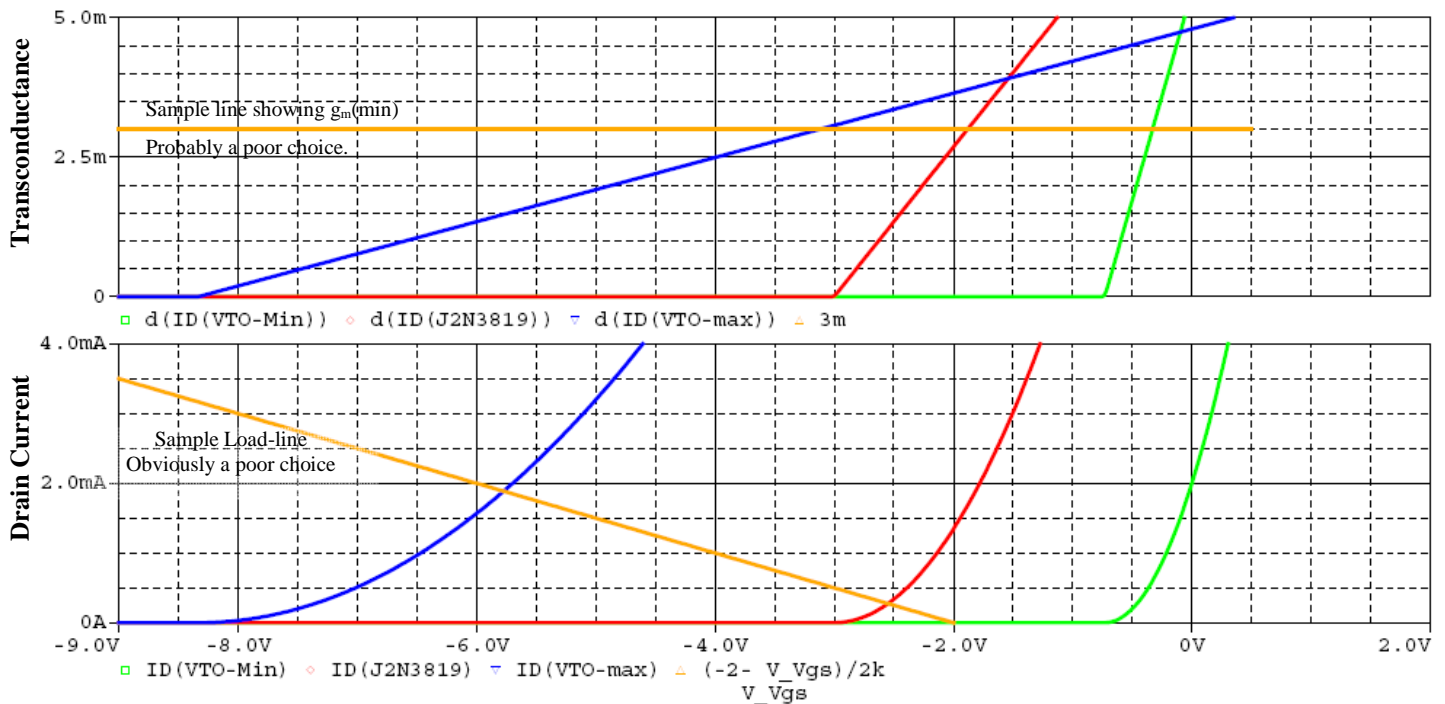


To achieve the required input impedance and required voltage gain using a single JFET, we must choose an amplifier having a common-source configuration. From the previous PSpice exercise using a BJT, we know that there are three possible implementations of this type of amplifier which differ only in the treatment of the FET-source resistor, R_{SS} . The options are: 1) an FET-source resistor without a shunt (by-pass) capacitor, 2) an FET-source resistor with a shunt capacitor, and 3) two FET-source resistors in series with one having a shunt capacitor.

4. Determine which of the three options would be best for this design and provide a brief explanation of your choice in your report and on the cover page.

Selection of an operating point

You may find it helpful to create a plot similar to the one shown below for use during your preliminary design. In this plot the transconductance, g_m , and the drain current, I_D , versus gate-to-source voltage, V_{GS} , are shown in the same window. This allows one to use the cursor to associate particular values of g_m with the corresponding value of I_D .



5. Preliminary design (neatly handwritten)

- (a) Draw a schematic of the circuit that you intend to use on the cover page.
- (b) Label all components in your schematic (drawn on the cover page) with the labels that you will use in your hand calculations.

- * (c) Select a value for the drain resistor, R_D , and associated minimum value of g_m . Provide a clear, concise, and compelling explanation of how and why you selected that particular value of R_D and $g_m(\min)$. Note that trial and error, it seemed like a good idea at the time, Joe told me it might work, etc. do not qualify as satisfactory explanations.
- (d) Plot the minimum value of g_m for your preliminary design on the transconductance plot using “Add Trace” in the same PSpice Probe window that displays the plot of I_D vs. V_{GS} . Plot the load-line that you intend to use to set the operating points for the three JFET’s on the plot of I_D vs. V_{GS} , using “Add Trace” in that same Probe window, and include that plot (similar to the one above) in your report. You may include this transconductance plot with the load-line plot in place of the transconductance plot required for Part 3.

- (e) Show complete hand calculations of R_1 , R_2 , R_{SS} , and any other components that affect the operating point. Underline, box, or in some other manner clearly identify the final results of your hand calculations (i.e., the final component values, which must also be real 5% values) and record your results, including V_G , on the cover page.

External Capacitors

Set all external capacitors to 1 mF for your preliminary design simulations to ensure that they do not influence your results. The final value of the capacitors will be determined in Part 9.

6. Simulation of preliminary design

- (a) Create a simulation schematic of your circuit using a 2N3819 and two additional, identical schematics of your circuit using the two Jbreak models and run an operating point simulation on all three schematics simultaneously. (You can have all three schematics on the same page.)
- (b) Enable the bias voltage display and the bias current display so that the all bias point information is displayed on your schematics. Move the bias point display boxes, if necessary, to ensure that they do not overlap or conceal any component values or designations. Include this page of schematics for all three circuits, which also display the bias point information, in your report.
- * (c) Provide a written comment on the success (or failure) of your preliminary bias point calculations. If your simulation agrees with your calculations, a simple statement to that effect is sufficient. If your simulation does not produce the predicted operating point, identify the weakness in your analysis, explain on the cover page, and modify your analysis.
- (d) If and only if your preliminary design did not achieve the operating point you predicted, return to Part 5e, reconsider your choice of component values and repeat Part 6.

7. A.C. simulation of the complete amplifier

- (a) Modify the simulation schematics of your circuit, if necessary, to include an ac signal source (VAC) of amplitude 1 mV. Perform an ac simulation on all three circuits over the range of at least 1 Hz to 1 MHz to show that the gain requirement is satisfied by all three circuits. Include this plot showing the performance of all three amplifiers in your report.
- (b) If and only if your preliminary design did not achieve the required gain, return to Part 6b.

8. Transient simulation of the complete amplifier

- (a) Using the same circuits used in Part 7, and replacing the ac signal source with a sinusoidal source (VSIN) having an amplitude of 0.1 V and frequency of 1 kHz, perform a transient simulation of all three circuits and produce a plot of the output voltage as a function of time for the time interval 0 to 10 ms.
- (b) Using the cursor, mark a peak (maximum value) and trough (minimum value) on the smallest (lowest amplitude) of the three waveforms of item 8a. These points must be marked using the cursor, not handwritten. Include this plot in your report.
- (c) Using the values marked by the cursor on the plots of item 8b, calculate the peak-to-peak voltage of the smallest waveform and determine the gain. Clearly identify these quantities by an underline, box, or some other type of identification and record on the cover page.

9. Selection of external (coupling) capacitors (neatly handwritten)
- * (a) Calculate and show your calculations for the minimum value of each external capacitor required for your circuits to ensure that $f_L < 10$ Hz.
 - (b) Select the capacitor values (in accord with the capacitor restrictions) and clearly identify the final values that you intend to use by an underline, box, or some other type of identification and record the final values on the cover page.
 - (c) Replace the transient source, VSIN, with an ac source, VAC, having an amplitude of 1 mV. Perform an ac simulation on all three circuits over the range of at least 10 Hz to 1 MHz to show that both the gain requirement and frequency response requirement are satisfied by all three circuits. Include this plot showing the performance of all three amplifiers in your report.
 - * (d) Provide the schematics and corresponding complete Spice output file used for Part 9c. (You may remove page breaks, blank lines, and reduce font size to no smaller than 8 points if you wish to conserve paper; however, do not alter any text in the output file.)
 - * Pay special attention to these items.
 - * * Save a copy of your report and hand calculations for use in your ECE 208 Lab Report.

NOTE: The schematics and corresponding complete Spice output file used for Part 9c are required.

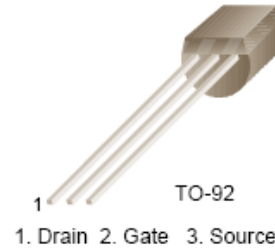
Although you are encouraged to work with your classmates, each student is required to create their own simulation and produce their own plots and other results from their own unique simulations. Potential sanctions are provided on the course website.

Minimum report requirements:

- 1) Completed cover page showing preliminary design results (cover page is provided below) including:
 - a) Device parameters for minimum and maximum device models.
 - b) Brief explanation of choice of amplifier prototype.
 - c) Hand-drawn schematic with all components identified with the designation used in your preliminary design calculations.
 - d) The minimum value of g_m that you intend to achieve and the value of R_D selected.
 - e) A clear, concise, and compelling explanation of how and why you selected those particular values of $g_m(\text{min})$ and R_D .
 - f) Value of load line intercept, V_G , determined in your preliminary design and all remaining resistive elements used to establish the chosen operating point (single 5% resistor values only).
 - g) Comments on the success (or failure) of your preliminary bias point calculations.
 - h) Values of the resistors used in your final design (even if identical to the original design).
 - i) Standard values for the external capacitors you determined to ensure $f_L < 10$ Hz.
 - j) Minimum voltage gain $|A_{Vs}|$ calculated from the transient simulation.
- 2) Plots of output characteristics and transfer characteristic plots for each of the three transistor models.
- 3) Plot of the transconductance for all three transistor models. (May be combined with Item 4 below.)
- 4) Plot from a single Probe window showing the minimum value of g_m (generated with “Add Trace”) on the transconductance plot and your Load-Line (generated with “Add Trace”) on the plot of the transfer characteristics for the three device models.
- 5) Neatly prepared hand calculation of the component values required to achieve your operating point.
- 6) PSpice simulation schematic displaying the bias point voltages and currents for three transistors.
- 7) A.C. simulation plots of all three circuits showing that mid-frequency gains meet specifications.
- 8) Neatly prepared hand calculation of design modification (if necessary).
- 9) Transient plots for all three circuits, including the cursor marked peak and trough of each output waveform.
- 10) Neatly prepared hand calculation of the capacitor values required to ensure $f_L < 10$ Hz.
- 11) Output plots of the A.C. frequency response for all three circuits (10 Hz to 1 MHz) demonstrating that each of the three transistors achieve the required gain and frequency response in your circuit.
- 12) The schematics and complete Spice output file corresponding to the schematic used for Part 9c (the final A.C. simulation used to display the complete frequency response). **REQUIRED**
(You may remove page breaks, blank lines, and reduce font size to no smaller than 8 points if you wish to conserve paper; however, do not alter any text in the output file)

N-Channel RF Amplifier

- This device is designed for RF amplifier and mixer applications operating up to 450MHz, and for analog switching requiring low capacitance.
- Sourced from process 50.



Epitaxial Silicon Transistor

Absolute Maximum Ratings* $T_C=25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DG}	Drain-Gate Voltage	25	V
V_{GS}	Gate-Source Voltage	-25	V
I_D	Drain Current	50	mA
I_{GF}	Forward Gate Current	10	mA
T_{STG}	Storage Temperature Range	-55 ~ 150	$^\circ\text{C}$

* This ratings are limiting values above which the serviceability of any semiconductor device may be impaired.

NOTES:

- 1) These rating are based on a maximum junction temperature of 150 degrees C.
- 2) These are steady limits. The factory should be consulted on applications involving pulsed or low duty cycle operations.

Electrical Characteristics $T_C=25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
Off Characteristics						
$V_{(BR)GSS}$	Gate-Source Breakdwon Voltage	$I_G = 1.0\mu\text{A}, V_{DS} = 0$	25			V
I_{GSS}	Gate Reverse Current	$V_{GS} = -15\text{V}, V_{DS} = 0$			2.0	nA
$V_{GS(off)}$	Gate-Source Cutoff Voltage	$V_{DS} = 15\text{V}, I_D = 2.0\text{nA}$			8.0	V
V_{GS}	Gate-Source Voltage	$V_{DS} = 15\text{V}, I_D = 200\mu\text{A}$	-0.5		-7.5	V
On Characteristics						
I_{DSS}	Zero-Gate Voltage Drain Current	$V_{DS} = 15\text{V}, V_{GS} = 0$	2.0		20	mA
Small Signal Characteristics						
g_{fs}	Forward Transfer Conductance	$V_{DS} = 15\text{V}, V_{GS} = 0, f = 1.0\text{KHz}$	2000		6500	μmhos
g_{oss}	Output Conductance	$V_{DS} = 15\text{V}, V_{GS} = 0, f = 1.0\text{KHz}$			50	μmhos
y_{fs}	Forward Transfer Admittance	$V_{DS} = 15\text{V}, V_{GS} = 0, f = 1.0\text{KHz}$	1600			μmhos
C_{ISS}	Input Capacitance	$V_{DS} = 15\text{V}, V_{GS} = 0, f = 1.0\text{KHz}$			8.0	pF
C_{RSS}	Reverse Transfer Capacitance	$V_{DS} = 15\text{V}, V_{GS} = 0, f = 1.0\text{KHz}$			4.0	pF

Thermal Characteristics $T_A=25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Max.	Units
P_D	Total Device Dissipation Derate above 25°C	350 2.8	mW mW/ $^\circ\text{C}$
$R_{\theta JC}$	Thermal Resistance, Junction to Case	125	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	357	$^\circ\text{C/W}$

* Device mounted on FR-4 PCB $1.5" \times 1.6" \times 0.06"$

Name _____

ECE 255
Fall 2009

ELECTRONIC ANALYSIS AND DESIGN
PSpice Design 3– Preliminary and Final Design Results

Device Parameters	I_{DSS} $V_{DS} = 15 \text{ V}$	$V_{GS} @ I_D = 200 \mu\text{A}$ $V_{DS} = 15 \text{ V}$	Lambda	Beta	VTO
Min $ V_P $	2.0 mA	-0.5 V	0.003 V^{-1}		
Max $ V_P $	20 mA	-7.5 V	0.001 V^{-1}		

Explanation of choice of amplifier prototype:

Hand-drawn schematic:

Intended operating point and R_D :

$g_m(\text{min}) = \underline{\hspace{2cm}}$

$R_D = \underline{\hspace{2cm}}$

Explanation of why this operating point was chosen:

Load line intercept, source resistor(s) and bias component values from preliminary design:

$V_G = \underline{\hspace{2cm}}$, $R_{SS} = \underline{\hspace{2cm}}$, $(R_{SS2}) = \underline{\hspace{2cm}}$, and $R_1 = \underline{\hspace{2cm}}$, $R_2 = \underline{\hspace{2cm}}$

Comments on the success (or failure) of your preliminary bias point calculations.

Whether or not redesign is required, list the final values used in your simulation:

$R_D = \underline{\hspace{2cm}}$, $R_{SS} = \underline{\hspace{2cm}}$, $(R_{SS2}) = \underline{\hspace{2cm}}$, $R_1 = \underline{\hspace{2cm}}$, $R_2 = \underline{\hspace{2cm}}$

Component values for external capacitors used:

Minimum transient voltage gain $|A_{Vs}|$

$C_1 = \underline{\hspace{2cm}}$, $C_2 = \underline{\hspace{2cm}}$, $(C_{SS}) = \underline{\hspace{2cm}}$ $|A_{Vs}|_{\text{min}} = \underline{\hspace{2cm}}$