ID # ____________________

NAME ____________________

EE-255 EXAM 2 March 4, 1999

Instructor (circle one) Nyenhuis Talavage

This exam consists of 12 multiple choice questions and three workout problems. Record all answers to the multiple choice questions on this page. You must turn in the entire exam. There will be no partial credit for the multiple choice questions, but there will be partial credit for the workout problems. You MUST show your work on the workout problems.

Circle the one best answer for each question. Five points per question.

Do not open and begin until you are instructed to do so!

1) a b c d e

2) a b c d e

3) a b c d e

4) a b c d e

5) a b c d e

6) a b c d e

7) a b c d e

8) a b c d e

9) a b c d e

10) a b c d e

11) a b c d e

12) a b c d e

1) What is the "Early effect" in a bipolar transistor?

(a) It works best Early in the morning
(b) β decreases when V_{CE} is increased
(c) I_B increases when V_{CE} is increased
(d) I_C increases when V_{CE} is increased
(e) There is an increase in leakage current when V_{CE} is increased

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2) As the temperature of an npn bipolar transistor increases from 0 °C to 100 °C, which statement is most likely to be correct?

(a) β and V_{BE} increase
(b) β and V_{BE} decrease
(c) β increases and V_{BE} decreases
(d) β decreases and V_{BE} increases
(e) β and V_{BE} do not change

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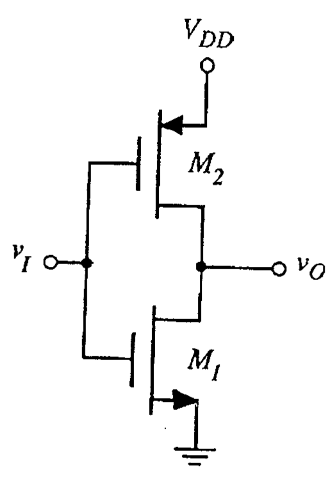
3) Consider the CMOS inverter shown. For the NMOS device, $V_{th} = 1$ V, $k_n = 1$ mA/V^2. For the PMOS device, $V_{th} = -2$ V and $k_p = 1$ mA/V^2. For what values of V_I is V_O precisely equal to 0 if $V_{DD} = 5$ V?



(a) $0 \text{ V} < V_I < 5 \text{ V}$
(b) $1 \text{ V} < V_I < 5 \text{ V}$
(c) $2 \text{ V} < V_I < 5 \text{ V}$
(d) $3 \text{ V} < V_I < 5 \text{ V}$
(e) $4 \text{ V} < V_I < 5 \text{ V}$

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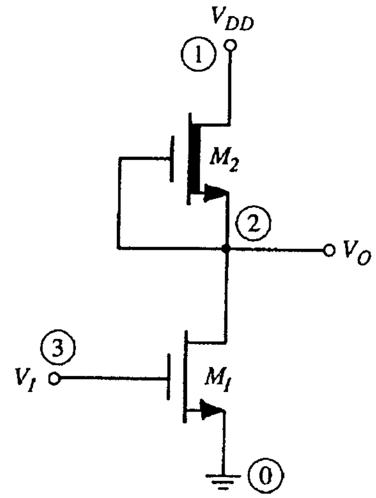
4) Which two spice lines correctly describe M2 in the circuit shown? (The substrate is connected to ground)



(a) .model dep_fet nmos vto=-1 kp=1e-4
M2 1 2 2 0 dep_fet L=1e-6 W=1e-5

(b) .model dep_fet nmos vto=1 kp=1e-4
M2 1 2 2 0 dep_fet L=1e-6 W=1e-5

(c) .model dep_fet nmos vto=-1 kp=1e-4
M2 0 2 2 1 dep_fet L=1e-6 W=1e-5

(d) .model dep_fet nmos vto=-1 kp=1e-4
M2 1 2 2 0 nmos L=1e-6 W=1e-5

(e) .model dep_fet nmos vto=-1 kp=-1e-4
M2 2 2 1 0 dep_fet L=1e-6 W=1e-5

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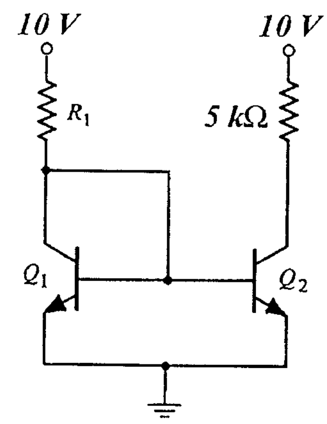
5) In the following circuit, the transistors are matched with $\beta = 100$ and $V_{BE}(on) = 0.7$ V. What value of R_1 will lead to $V_{CE2} = 5$ V?



(a) 1.3 kΩ (b) 3.3 kΩ (c) 5.3 kΩ (d) 7.3 kΩ (e) 9.3 kΩ

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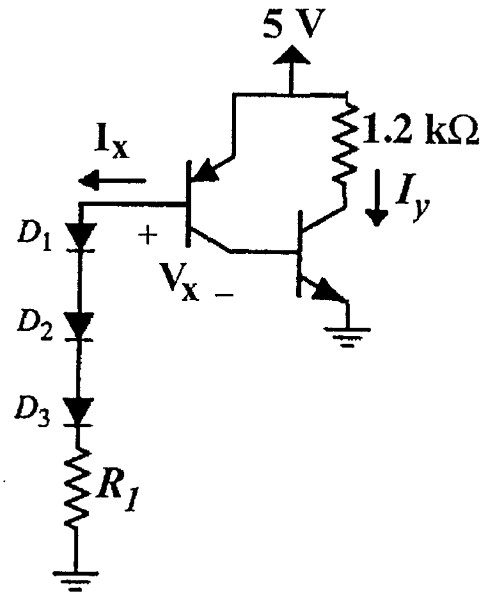
6) For the circuit below, $\beta = 25$ for both transistors, $R_1 = 2.2\ M\Omega$, $|V_{BE}(on)| = |V_\gamma| = 0.7$ V, $|V_{CE}(sat)| = 0.2$ V. $I_X = ?$



(a) –2 μA (b) –1 μA (c) 0 μA (d) 1 μA (e) 2 μA

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7) For the circuit in problem #6, $V_X = ?$

(a) 2.2 V (b) 2.9 V (c) 3.6 V (d) 4.3 V (e) 5.0 V

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8) For the circuit in problem #6, if R_1 is chosen such that $|I_X| = 10\ \mu A$, I_y is most nearly

(a) 0 mA (b) 2 mA (c) 4 mA (d) 6 mA (e) 8 mA

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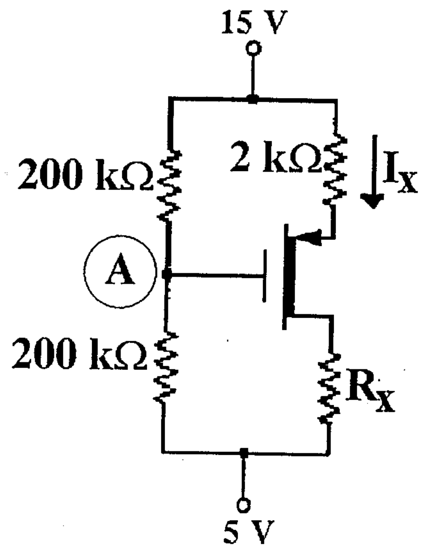
9) For the circuit below, what is the voltage, referenced to ground, at node A? (The transistor has parameters $V_{th} = 1$ V and $k = 0.5$ mA/V^2)



(a) 0.0 V (b) +2.5 V (c) +5.0 V (d) +7.5 V (e) +10.0 V

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10) For the circuit in problem #9, if $R_X = 2$ kΩ, I_X = ?

(a) 0 mA (b) 1 mA (c) 2 mA (d) 3 mA (e) 4 mA

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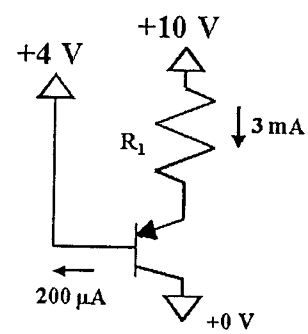
11) Assume $V_{BE}(on) = -0.6$ V and $V_{CE}(sat) = -0.2$ V. What is the value of R_1?



(a) 1.0 kΩ (b) 1.4 kΩ (c) 1.8 kΩ (d) 1.9 kΩ (e) 3.4 kΩ

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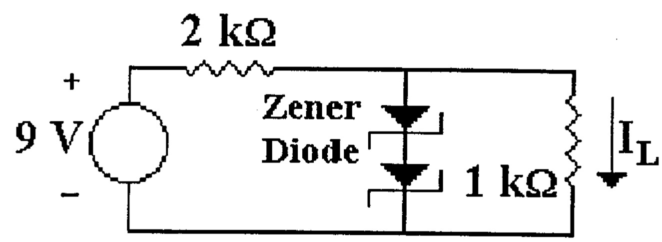
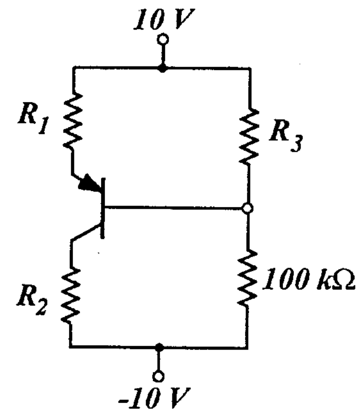
12) The zener diode used in the following circuit has parameters $V_{Z0} = 4.0$ V, $r_Z = 0.0\ \Omega$, $V_O = 0.7$ V, $R_O = 4\ \Omega$. The current I_L is most nearly



(a) 0.0 mA (b) 0.7 mA (c) 1.5 mA (d) 3.0 mA (e) 4.0 mA

SHOW ALL WORK FOR PROBLEM 13 ON THIS SHEET

13) Design the following circuit such that it is bias stable with $I_C < 5$ **mA**, $|V_{CE}| > 5$ **V** and a total power dissipation in the transistor of less than 20 mW (**$P_D < 20$ mW**). You are given that $\beta = 100$, $V_{BE}(on) = -0.5$ V, $V_{CE}(sat) = -0.2$ V. (20 pts)



(5 pts) a) State your values for I_C, V_{CE} and P_D, the power dissipated in the transistor (Recall the stipulations above)

I_C = [ ]

V_{CE} = [ ]

P_D = [ ]

(10 pts) b) Compute appropriate values for R_1, R_2 and R_3.

R_1 = [ ]

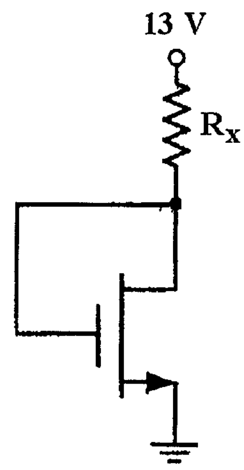
R_2 = [ ]

R_3 = [ ]

(5 pts) c) Demonstrate that your circuit meets the bias stable criterion.

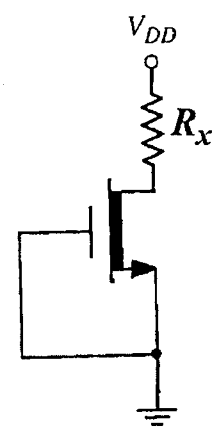
SHOW ALL WORK FOR PROBLEMS 14 AND 15 ON THIS SHEET

14) For the following circuit, determine a value for R_X such that $I_D = 9$ mA. You are given that $V_{th} = 1$ V and $k = 10^{-3}$ A/V^2. (10 pts)



R_X =

15) For the following circuit, determine a value for R_X and source V_{DD} such that $V_{DS} = 5$ V. You are given that $V_{th} = -2$ V and $k = 10^{-3}$ A/V^2. (10 pts)



R_X =

V_{DD} =

EE-255 Formula Sheet: Exam 2

Data:

$At\ 25^\circ C(R.T.)\quad V_T = kT/q = 0.026\ V \qquad k = 1.3806\times10^{-23}\ J/K$

$q = 1.6022\times10^{-19}\ C \qquad 0^\circ C = 273.16K$

Formulas:

$e^x = 1 + x + x^2/2 + \cdots$

Diodes:

$I_D = I_0\left(e^{V_D/nV_T} - 1\right) \quad V_D = V_0 + I_D R_0 \qquad C_j = \dfrac{C_{j0}}{\left(1 - V_D/V_{bi}\right)^N} \quad nV_T = \dfrac{V_{D2} - V_{D1}}{\ln(I_{D2}/I_{D1})}$

$r_d = \left.\dfrac{dv_D}{di_D}\right|_Q = \dfrac{nV_T}{I_D + I_0} \qquad v_D = V_D + v_d$

Rectifiers:

$V_r = V_M\left(\dfrac{T_p}{RC}\right)$

Monolithic Resistors:

$R = R_S\left(\dfrac{L}{W}\right)$

n-channel MOSFETs:

$I_D = k_n\left[2(V_{GS} - V_{Th})V_{DS} - V_{DS}^2\right]$ (ohmic/triode)

$I_D = k_n\left[V_{GS} - V_{Th}\right]^2$ (saturation)

$V_{GS} > V_{Th}$ (NOT cut-off)

$V_{DS} > V_{GS} - V_{Th}$ (saturation)

p-channel MOSFETs:

$I_D = k_p\left[2(V_{GS} - V_{Th})V_{DS} - V_{DS}^2\right]$ (ohmic/triode)

$I_D = k_p\left[V_{GS} - V_{Th}\right]^2$ (saturation)

$V_{GS} < V_{Th}$ (NOT cut-off)

$V_{DS} < V_{GS} - V_{Th}$ (saturation)

$I_D = k_p\left[2(V_{SG} + V_{Th})V_{SD} - V_{SD}^2\right]$ (ohmic/triode)

$I_D = k_p\left[V_{SG} + V_{Th}\right]^2$ (saturation)

$V_{SG} > -V_{Th}$ (NOT cut-off)

$V_{SD} > V_{SG} + V_{Th}$ (saturation)

MOSFETs:

$r_o = \dfrac{1}{\lambda I_D} = \dfrac{V_A}{I_D} \qquad V_{Th} = V_{Th0} + \gamma\left[\sqrt{2\phi_f + V_{SB}} - \sqrt{2\phi_f}\right]$

Bipolar Transistors:

$I_C = \beta I_B \cong I_S\, e^{\frac{V_{BE}}{V_T}}\left(1 + \dfrac{V_{CE}}{V_A}\right)$ (*active*) $\qquad \beta = \dfrac{\alpha}{1-\alpha} \quad \alpha = \dfrac{\beta}{1+\beta}$

$I_C = \dfrac{\beta\left[V_{Th} - V_{BE}(on)\right]}{R_{Th} + (\beta+1)R_E}$

Thermal Effects:

$T_{dev} - T_{amb} = \theta P_D \qquad P_D = I_B V_{BE} + I_C V_{CE} \qquad P_D = I_D V_{DS}$