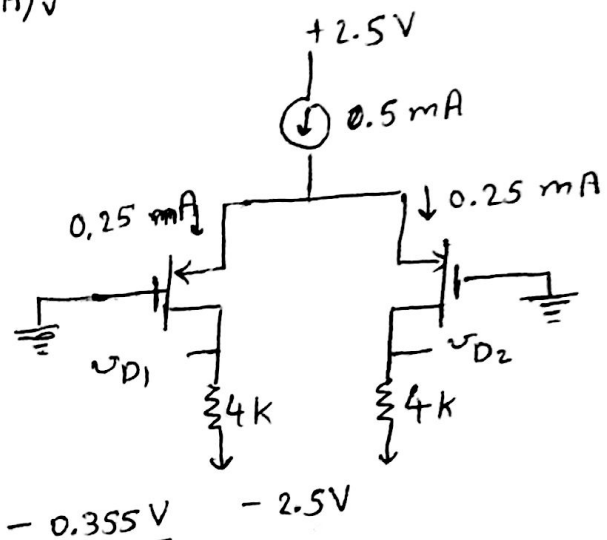
HW 11 Solution

8.2 $V_{tp} = -0.8V$, $K_p' \frac{W}{L} = 4\ mA/V^2$



(a) $v_{G1} = v_{G2} = 0$.

$v_{GS1} = v_{GS2}$ and the transistors are matched. so, $I_1 = I_2 = I/2$

$= 0.25\ mA$

$\frac{I}{2} = \frac{1}{2} K_p' \frac{W}{L} (V_{OV})^2$

$\Rightarrow 0.5 = 4 (V_{OV})^2 \Rightarrow |V_{OV}| = 0.355V$

$V_{OV} = -0.355\ V$

$|V_{OV}| = V_{SG} - |V_{tp}| = V_{SG} - 0.8 \Rightarrow V_{SG} = 1.155\ V \Rightarrow V_{GS} = -1.155\ V$

$V_S = V_G - V_{GS} = 0 + 1.155 = 1.155V$

$-2.5 + I/2\,(4K) = -2.5 + 0.25\,(4) = -1.5V = V_{D1} = V_{D2}$

(b) ~~$V_{CM\,max} = V_t$~~ * $V_{OS} < V_{GS} - V_{tp}$ (To remain in sat^n region),

$V_D < V_G - V_{tp} \Rightarrow V_{G\,min} = V_D + V_{tp}$

$V_{CM\,min} = -1.5 - 0.8 = -2.3V$

$|V_{OV}| = V_{SG} - |V_{tp}|$

$2.5 - V_{CS} - V_{SG} = V_{CM} \Rightarrow 2.5 - V_{CS} - (|V_{OV}| + |V_{tp}|) = V_{CM}$

$V_{CS} > 0.5V \Rightarrow 2.5 - (0.355 + 0.8) - V_{CM} > 0.5$

$\Rightarrow V_{CM\,max} = 2 - (1.155) = 0.845V$

Input common mode range $-2.3V < V_{CM} < 0.845\ V$

8.4 $v_{G2} = 0$, $v_{G1} = v_{id}$

Let's find the value of v_{id} at which $I_{Q1} = I$ and $I_{Q2} = 0$

This happens when V_{GS2} is ~~reduced~~ increased to V_t. (PMOS)

$\Rightarrow V_{SG2} = V_S = |V_{tp}| = 0.8V$

Now $I_{Q1} = \frac{1}{2}\left(K_p' \frac{W}{L}\right)(V_{SG1} - |V_{tp}|)^2 = I$

$\Rightarrow V_{SG1} = |V_{tp}| + \sqrt{2}\, V_{OV}$ (V_{OV} corresponds to $I_D = I/2$)

$\Rightarrow V_S - v_{id} = |V_{tp}| + \sqrt{2} V_{OV}$

$v_{id\,min} = -\sqrt{2}V_{OV}$ ($I_{Q1} = I$ and $I_{Q2} = 0$)

even if v_{id} is reduced beyond $-\sqrt{2}V_{OV}$, i_{Q1} remains I,

likewise current can be steered to Q_2 ($I_{Q2} = I$, $I_{Q1} = 0$)

with $v_{id\,max} = \sqrt{2}V_{OV}$

$$-\sqrt{2}V_{OV} \leq v_{id} \leq \sqrt{2}V_{OV}$$

$|V_{OV}| = 0.355\,V$ (found in 8.2 for $I_{Q1} = I_{Q2} = I/2$)

$$-0.5V \leq v_{id} \leq 0.5\,V$$

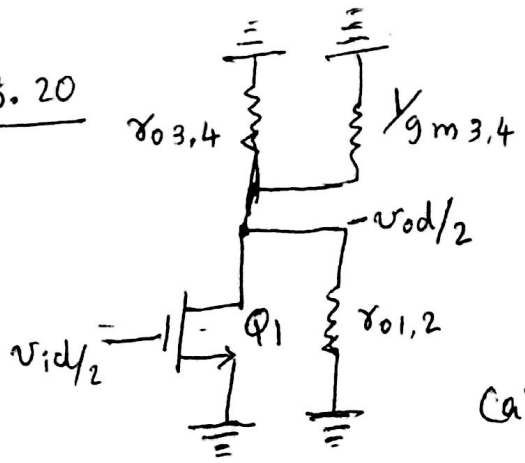
at $v_{id} = -0.5V$ $\quad v_{D1} = -2.5 + I(4) = -2.5 + 4(0.5) = -0.5\,V$

$v_{D2} = -2.5V$, $\quad v_S = 0.8V$

at $v_{id} = 0.5\,V$, $\quad v_{D1} = -2.5\,V$, $v_{D2} = -0.5\,V$, $0.8\,V$

$v_S - v_{G1} = 0.8 \Rightarrow v_S = 1.3\,V$

8.20



$$A_d = \frac{v_{od}}{v_{id}} = \frac{v_{od}/2}{v_{id}/2}$$

here $\dfrac{-v_{od}/2}{v_{id}/2} = -g_{m1,2}\left(r_{o1,2} \,||\, r_{o3,4} \,||\, 1/g_{m3,4}\right)$

(a) so $A_d = g_{m1,2}\left(r_{o1,2} \,||\, r_{o3,4} \,||\, 1/g_{m3,4}\right)$

(b) neglecting $r_{o1,2}$ and $r_{o3,4}$ $\quad A_d = g_{m1,2}/g_{m3,4}$

$$g_m = \mu C_{ox} W/L\, V_{OV} = \sqrt{2\mu C_{ox} W/L\, I_D}$$

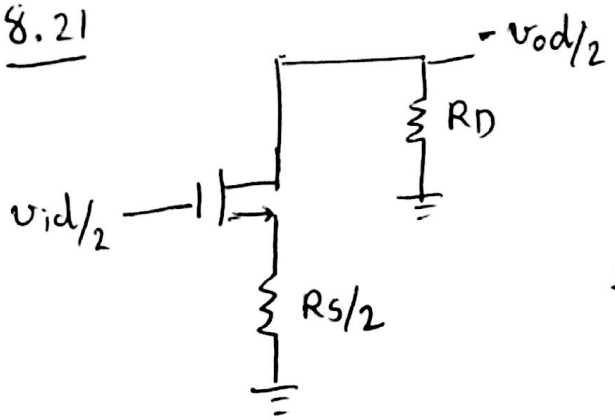
$$g_{m1,2} = \mu_n C_{ox}(W/L)_{1,2} V_{OV} = \sqrt{2\mu_n C_{ox}(W/L)_{1,2} I/2}$$

$$g_{m3,4} = \sqrt{2\mu_p C_{ox}(W/L)_{3,4} I/2}$$

so $A_d = \sqrt{\dfrac{\mu_n}{\mu_p}\dfrac{(W/L)_{1,2}}{(W/L)_{3,4}}}$ DC bias is same for PMOS & NMOS

(c) $10 = \sqrt{4\left(W_{1,2}/W_{3,4}\right)} \Rightarrow \boxed{W_{1,2}/W_{3,4} = 25}$

8.21



$$\frac{-v_{od}/2}{v_{id}/2} = \frac{-R_D}{1/g_m + R_S/2}$$

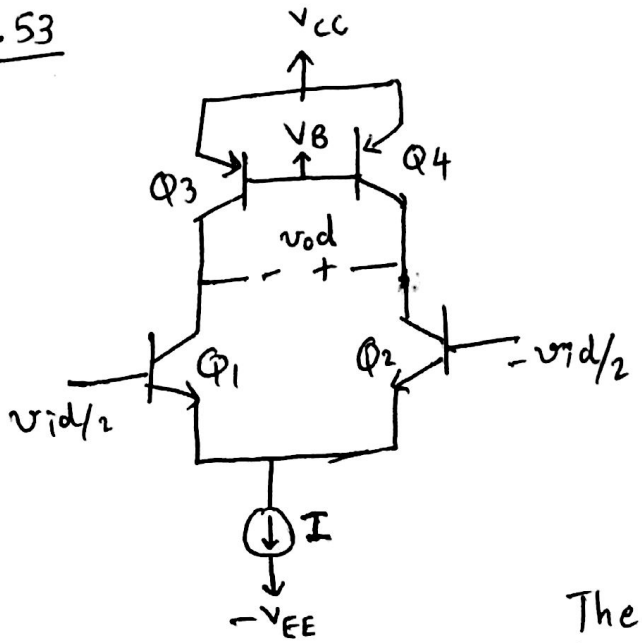
$$\Rightarrow \frac{v_{od}}{v_{id}} = \frac{R_D}{1/g_m + R_S/2} = A_d$$

with $R_S = 0$, $A_d = g_m R_D$

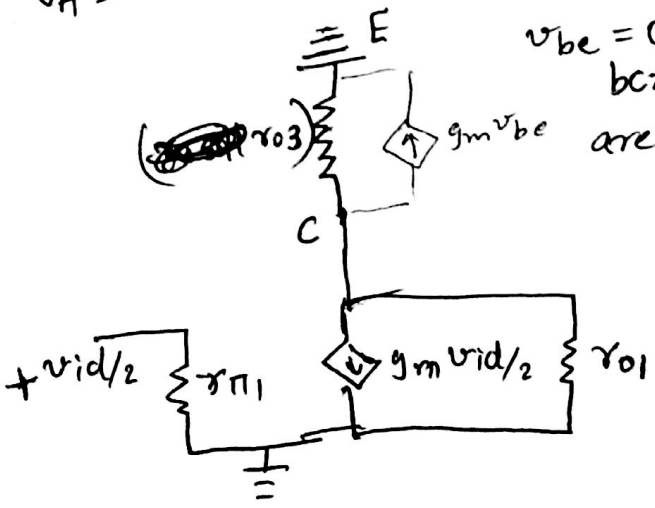
$$\text{gain} = \frac{1}{2} g_m R_D = \frac{R_D}{1/g_m + R_S/2} = \frac{R_D g_m}{1 + g_m R_S/2}$$

$$\Rightarrow 2 = 1 + g_m R_S/2 \Rightarrow \boxed{R_S = 2/g_m}$$

8.53



$V_A = 10\,V$ for all transistors



The pnp transistors are connected to V_B at the base.

$$\text{gain} = \frac{-v_{od}/2}{v_{id}/2} = -g_{m_1}(r_{o1} \,||\, r_{o3}) \Rightarrow \frac{v_{od}}{v_{id}} = g_{m_1}(r_o/2)$$

$$r_o = \frac{|V_A|}{I_C}, \quad g_m = \frac{I_C}{V_T}$$

$$= \frac{I/2}{V_T} \frac{|V_A|}{I/2\,(2)}$$

$$= \frac{10}{2(0.025)} = 200$$