EE-612 EXAM 2: Fall 2008 November 13, 2008

NAME KEY ______________ ID # ______________

This exam consists of **three** questions – each is divided into several parts. Following each problem, there is a sheet of scratch paper that you may use. **Do not remove this scratch paper from the exam.**

You are permitted to use a calculator, and you will need one.

You will be asked a series of questions that require you to perform some simple calculations. These are the kind of quick calculations that a device engineer should be able to do. If you find yourself doing a complicated analysis, you are not approaching the problem correctly. There may be a term or two that you cannot recall the definition of, but you should be able to figure out what is meant from the context of the question.

The last page is a formula sheet, which you may remove.

Be sure to clearly identify your answers and to show all of your work.

It is important that you CLEARLY show your work and that the final answer is CLEARLY marked. You may wish to use the scratch paper to get started, and then transfer the key results to the exam itself.

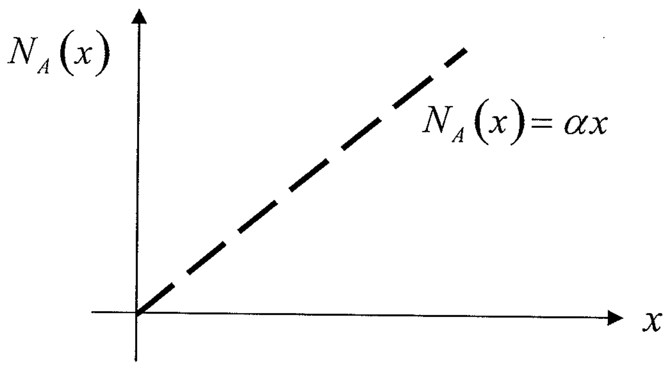
If I have trouble identifying your final answer and how you got it, the problem is yours, and there will be NO REGRADES. You will receive no credit for your answer, unless it is clear how you obtained the answer.

Scoring:

Problem 1:	**4 parts**	**10 points each**	**40 points total**
Problem 2:	**4 parts**	**10 points each**	**40 points total.**
Problem 3:	**2 parts**	**10 points each**	**20 points total.**

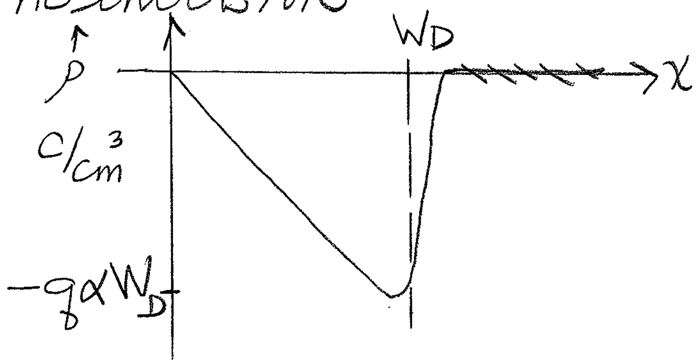
Problem I

Problem 1) consists of 4 questions about an MOS capacitor with a p-type channel doping profile that increases linearly with depth, x, into the substrate.



1a) Assume that the surface potential is positive, and make a sketch of the space charge density in C/cm^3 vs. x.

* assume no inversion



1b) Derive an equation that relates the electric field at the surface, E_S, to the depletion layer depth, W_D.

assume depletion approximation

$$\epsilon_{Si} \mathcal{E}_S = -Q_S \qquad Q_S = \frac{1}{2}\left(-q\alpha W_D\right) W_D$$

from Gauss' Law

$$\mathcal{E}_S = \frac{q\alpha}{2\epsilon_{Si}} W_D^2$$

I) continued

1c) Write down an equation for the spatially varying electric field, $E(x)$.

$$\frac{d\mathcal{E}(x)}{dx} = \frac{\rho(x)}{\epsilon_{Si}} = -q\frac{N_A(x)}{\epsilon_{Si}} = -\frac{q\alpha x}{\epsilon_{Si}}$$

1d) Solve the equation in part 1c) and find an expression for $E(x)$ in terms of the surface potential, W_D. HINT: for $x = 0$, your answer should agree with your answer to part 1b).

$$\frac{d\mathcal{E}}{dx} = -\frac{q\alpha}{\epsilon_{Si}} x$$

$$\int_0^{\mathcal{E}(x)} d\mathcal{E} = -\frac{q\alpha}{\epsilon_{Si}} \int_{W_D}^{x} x'dx' = -\frac{q\alpha}{\epsilon_{Si}} \left(\frac{x^2}{2} - \frac{W_D^2}{2} \right)$$

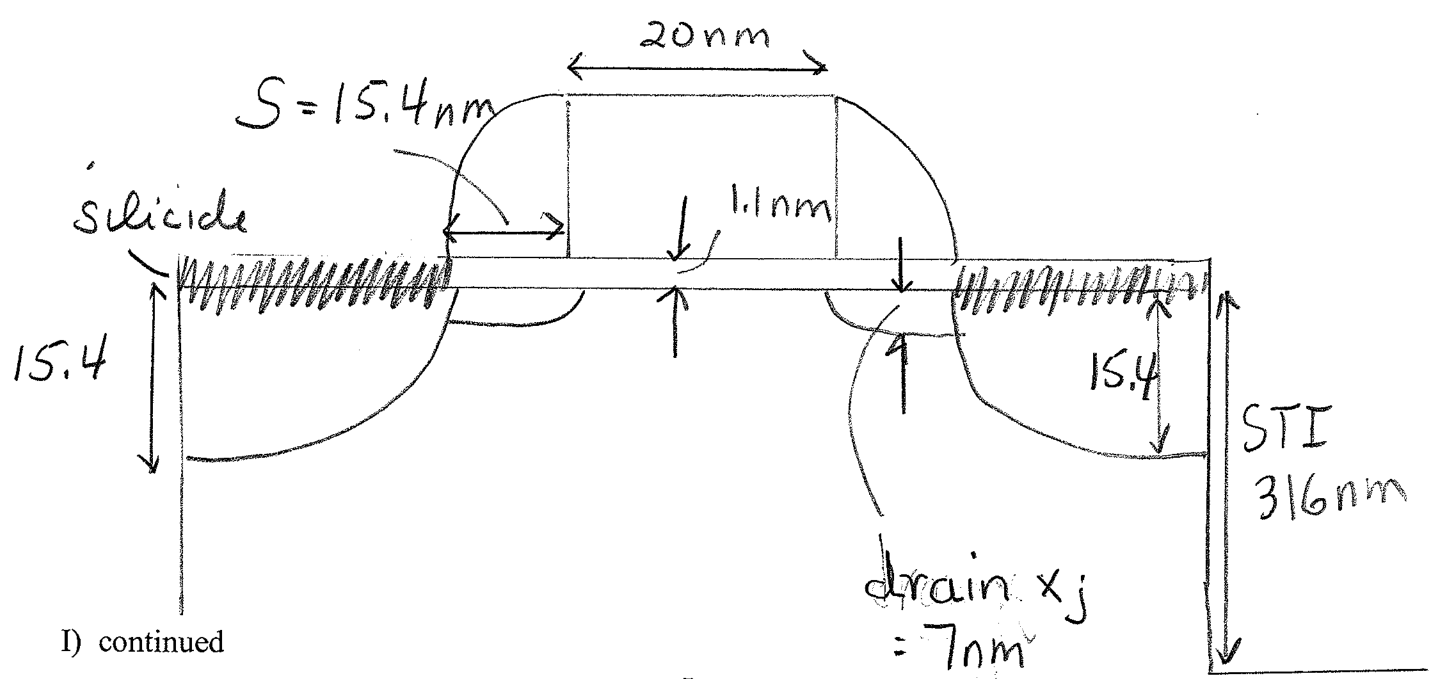
$$\mathcal{E}(x) = +\frac{q\alpha}{2\epsilon_{Si}} W_D^2 \left(1 - (x/W_D)^2 \right)$$

Problem II

The 2007 Edition of the ITRS lists the following parameters for the Low Standby Power (LSTP) planar, bulk MOSFET at 2012-2013 as:

Physical gate length:	20nm
EOT:	1.1nm
Gate poly depletion and inversion layer equivalent thickness:	3.1Angstroms
Maximum gate leakage current:	1.5E-01 A/cm^2
Vdd :	0.95V
Vt(sat):	547 mV
Isd,leak:	3.03E-05 μA/μm
Id,sat	519 μA/μm
Rsd:	180 Ω-μm
Cg, ideal:	4.9E-16 F/μm
Cg, total:	6.70E-16 F/μm
Drain extension Xj:	7nm
Drain extension sheet resistance:	1160 Ω/square
Contact Xj	15.4 nm
Allowable junction leakage:	21 pA/um
Sidewall spacer thickness:	15.4 nm
Contact maximum resistivity	5.6E-08 Ω-cm^2
STI depth	316 nm

2a) Using the information provided, sketch and label a cross-section of an NMOS transistor. (You should only label physical parameters on the sketch – not electrical parameters.



I) continued

2b) Using the information provided, compute the component of the series resistance due to the source or drain extension (in Ω-μm).

$$R_{ext} = \rho_{sd} \frac{S}{W} = 1160 \cdot \frac{15.4 \times 10^{-7}}{1 \times 10^{-4}} = 18\ \Omega\text{-}\mu m$$

$W = 1\ \mu m$

2c) Using the information provided, estimate how much (percentage wise) the series resistance lowers the intrinsic on-current.

$$\frac{\Delta I_D}{I_D} = \frac{R_S}{R_{ON} + R_S} = \frac{90}{776 + 90} = 9.6\%$$

$$R_S = R_{SD}/2 = 90$$

$$R_{ON} = \frac{V_{DD} - V_T}{I_{ON}} = \frac{0.95 - 0.547}{519\ \mu A/\mu m} = 776\ \Omega\text{-}\mu m$$

2d) Using the information provided, determine the average electron velocity at the beginning of the channel under on-current conditions.

$$I_{ON} = W C_G \underbrace{(V_{DD} - V_T - I_{ON} R_S)}\langle \upsilon(0) \rangle$$

$$0.95 - 0.547 - 0.519 \cdot 90 \times 10^{-3}$$

$$0.36\,V$$

$$C_G = \frac{\epsilon_{ox}}{(1.1 + 0.31)\,nm} = 2.45 \times 10^{-6}\ F/cm^2$$

$$\langle \upsilon(0) \rangle = \frac{I_{ON}}{W C_G (V_{DD} - V_T - I_{ON} R_S)} = \frac{519 \times 10^{-6}}{10^{-4} \cdot 2.45 \times 10^{-6} \times 0.36}$$

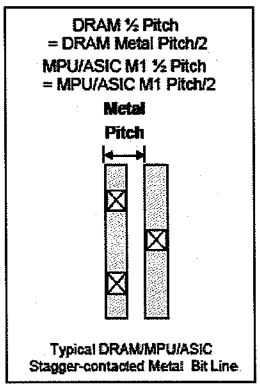
$$= 5.9 \times 10^{6}\ cm/s$$

Problem III

The 2007 Edition of the ITRS lists the following parameters for the 2013 Metal 1 layer:

Metal 1 wiring pitch:	64nm
Metal 1 A/R (for Cu):	1.9
Capacitance per unit length for M1 wires assuming Keff = 4.2:	1.8 pF/cm
Interconnect RC delay for a 1mm Cu M1 wire:	2075 ps

The ITRS Executive Summary provides the figure below.



L^2

You should also recall that: $\tau_w = 0.5 R_L C_L W^2$

3a) Using the information provided, determine the resistivity of the Cu Metal 1 wires in Ω-cm.

$R_L = \frac{\rho_w}{A_w}$ need R_L and A_w $A_w = 32nm \times (1.9 \times 32nm)$

$= 1946 nm^2$

$= 1.95 \times 10^{-11} cm^2$

$R_L = \frac{\tau_w}{0.5 \cdot C_L \cdot L^2} = \frac{2075 \times 10^{-12}}{0.5 \times 1.8 \times 10^{-12} \cdot 10^{-2}}$

$= 2.3 \times 10^5 \ \Omega/cm \Rightarrow \rho_w = R_L A_w = 4.5 \times 10^{-6} \ \Omega\text{-cm}$

3b) Compute the delay of a 2mm long M1 wire.

$\tau_w \sim L^2$

if L increases by 2X τ_w increases by 4X

$\tau_w = 4 \times 2075 ps = 8.3 ns$