EE-612 EXAM 1: Fall 2006 September 20, 2006

NAME_______________________________ ID # _________________________________

This exam consists of **three** questions – each is divided into several parts. Following each problem, there is a sheet of scratch paper that you may use. **Do not remove this scratch paper from the exam.**

You are permitted to use a calculator, and you will need one.

You will be asked a series of questions that require you to perform some simple calculations. These are the kind of quick calculations that a device engineer should be able to do. If you find yourself doing a complicated analysis, you are not approaching the problem correctly. There may be a term or two that you cannot recall the definition of, but you should be able to figure out what is meant from the context of the question.

The last page is a formula sheet, which you may remove.

Be sure to clearly identify your answers and to show all of your work.

It is important that you CLEARLY show your work and that the final answer is CLEARLY marked. You may wish to use the scratch paper to get started, and then transfer the key results to the exam itself.

If we have trouble identifying your final answer, the problems is yours, and there will be NO REGRADES. You will receive no credit for your answer, unless it is clear how you obtained the answer.

Scoring:

Problem 1: 10 parts 5 points each 50 points total
Problem 2: 2 parts 10 points each 20 points total.
Problem 3: 3 parts 10 points each 30 points total.

Problem I

Problem 1) consists of 10 questions about the MOSFET characteristics shown below. Use the information provided and reasonable assumptions to answer the following questions. **Assume *W* = 1 μm** and CLEARLY explain how you get each answer.

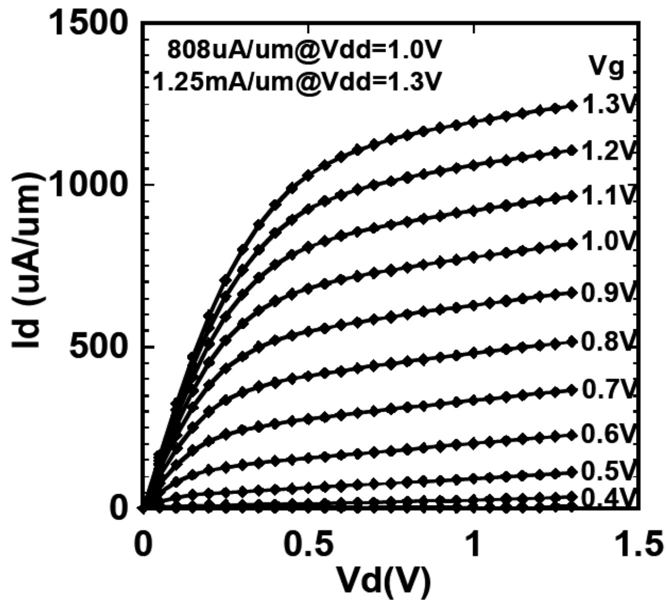

Fig. 16 Id-Vd characteristics of 65nm Lg nMOSFETs with $HfSi_x/HfO_2$ gate stack.

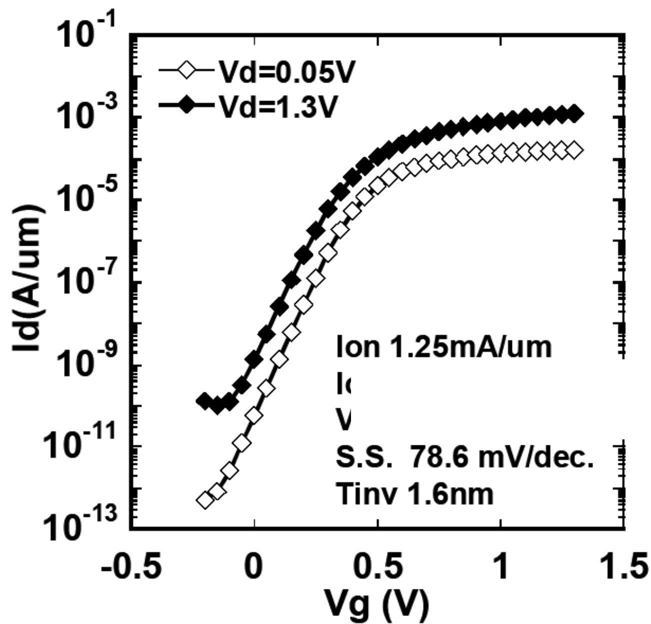

Fig. 17 Id-Vg characteristics of 65nm Lg nMOSFETs with $HfSi_x/HfO_2$ gate stack.

Source: T. Hirano, et al., 2005 IEDM.

Problem I (continued)

1a) Determine the on-current assuming that the power supply, $V_{DD} = 1.3V$

1b) Determine the off-current assuming that the power supply, $V_{DD} = 1.3V$

1c) Compute the approximate channel resistance for this MOSFET at $V_G = 1.3V$

1d) Compute the approximate output resistance for this device at $V_G = 1.3V$.

Problem I (continued)

1e) Compute the approximate drain induced barrier lowering (DIBL)

1f) Compute the gate capacitance in Farads per cm^2 (assume that T_{inv} is what we have called EOT_{elec}).

1g) Compute the approximate inversion layer electron density (per cm^2) under on-current conditions.

Problem I (continued)

1h) Estimate the velocity at the beginning of the channel (in cm/s) under on-current conditions.

1i) Estimate the body effect parameter, *m*.

1j) The typical device engineering would look at Fig. 16 and without doing any calculation would immediately say that this is a heavily velocity saturated transistor. Explain why he or she would say that.

Problem I (scratch paper)

Problem II

Consider a MOSFET or MOS capacitor at room temperature with $N_A = 1 \times 10^{18}$ cm^{-3} and answer the following questions

2a) Compute the surface potential, ψ_S, at the onset of strong inversion.

2b) Estimate the surface potential, ψ_S, when $|Q_i / q| = 1.0 \times 10^{13}$ cm^{-2}.

Problem II (scratch paper)

Problem III

Consider a p-channel MOSFET with $N_D = 1.0 \times 10^{18}$ cm^{-3} and a p+ poly silicon gate with $N_A = 1.0 \times 10^{20}$ cm^{-3}.

3a) Sketch an energy band diagram at $V_G = 0$ V being careful to show any poly depletion or accumulation.

3b) Compute the flatband voltage for this MOSFET (and be careful to get the sign correct).

3c) Assume that EOT = 1nm and that we require that poly depletion under on-current conditions with $Q_i / q = 1.0 \times 10^{13}$ cm^{-3} degrades the capacitance by no more than 10%. How heavily must the polysilicon be doped? (You may ignore the inversion layer capacitance.)

Problem III (scratch paper)