Fall 2008

EE 612: Nanoscale Transistors

SOLUTION TO HW1: MOSFET review

Exercises with nano-CMOS on www.nanoHUB.org

The purpose of this exercise is to help you review the basic theory of the MOSFET, device some key device parameters, and give you a feel for the typical values of key device performance metrics for state-of-the-art MOSFETs.

1) Locate the simulation tool, nano-CMOS, and use it to examine the IV characteristics of "45nm" N-channel CMOS technology. Select "NMOS 45nm," and use the default values. Push the "Simulate" button, and then answer the following questions.

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You should clearly describe how you obtain each parameter. You can download images from the nanoHUB and insert them in a Word file to document your work. Note that you are able to change the minimum and maximum axes scales and to select either linear or logarithmic scales.

a) Determine the on-current in μA/μm
b) Determine the off-current in μA/μm
c) Determine the subthreshold swing, S, in mV/decade
d) Estimate V_{DSAT} for $V_{GS} = 1.0$V. (Do not simply "eyeball" the answer; develop a simple methodology so that another person who follows it would get the same answer.
e) Estimate the DIBL in mV/V
f) Estimate V_T(lin) and V_T(sat) in V
g) Estimate the output resistance, R_o in Ω-μm
h) Estimate the channel resistance, R_{ch} in Ω-μm
i) Estimate the transconductance, g_m, in mS/mm at the maximum gate voltage.
j) The "self-gain," $A = g_m R_o$ is often used as a metric for analog applications (it is roughly the maximum small signal gain that could be achieved in an amplifier circuit with this transistor). Estimate the self-gain for this transistor.

Question 1 Solution: Device Parameters for 45 nm N-MOSFET

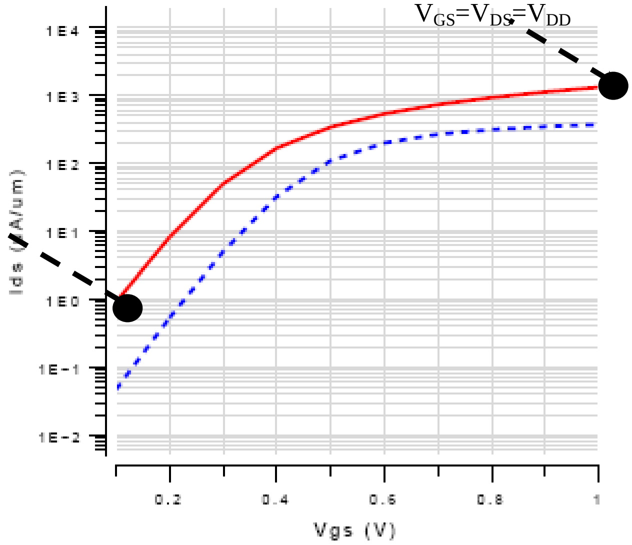
(a) On-current :

I_D when $V_{GS}=V_{DS}=V_{DD}$(power supply voltage)

On-current=1300 uA/um

(b) Off-Current :

I_{DS} when $V_{GS} = 0$ and $V_{DS} = V_{DD}$
By using extrapolation assuming the same slope around Vgs=0.1V, off-current is about 0.1uA/um.



On Current =
1.3e3uA/um @ 1V
$V_{GS}=V_{DS}=V_{DD}$

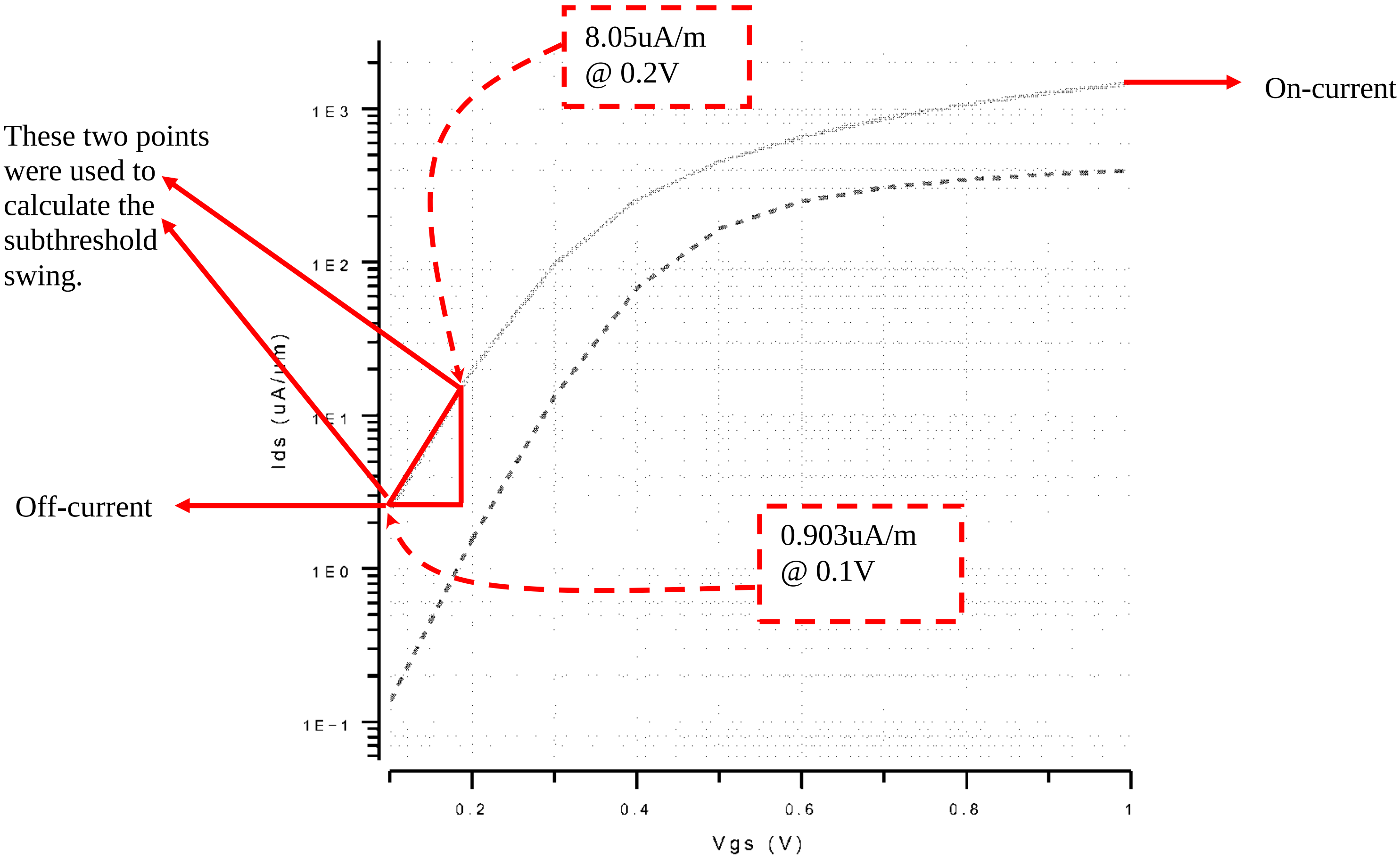
0.9uA/um @ V_{GS}=0.1
$V_{DS}=V_{DD}$

Figure 1

(c) <u>Subthreshold Swing (SS)</u>:

This parameter quantifies how abruptly the transistor turns on with increasing gate voltage (it is the inverse of subthreshold slope). It is defined as the gate-voltage change needed to induce a drain-current change of one order of magnitude. We typically do this at high V_D, because high drain voltages may degrade the SS by 2D electrostatics, so this is a worst case.

Subthreshold Swing = 140 mV/decade (below threshold Vth ~ 0.25V)



8.05uA/m
@ 0.2V

On-current

These two points were used to calculate the subthreshold swing.

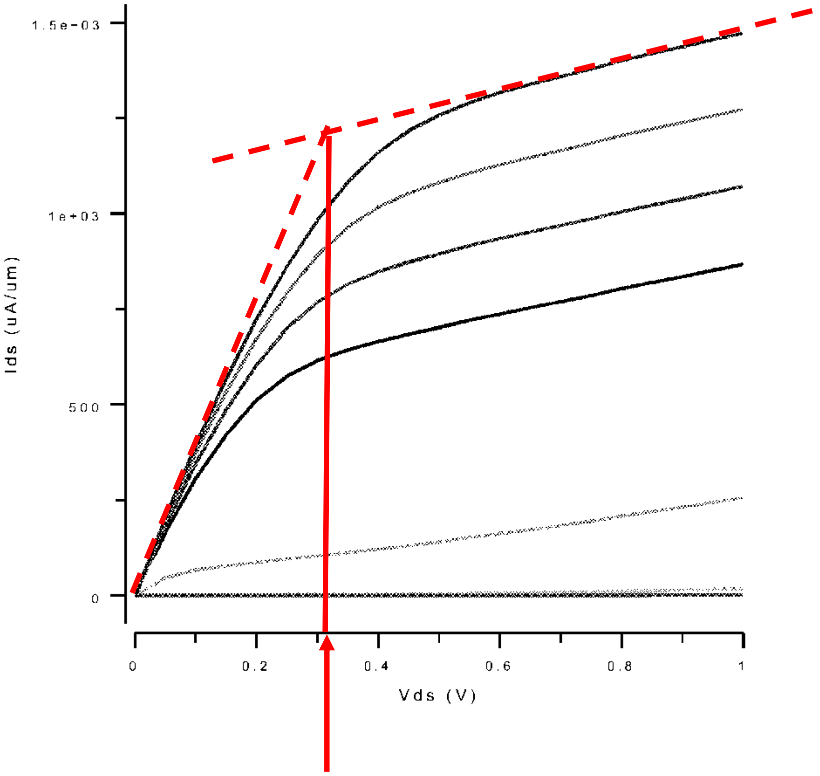
Off-current

0.903uA/m
@ 0.1V

(d) V_{DSAT} :

V_{DSAT} is the value of Drain Voltage at which I_{DS} saturates. $V_{DSAT}\uparrow$ as $V_G\uparrow$ because at higher gate voltage large number of carriers are required to Pinch-Off the channel (V_{DSAT} is the point of pinch off). Since V_{DSAT} is a function of V_G, here V_{DSAT} is taken for maximum V_G ie $V_{GS} = V_{DD}$. To determine V_{DSAT} from the I_D-V_D plot, tangents to the linear and saturation regiona of the I_D-V_D plot are drawn, and their intersection gives the value of V_{DSAT}.

$V_{DSAT} = 0.28$ V



The intercept gives the approximate value of V_{DSAT} for V_{GS} = 1.0 V

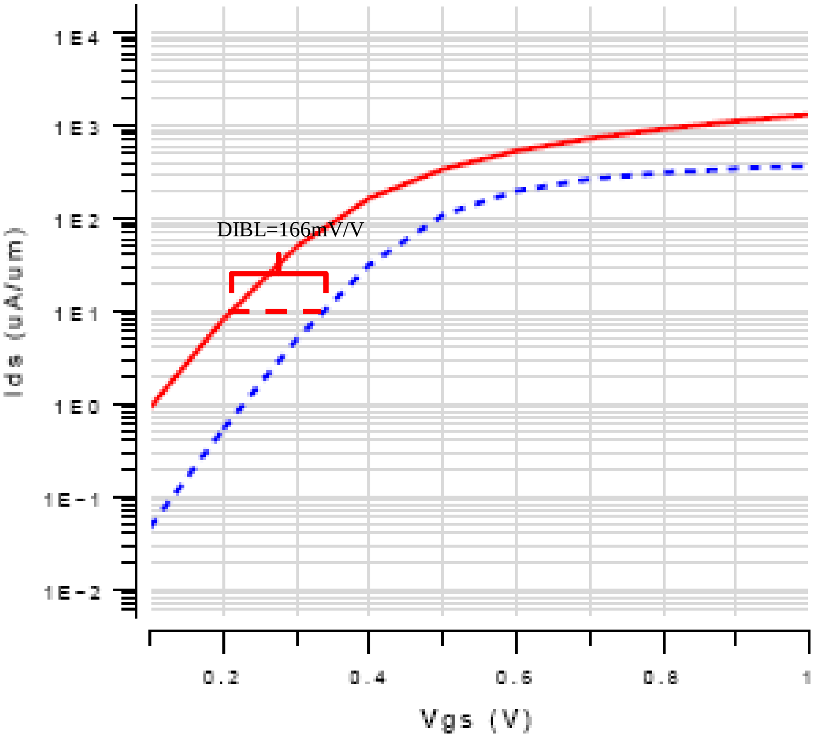
Figure 2

(e) Drain Induced Barrier Lowering (DIBL) :

When the source and drain depletion regions are a substantial fraction of the channel length, short-channel effects start to occur. DIBL is caused by lowering of the source-junction potential barrier below the built in potential. As the drain bias is increased the conduction band edge, which reflects the electron energies in the drain is pulled down and the drain channel depletion width expands. The net result is a large leakage current between the source and drain, and that this current is a strong function of the drain bias.

DIBL is calculated by taking the horizontal shift in the sub-threshold characteristics (in millivolts) divided by change in the V_D, on LogI_D-V_{GS} plot. We select a region of the plot where the drain current is exponential with gate voltage (linear on the logI_D plot) and where the low V_D and high V_D characteristics are parallel. In this case, we selected I_D = 10 uA/um.

DIBL = 167 mV/V



(f) V_T(Lin) :

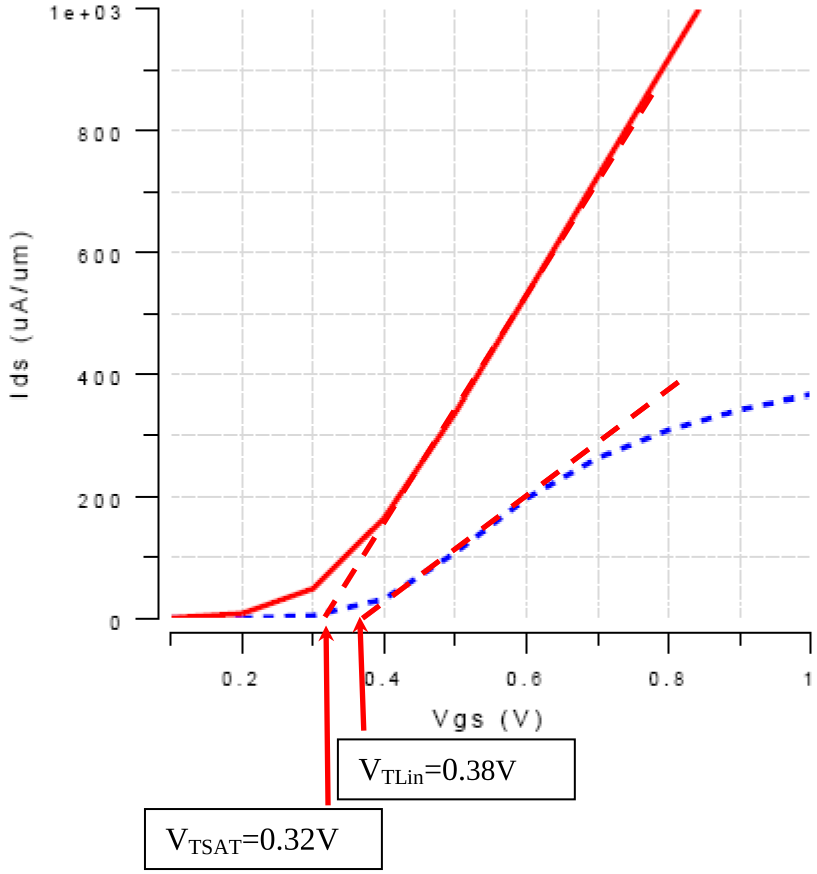
This is the threshold voltage for $V_D << V_G$ (i.e. in the linear region of operation). It is obtained by fitting a line to the point of maximum slope, and then finding the intercept with the x-axis.

V_T(Lin) = 0.38V

V_T(Sat):

This is the threshold voltage for high V_D (the saturated region of operation).

V_T(Sat) = 0.32V



V_{TLin}=0.38V

V_{TSAT}=0.32V

* It is more exact to correct $V_{ds}/2$ term, which is normally negligible if V_{ds} is so small.

** Following is also used for V_{Tsat} , $V_{Tsat} = V_{Tlin} - \text{DIBL} \times \Delta V_{DS}$

(g) Output resistance/Drain Resistance (R_0) :

This parameter reflects the non-saturating drain current with drain bias. It is calculated by taking 2 points on line 1 (refer figure 4 on next page) and using the formula $R_0 = \Delta V_D/\Delta I_D$

$R_0 = \Delta V_D/\Delta I_D = 2500\Omega$-um

(h) Channel Resistance (R_{CH}) :

At small Drain biases, a MOSFET acts like a resistor (the linear portion of I_D-V_D plot). The total resistance (R_{TOT}) is a sum of source-drain series resistance and channel resistance. It is calculated by taking 1 point on the linear portion of I_D-V_D and point 2 is taken at the origin. R_{TOT} is then calculated by using the formula $R_{CH} = \Delta V_D/\Delta I_D$. For point 1, we use a very small drain voltage. In this case, $V_D = 0.05V$ was used and we find:

$R_{TOT} = 259\ \Omega$-um
$R_{CH} = 259\ \Omega$-um – Rsd (=150 Ω-um) = 109 Ω-um

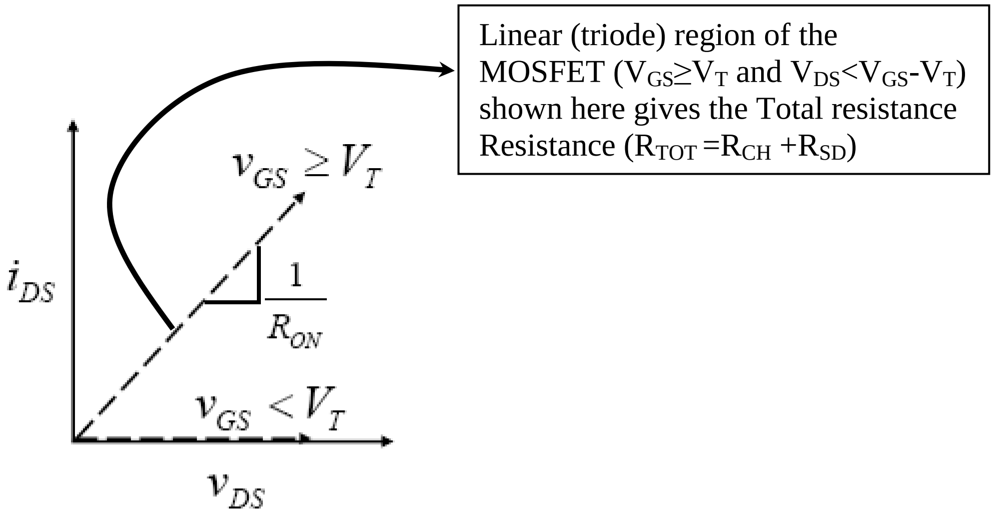

Linear (triode) region of the MOSFET ($V_{GS} \geq V_T$ and $V_{DS} < V_{GS} - V_T$) shown here gives the Total resistance Resistance ($R_{TOT} = R_{CH} + R_{SD}$)

Figure 3

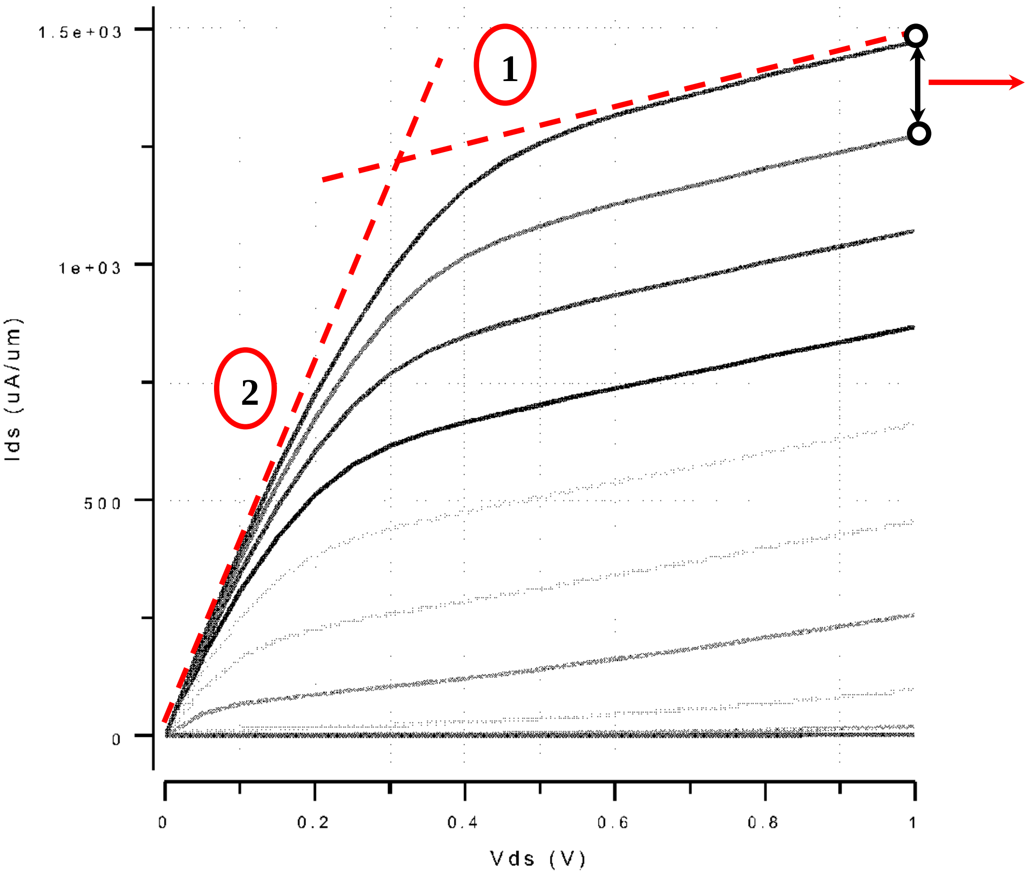
(i) Transcoductance (g_m):

This parameter measures the strength of the drain current change when the gate voltage changes. It is calculated by using the points indicated on the plot below and using the formula :

$g_m = \Delta I_D / \Delta V_{GS} = 1900\text{mS/mm}$

The units for transconductance are siemans per meter, or millisiemans per millimeter or microsiemans per micrometer. Device people tend to use mS/mm, but all three have the same numerical value.

(j) $A = g_m R_o \approx 5$

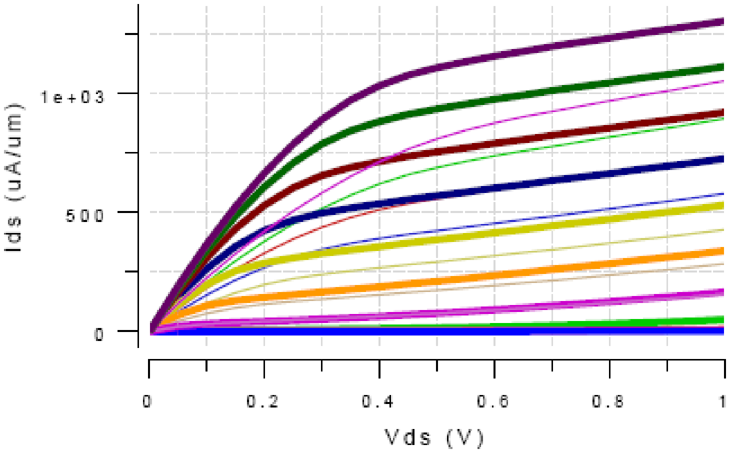


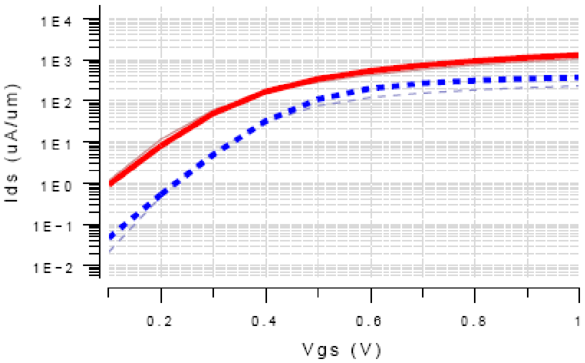
To find g_m use $\Delta I_D / \Delta V_{GS}$

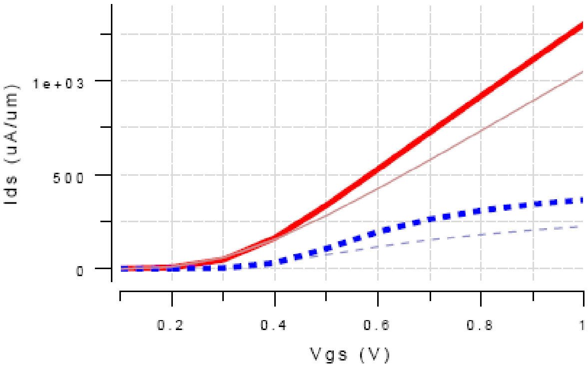
Figure 4

2) Repeat problem 1) for a p-channel MOSFET by selecting “PMOS 45nm,” and pushing the “Simulate” button. You should use the default values. Estimate all of the device parameters from problem 1) for the PMOS transistor. <u>Discuss</u> the main difference that you see.

Question 2 Solution: Comparison NMOS-45nm and PMOS-45nm







Question 2 Solution Cont.

Device parameter	**NMOS-45nm**	**PMOS-45nm**	**Inc↑ /Dec↓**	**Reason**
I_{ON} (µA/µm)	1300	1050	↓	Due to lower saturation velocuty of holes (PMOS) than electrons (NMOS).
I_{OFF} (µA/µm)	0.1	0.1		Typically designed to be the same.
V_{DSAT}	0.28	0.35		Due to lower saturation velocity of holes, pinch off occurs late.
SS (mV/dec)	139.9	96		A function of 2D electrostatics
DIBL (mV/V)	166	189		A function of 2D electreostatics
R_O (Ω-µm)	2500	2272	↓	Depends in complicated way on 2D design and transport (saturation velocity)
R_{ch} (Ω-µm)	109	227		Due to lower mobility of holes, channel resistance is higher for PMOS
g_m (mS/mm)	1900	1580	↓	Due to lower saturation velocity of holes.
A	4.7	3.6	↓	The product of g_m and R_o ; both are lower for PMOS.
V_T (sat) (V)	0.32	0.28		Typically designed to be similar
V_T (lin) (V)	0.38	0.35		Typically designed to be similar

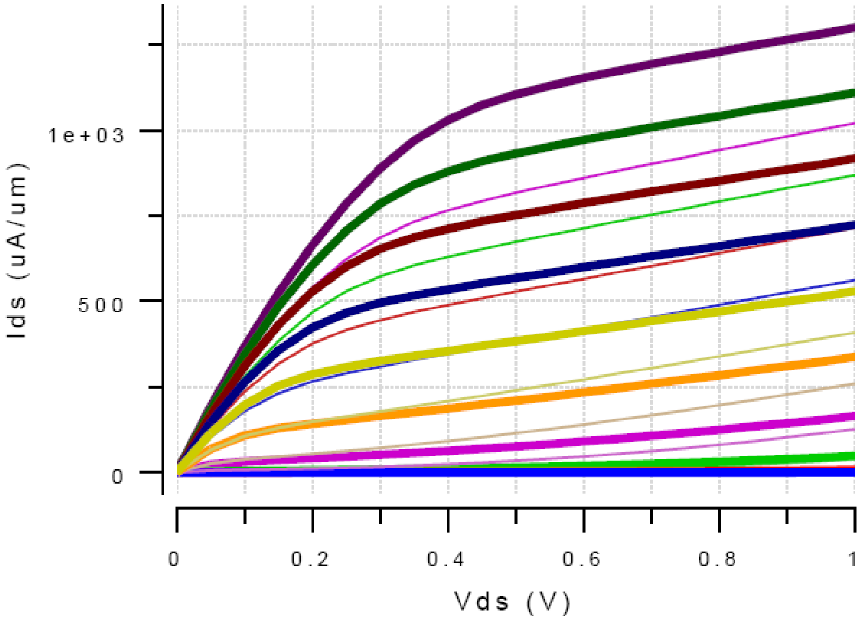
3) In EE-612, we will discuss the physics of MOSFETs and explain what controls key performance metrics like DIBL, subthreshold swing, etc. Use the nano-CMOS program in a “discovery” mode to determine which technology parameters (e.g. Leff, Vth, Vdd, Tox, Rdsw, Temperature) have the strongest effect on DIBL. You should use the 45nm NMOS device and develop a simple, logical way to explore the parameter space near the default values. Your final answer should be a list of the two technology parameters that have the biggest effect on DIBL and a brief description of the process you use to arrive at this conclusion.

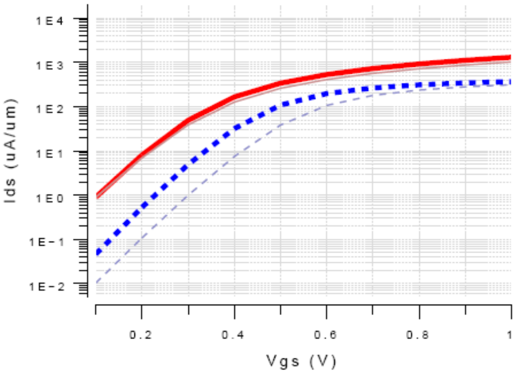
Question 3 Solution: Effect of device parameter changes

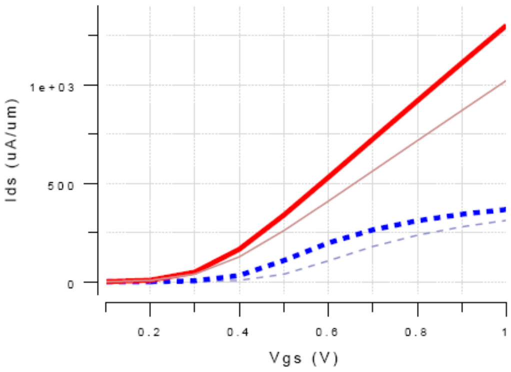
This problem requires us to run 5 different simulations. For each simulation, we present a table of results and then a brief discussion of the only the main changes that occurred.

45 nm PTM model seems to have a problem in Temperature dependence because of off current behavior. Therefore, full credits are given for the answer of Tox and Leff (or Temperature and Leff) if it is evidenced by simulation and discussion.

3a) Effect of increasing Tox (1.1nm-1.8nm):



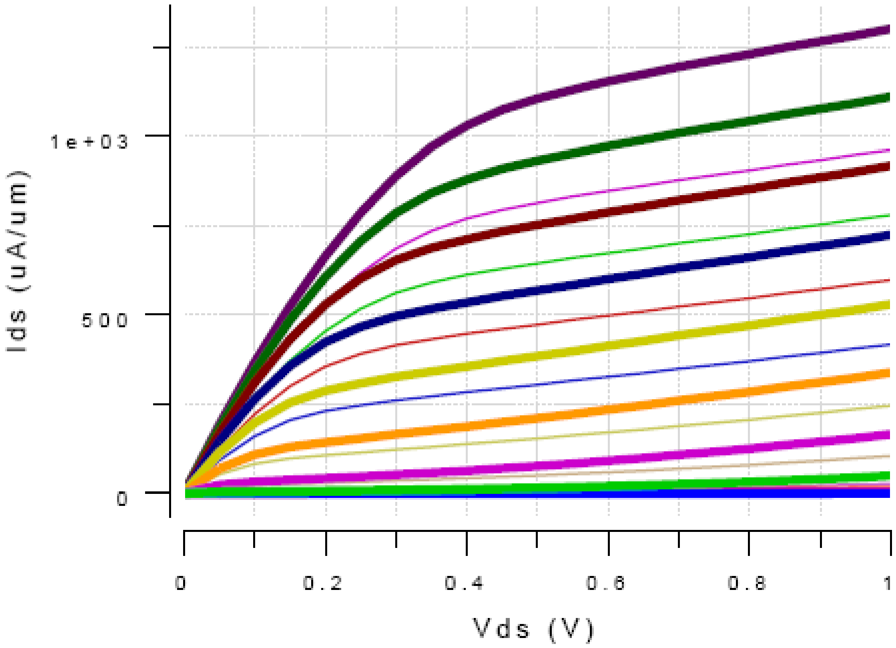


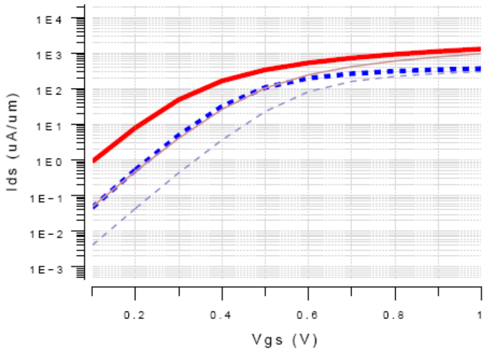


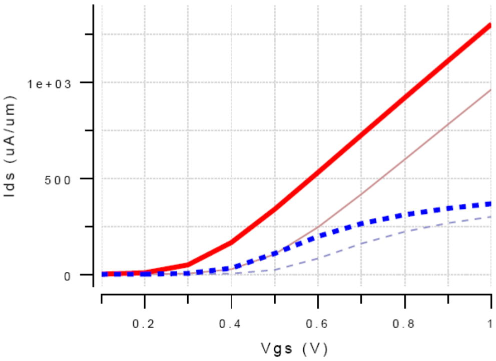
Question 3a Solution (cont.)

Device parameter	**NMOS - 45nm**		**Inc↑ /Dec↓**	**Remarks**
	T_{ox} 1.1 nm	**T_{ox} 1.8nm**		
I_{ON} (µA/µm)	1300	1020	↓	If T_{ox}↑, Oxide capacitance↓ so we have less charge and lower current.
SS (mV/dec)	140	140		
DIBL (mV/V)	166	200	↑	As T_{ox}↑ , 2D electrostatics gets worse, which increases DIBL. (Surprising that it did not increase SS too).
R_{ch} (Ω-µm)	285	320	↑	Less charge in the channel means high channel resistance.
g_m (mS/mm)	1900	1520	↓	Less inversion layer charge also means lower gm.
V_T (sat) (V)	0.32	0.32		
V_T (lin) (V)	0.38	0.45		According to MOS theory, a thicker oxide should give a higher V_T. That happens here, but not for V_T (sat), because the higher DIBL for V_T (sat) offsets the increase in V_T.

3b) Effect of increasing V_T:



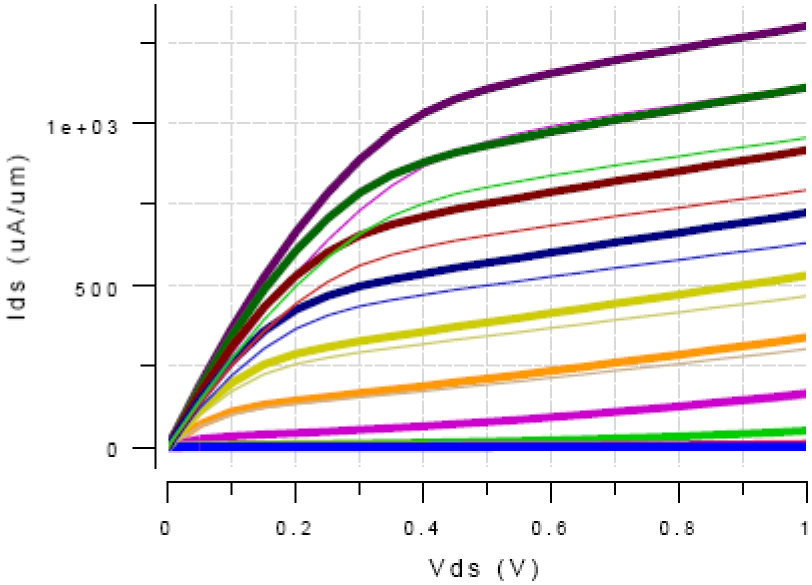


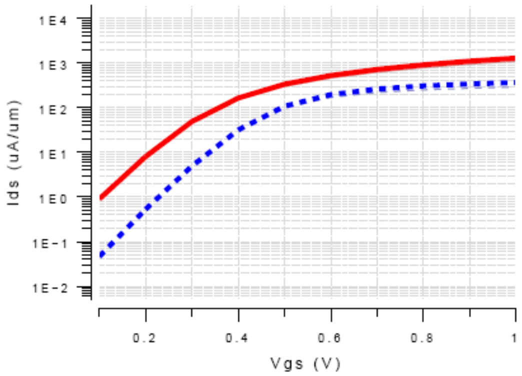


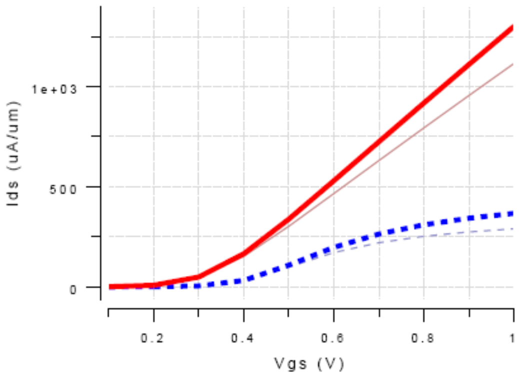
Question 3b Solution (cont.)

Device parameter	**NMOS - 45nm**		**Inc↑ /Dec↓**	**Remarks**
	V_T 0.25V	**V_T 0.4V**		
I_{ON} (µA/µm)	1300	962	↓	On current ~ ($V_G – V_T$), so it decreases as expected.
I_{OFF} (µA/µm)	0.9	0.05	↓	Off-current goes exponentially with V_T (~exp(-qV_T/mkT), so a small increase in V_T leads to a big reduction in off current.
SS (mV/dec)	140	140		
DIBL (mV/V)	166	130	↓	Higher V_{TH} is obtained by higher channel doping. This should improve 2D electrostatics and lower DIBL. It is surprising that it did not also lower SS.
R_O (Ω-µm)	2500	3448	↑	This is also a 2D effect. perhaps the high channel doping improves Ro too?
R_{ch} (Ω-µm)	285	354	↑	With increased V_T, there is less mobile charge in the channel, which increases resistance.
g_m (mS/mm)	1900	1820	↓	For complete velocity saturation, gm should be independent of V_T. It appears that velocity saturationis not complete.
V_T (sat) (V)	0.32	0.46	↑	Directly related to V_T
V_T (lin) (V)	0.38	0.48	↑	Directly related to V_T

3c) Effect of increasing R_{SD}:



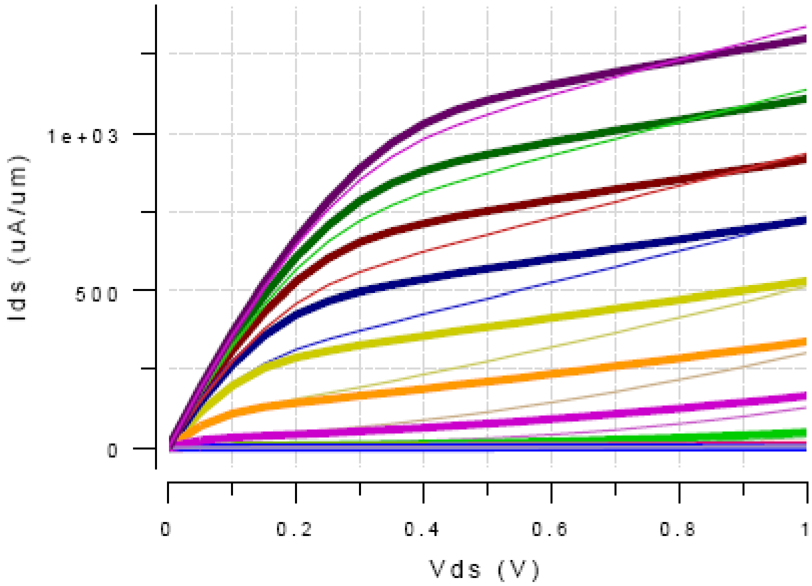


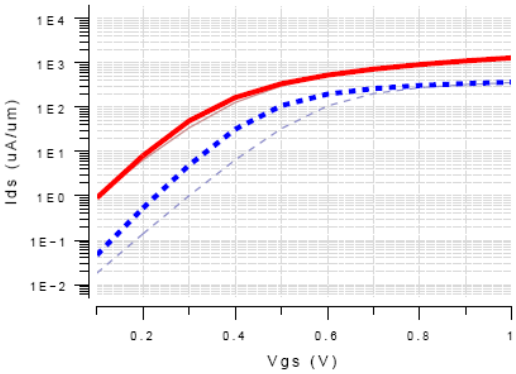


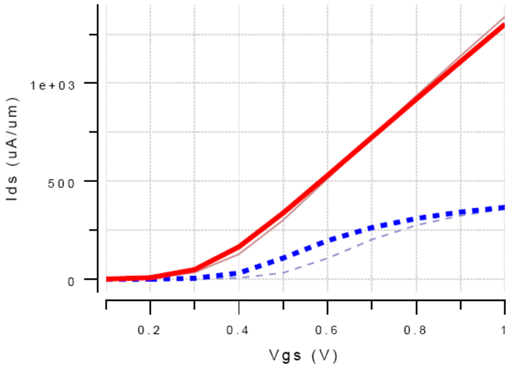
Question 3c Solution (cont.)

Device parameter	**NMOS - 45nm**		**Inc↑ /Dec↓**	**Remarks**
	R_{SD} 150 Ω-µm	**R_{SD} 220 Ω-µm**		
I_{ON} (µA/µm)	1300	1120	↓	Due to series resistance in the source and drain, a voltage drop occurs in the source and drain and therefore effective V_{GS} and V_{DS} are less than applied V_{GS}
R_O (Ω-µm)	2500	3333	↑	The increase is much more than the increase in R_{SD}. This is due to the negative feedback of the series resistors..
R_{ch} (Ω-µm)	333	374	↑	Resistances R_D, and R_S, are in series with R_{CH} and therefore total channel resistance (drain-source resistance) is sum of all three (R_S+R_D+R_{CH}).
g_m (mS/mm)	1900	1640	↓	The source and drain series resistances, which cannot be modulated by the gate voltage, will introduce a voltage drop between the gate and the source and drain contacts. These IR drops (source and drain) reduce the drain conductance as well as the transcoductance.

3d) Effect of increasing T

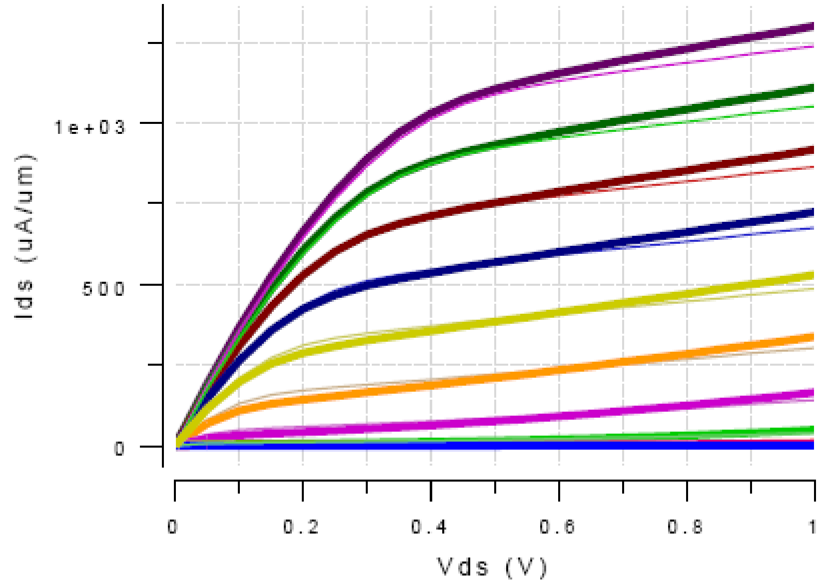


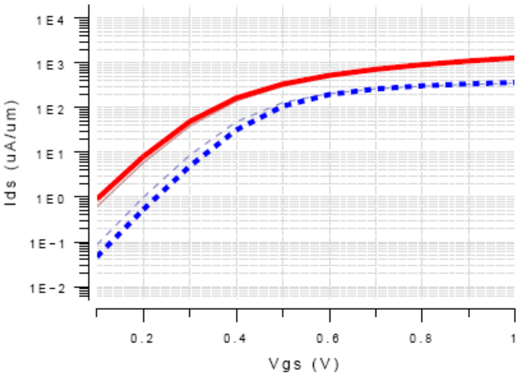


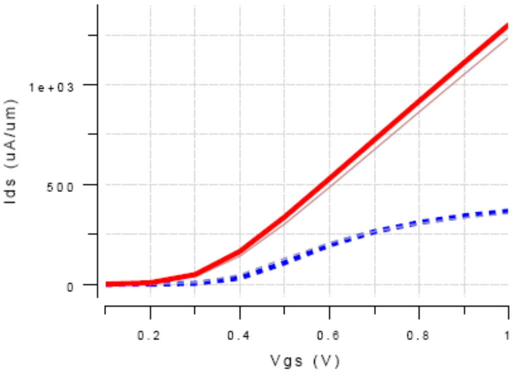


Device parameter	**NMOS - 45nm**		**Inc↑ /Dec↓**	**Remarks**
	T 300K	**T 425K**		
I_{OFF} (µA/µm)	0.9	0.98	↑	This is a surprise – we expect I_{OFF} to increase exponentially with temperature. This may be a problem with the model.

3e) Effect of increasing L_{eff}







Question 3e Solution (cont.)

Device parameter	**NMOS - 45nm**		**Inc↑ /Dec↓**	**Remarks**
	L_{eff} 35 nm	**L_{eff} 45 nm**		
I_{ON} (µA/µm)	1300	1240	↓	Longer channel lengths give lower channel fields, which lower current.
I_{OFF} (µA/µm)	0.9	0.6	↓	Longer channel lengths reduced 2D electrostatic effects, which lower IOFF.
SS (mV/dec)	140	190	↑	This is unexpected. Longer channels should improved 2D electrostatics and lower SS. May be a limitation of the model.
DIBL (mV/V)	166	80	↓	As expected, longer channels lave better DIBL.
R_O (Ω-µm)	2500	3333	↑	Output resistance is a short channel effect thast gets better for longer channels.