Fall 2008

EE 612: Nanoscale Transistors

HW3 SOLUTION: MOS Electrostatics (quantum)

In this assignment, you will examine the effects of quantum confinement on an MOS capacitor by re-doing the analysis of the 45 nm node device that was the subject of HW2. You will use the program, Schred, which solves the Schrödinger equation self-consistently with Poisson's equation (Schred is available on the nanoHUB, www.nanohub.org). Familiarize yourself with Schred by running a simulation with default parameters and examining the output plots. Then you are ready to proceed with the homework assignment.

For these exercises, assume:

$N_A = 2.7 \times 10^{18}$ cm^{-3} for the bulk doping
$EOT = 1.1$ nm
$Q_F = 0.0$
$T = 300$K
$V_{DD} = 1.0$ V

Modify the Schred input to perform a ***quantum mechanical*** MOS C-V simulation for this device for $-2 \le V_G \le 2$ V. You should consider three different gate electrodes: polysilicon doped at 1 x 10^{20} cm^{-3}, polysilicon doped at 1.5 x 10^{20} cm^{-3}, and a metal gate with a workfunction corresponding to a polysilicon gate with $E_F - E_C$.

Solution: Schred parameters used:

Device parameters

Device structure:	Bulk MOS
Oxide thickness:	1.1 nm
Oxide dielectric constant:	3.9
Substrate doping:	2.7e18 /cm^3
Polysilicon gate doping:	-1e20 /cm^3
Metal workfunction:	4.05 eV
Acceptor ionization energy:	0.05 eV
Donor ionization energy:	0.05 eV

Environment parameters

Ambient temperature:	300 K
Minimum Voltage:	-2 V
Maximum Voltage:	2 V
Step Voltage:	0.05 V

Models and plots

Charge model:	Quantum mechanical
Carrier statistics:	Fermi Dirac
Partial Ionization:	No
Exchange interaction:	No
Unprimed subbands:	4
Primed subbands:	2
Quantum Calculation in Accumulation Region	No

1) Determine the equivalent electrical oxide thickness (EOT_{elec}) at V_G=1.0V for each of the three cases, and compare them to the value obtained in HW2.

Solution:

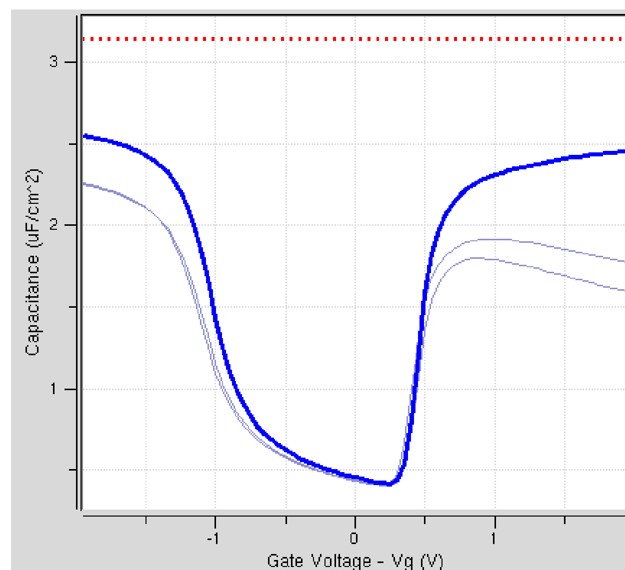

Fig. 1: MOS *C-V* curves for 3 different gates using quantum mechanical charge model

For the on-state, $V_G = V_{DD} = 1.0$ V.
At this gate voltage, the gate capacitance ($C_G(inv)$) is read from the *C-V* plot. The equivalent electrical oxide thickness (EOT_{elec}) is then obtained by $EOT_{elec} = \varepsilon_{ox} / C_G(inv)$

	$C_G(inv)$ (from plot)	EOT_{elec}
Metal gate (Work function: 4.05eV)	2.31 μF/cm^2	1.49 nm
N+ poly gate (1e20 /cm^3)	1.79 μF/cm^2	1.93 nm
N+ poly gate (1.5e20 /cm^3)	1.92 μF/cm^2	1.80 nm
HW 2 (N+ poly gate, classical simulation):	2.99 μF/cm^2	1.15 nm

Perform a second simulation that does a ***classical analysis*** for N_P = 1e20 cm^{-3}.

2) Compare the quantum mechanical and classical C-V curves and discuss the differences.

Solution:

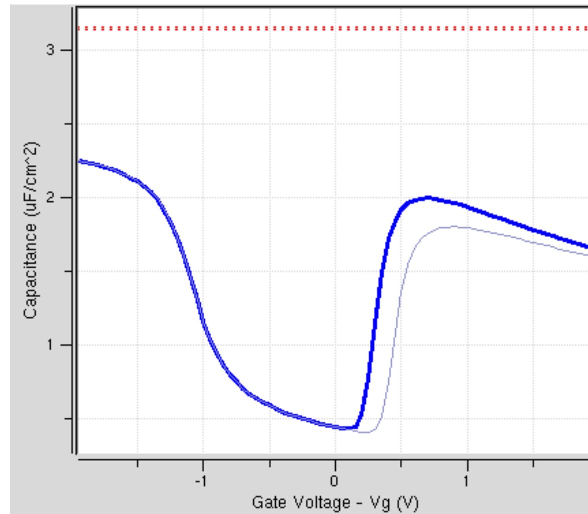

Fig. 2: MOS *C-V* curves for Polysilicon gate, quantum mechanical and classical (bold) model

V_T is increased and the gate capacitance in inversion is lower for the quantum mechanical model because of quantum confinement and because the electron density peak is away from the surface.

3) Determine the threshold voltage shift due to quantum mechanical confinement and compare it to the value that you would get from Fig. 4.17 and eqn. (4.57) on p. 198 of Taur and Ning.

Solution:

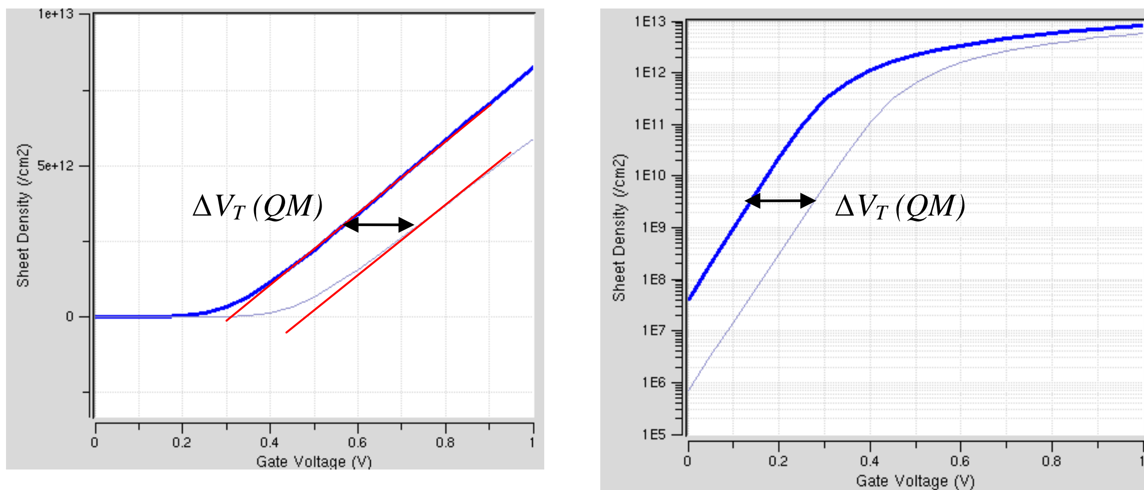

Fig 3: Linear and semilog plots of charge sheet density vs. gate voltage for classical (bold curve) and quantum mechanical inversion charge model.

Subthreshold slope, $S = 76$ mV/decade, (from Fig. 3).
Body-effect coefficient, $m = S/60 = 1.26$.
E_S (at $C_G = C_{min}$) = 9e5 V/cm.
From fig 4.17 of text, Surface potential shift: 0.12V.
From eq 4.57 of text, calculated value of $\Delta V_T = 150$ mV
From semilog charge sheet density plot (Fig. 3), $\Delta V_T = 140$ mV (close to theory.)

4) For the on-state ($V_G = V_{DD}$) compare the quantum mechanical and classical electron density profiles.

Solution:

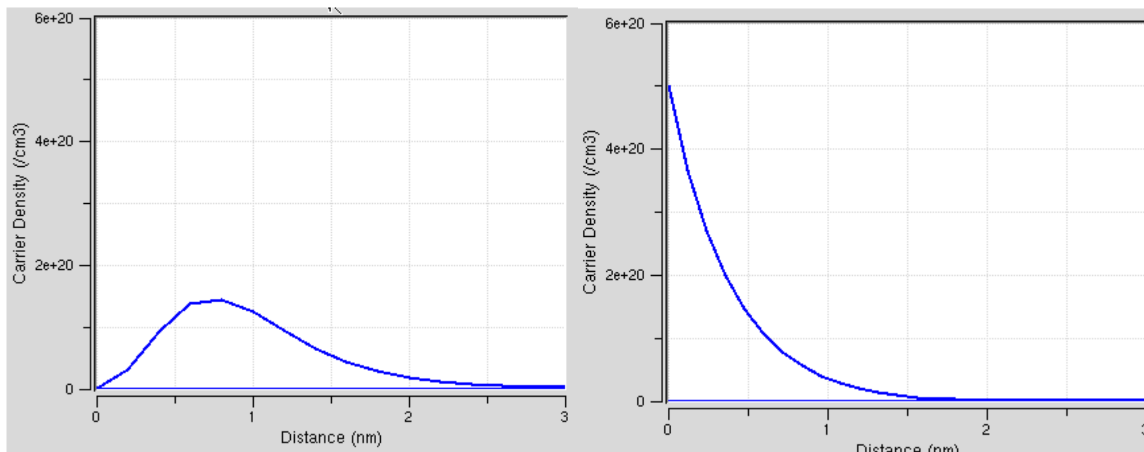

Fig 4: electron density profile for quantum mechanical and classical model

The inversion charge distribution is plotted in fig 4. Note that the peak electron density for the quantum mechanical model is at 0.8 nm away from the silicon – insulator interface, unlike the classical model where it peaks at the interface. This lowers the inversion layer capacitance in series with the gate insulator capacitance.

5) How much does poly depletion increase EOT_{elec} when $N_P = 1.0 \times 10^{20}$ cm^{-3}?

Solution: Change in EOT_{elec} due to poly depletion:

$$(EOT_{elec})_{\text{poly (1e20)}} - (EOT_{elec})_{\text{metal}} = 1.93 - 1.49 = 0.44 \text{ nm}$$

6) How much does the inversion layer thickness increase EOT_{elec} when $N_P = 1.0 \times 10^{20}$ cm^{-3}?

Solution: Change in EOT_{elec} due to inversion layer thickness:

$$(EOT_{elec})_{\text{metal}} - EOT = 1.49 - 1.1 = 0.39 \text{ nm}$$