

Fall 2008

EE 612: Nanoscale Transistors

HW7: DUE TUESDAY, OCTOBER 28, 2008

Two-Dimensional Electrostatics

Controlling 2D electrostatics is a key challenge for MOSFET device designers. This exercise will give you some “experience” to help you develop an intuitive feel for how two-dimensional electrostatics affects the IV characteristics of a nanoscale MOSFET using the simulation tool “MOSFET” on nanoHUB.org.

To begin, you should specify a MOSFET as follows.

$N_A = 1.0 \times 10^{18} \text{ cm}^{-3}$ for the channel doping
 $N_A = 1.0 \times 10^{17} \text{ cm}^{-3}$ for the substrate doping
Oxide thickness = 2.0 nm
 $Q_F = 0.0$
 $T = 300\text{K}$
 $V_{DD} = 1.5\text{V}$
Assume an n⁺ polysilicon gate
Select “Gaussian S/D doping density”
Specify a channel length of 75 nm.
Specify a S/D length of 100nm

For other parameters, you can use default values.

- 1) Run a MOSFET simulation and compute the subthreshold swing, DIBL, and threshold voltage.

Examine the plots from the simulation and select one plot of an internal device quantity that best illustrates why this device behaves so well. Explain.

- 2) Re-run the simulation with the original input parameters, but this time, reduce the channel length to 30 nm. Compute the subthreshold swing, DIBL, and threshold voltage and compare them to the original values. You should find that the performance of the device has degraded. Using the same plot you selected for part 1), explain why the performance has degraded.

- 3) Construct a plot of threshold voltage vs. channel length for this device. (You will need to run simulations with several different channel lengths.) You should find that V_T is independent of channel length for $L > L_{MIN}$. Determine L_{MIN} .
- 4) Re-run the simulation with the original input parameters, but this time increase the oxide thickness. Beginning with 2nm oxide thickness, compute the subthreshold swing and DIBL, then increase the oxide thickness and repeat. Continue until SS and DIBL begin to increase significantly. When SS and DIBL have degraded, examine the same plot you selected for part 1) to explain why the performance has degraded. To keep $DIBL < 100$ mV/V, L/t_{ox} should be greater than some ratio. What is that ratio?
- 5) Re-run the simulation of part 2), but this time, select “Gaussian S/D and HALO Doping Density.” Compare the IV characteristics to those of part 2). Using the same plot of an internal device quantity you used in parts 1) and 2), explain why the performance has improved. Finally, select a plot or plots to explain exactly what “halo” doping is.
- 6) For the device of part 5), construct a plot of threshold voltage vs. channel length. Compare the results to those of part 3).