

Fall 2008

EE 612: Nanoscale Transistors

**HW8: DUE TUESDAY, NOVEMBER 4**

**SELECTED MOSFET PROBLEMS**

- 1) Problem 4.6 in Taur and Ning.
- 2) Problem 4.7 in Taur and Ning.
- 3) Problem 4.8 in Taur and Ning.
- 4) A sketch of a MOSFET from an older generation technology is attached. Update this sketch from the 2007 edition of the International Roadmap for Semiconductors. See <http://www.itrs.net> and look for ITRS Edition Reports and select 2007 Edition. For this problem, we will only consider the NMOS high-performance (HP) device and only the the “Extended Planar Bulk” device.

You should produce a figure for the 2012 technology node like that for the attached figure. You can find the numbers you will need in two tables of the ITRS: Table PIDS2a in the chapter, “Process Integration, Devices, and Structures” and Table FEP4a in “Front End Process.”

You should find the following device parameter values, list the numerical values, and indicate them on your sketch:

- Physical gate length
- Equivalent electrical oxide thickness (and EOT<sub>electrical</sub>)
- Maximum gate leakage current density
- Power supply voltage
- Saturation threshold voltage
- Off-current
- On-current
- Parasitic source-drain resistance
- Intrinsic gate capacitance
- Parasitic gate capacitance
- Drain extension junction depth
- Drain extension junction sheet resistance
- Lateral abruptness of drain extension
- Contact junction depth
- Allowable junction leakage current
- Sidewall spacer thickness

Metal-semiconductor contact resistance in  $\Omega\text{-cm}^2$   
Contact silicide sheet resistance  
Channel doping concentration  
Shallow trench isolation depth

5) For the 2010 planar bulk N-MOSFET compute:

The on-current / off-current ratio

The ratio of the source resistance to the total resistance (device on resistance plus  $R_S$ )

The ratio of the parasitic gate capacitance to the total gate capacitance

The estimated inversion layer density per  $\text{cm}^2$  under on-current conditions

The estimated velocity at the beginning of the channel under on-current conditions

The estimated resistance of the source/drain extension

# MOSFET Architecture at the 180 nm Technology Node

(From the 1997 National Technology Roadmap for Semiconductors)

