EE-612 FINAL EXAM: Fall 2008 December 15, 2008

NAME KEY ID # ____________

This exam consists of **four** questions – each is divided into several parts. Following each problem, there is a sheet of scratch paper that you may use. **Do not remove this scratch paper from the exam.**

You are permitted to use a calculator, and you will need one.

You will be asked a series of questions that require you to perform some simple calculations. These are the kind of quick calculations that a device engineer should be able to do. If you find yourself doing a complicated analysis, you are not approaching the problem correctly. There may be a term or two that you cannot recall the definition of, but you should be able to figure out what is meant from the context of the question.

The last page is a formula sheet, which you may remove.

Be sure to clearly identify your answers and to show all of your work.

It is important that you CLEARLY show your work and that the final answer is CLEARLY marked. You may wish to use the scratch paper to get started, and then transfer the key results to the exam itself.

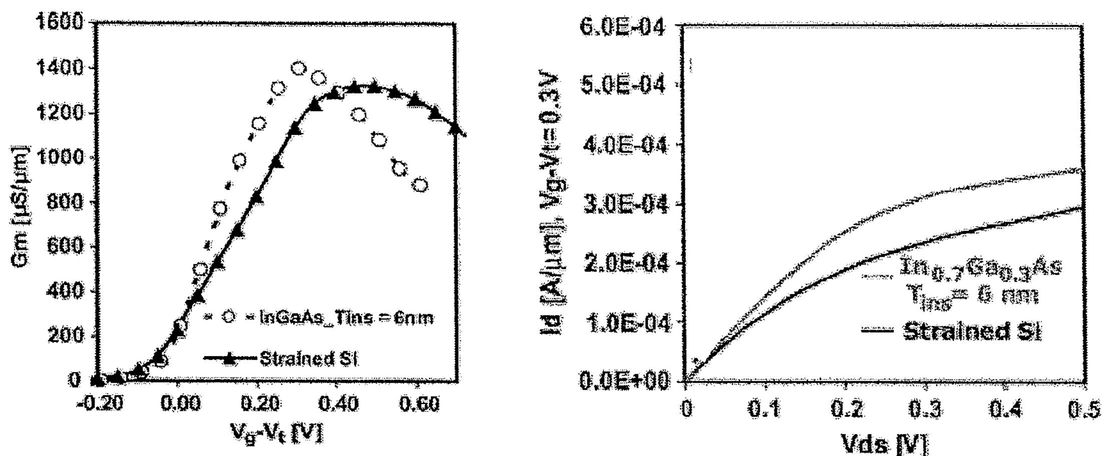
If I have trouble identifying your final answer and how you got it, the problems is yours, and there will be NO REGRADES. You will receive no credit for your answer, unless it is clear how you obtained the answer.

PROBLEM WEIGHTING:

Problem 1:	**10 parts**	**10 points each**	**100 points total**
Problem 2:	**3 parts**	**10 points each**	**30 points total.**
Problem 3:	**2 parts**	**10 points each**	**20 points total.**
Problem 4:	**5 parts**	**10 points each**	**50 points total**
Total:			**200 points**

Problem I

Problem 1) consists of 10 questions about a III-V heterostructure FET recently reported by Intel. In this device, the channel is an $In_{0.7}Ga_{0.3}As$ quantum well and the "insulator" is a wide bandgap AlInAs layer with a physical thickness of 6 nm (dielectric constant of $\kappa = 12.7$). The channel length is 80 nm, and the estimated series resistance of this device is $R_{SD} = 580\ \Omega$-μm. The gate capacitance (the insulator capacitance in series with the semiconductor capacitance is 0.9×10^{-6} F/cm^2. The room temperature transconductance vs. V_{GS}-V_T with $V_{DS} = 0.5$V is shown below. Also shown is the measured I_D vs. V_{DS} characteristic for $V_{GS} - V_T = 0.3$V. For the purposes of this problem, you should assume that this device operates just like a MOSFET. Clearly **explain** how you get each answer.



From: Gilbert Dewey, Mantu K. Hudait, Kangho Lee, Ravi Pillarisetty, Willy Rachmady, Marko Radosavljevic, Titash Rakshit, and Robert Chau, "Carrier Transport in High-Mobility III–V Quantum-Well Transistors and Performance Impact for High-Speed Low-Power Logic Applications," *IEEE Electron Device Letters*, Vol. 29, No. 10, pp. 1094 – 1097, October, 2008

1a) For MOSFETs, we talk about Tinv or $EOT_{electrical}$. For this device, determine the analogous quantity, the effective electrical thickness of the insulator assuming $\kappa = 12.7$.

$$C_G \equiv \frac{\epsilon_{ins}}{T_{inv}} = 9 \times 10^{-7}\ F/cm^2$$

$$T_{inv} = \frac{12.7 \times 8.854 \times 10^{-14}}{9 \times 10^{-7}} = 12.5\,nm$$

full credit for

$$EOT = \frac{3.9}{12.7} \times 6\,nm$$

Problem I (continued)

1b) If the "insulator" thickness of this device were reduced to 2nm, what would the total gate capacitance (insulator capacitance in series with the semiconductor capacitance) be?

$$\frac{1}{C_G} = \frac{1}{C_{ins}} + \frac{1}{C_S}$$ assume on-current (strong inv) conditions

for $T_{ins} = 6nm$: $C_{ins} = \epsilon_{ins}/6nm = 1.87\times10^{-6}$

$$\frac{1}{C_S} = \frac{1}{9\times10^{-7}} - \frac{1}{1.87\times10^{-6}} \rightarrow C_S = 1.74\times10^{-6}\ F/cm^2$$

for $T_{ins} = 2nm$: $C_{ins} = \epsilon_{ins}/2nm = 5.62\times10^{-6}$

assume C_S does not change

$$\frac{1}{C_G} = \frac{1}{5.62\times10^{-6}} + \frac{1}{1.74\times10^{-6}} \rightarrow C_G = 1.33\times10^{-6}\ F/cm^2$$

1c) ~~According to your textbook, the intrinsic transconductance, g_m^i (without series resistance)~~ is related to the extrinsic transconductance, g_m^{ex} (with series resistance) by

$$g_m^i = \frac{g_m^{ex}}{1 - g_m^{ex} R_S - g_{ds}\left(R_S + R_D\right)}.$$

Use this expression to deduce the peak, intrinsic transconductance of the Tins = 6nm InGaAs FET.

$g_m^{ex} \simeq 1400\ \mu S/\mu m$

$R_S + R_D = 580$

$R_S = 580/2$

$$g_{ds} = \left.\frac{\Delta I_D}{\Delta V_{DS}}\right|_{V_G=0.3} = \frac{3.5\times10^{-4} - 2.5\times10^{-4}}{0.5} = 2\times10^{-4}\ \Omega^{-1}\text{-}\mu m$$

$$g_m^i \simeq \frac{1400\times10^{-6}}{1 - 1400\times10^{-6}\cdot\frac{580}{2} - 200\times10^{-6}\times580}$$

$\simeq 2950\ \mu S/\mu m$

Problem I (continued)

1d) Use the peak, intrinsic transconductance of the Tins = 6nm FET to estimate the average velocity for the InGaAs FET. (If you were not able to determine g_m^i, then use g_m^{ex}.) List your assumptions.

$$I_D = W C_G (V_G - V_T) \langle v \rangle$$

$$\frac{\partial I_D}{\partial V_G} = g_m = W C_G \langle v \rangle$$ assumes $\langle v \rangle \neq f(V_G)$

$$\langle v \rangle = \frac{g_m^i}{W C_G} = \frac{2950 \times 10^{-6}}{10^{-4} \times 9 \times 10^{-7}} \text{ cm/s}$$ assumes $W = 1 \mu m$

$$= 3.2 \times 10^7 \text{ cm/s}$$

/

1e) The average velocity can also be estimated from the on-current. Do so and compare your answer for the Tins = 6nm FET to the answer in part ~~c~~ 1d). List your assumptions.

$$I_{ON} = W C_G (V_G - V_T) \langle v \rangle$$

$I_{ON} = 3.5 \times 10^{-4}$, $W = 10^{-4}$, $C_G = 9 \times 10^{-7}$

$(V_G - V_T) \rightarrow V_G - V_T - I_D R_S$

$$0.3 - 3.5 \times 10^{-4} \times \frac{580}{2} = 0.2$$

$$\langle v \rangle = \frac{3.5 \times 10^{-4}}{10^{-4} \cdot 9 \times 10^{-7} \times 0.2} = 1.94 \times 10^7 \text{ cm/s}$$ lower than 1d

in contrast to 1d) no assumptions → more reliable answer

Problem I (continued)

1f) Estimate the channel resistance for the intrinsic Tins = 6nm InGaAs FET.

from the plot:

$$R_{TOT} = \frac{0.1V}{1.3\times10^{-4}A} = 769\ \Omega\text{-}\mu m = R_{ch} + R_{SD}$$

$$R_{CH} = 769 - 580 = \boxed{189\ \Omega\text{-}\mu m}$$

1g) Use the estimated channel resistance to deduce the mobility for the Tins = 6nm InGaAs FET and compare it to the measured, bulk mobility of 10,000 cm^2/V-s.

$$I_D = \frac{W}{L}\mu_{eff} C_G (V_G' - V_T) V_D$$

$$\mu_{eff} = \frac{L}{W C_G (V_G' - V_T) R_{CH}}$$

$$= \frac{80\times10^{-7}}{10^{-4}\cdot 9\times10^{-7}\cdot 0.26}$$

$$= 1810\ cm^2/V\text{-}s$$

$$V_G - I_D R_S - V_T$$

$$= 0.3 - 1.3\times10^{-4}\cdot\frac{580}{2}$$

$$= 0.26V$$

Problem I (continued)

1h) Assume that the series resistance of this device could be reduced so that its effect was negligible and that the "insulator" thickness could be reduced to 2 nm. What inversion layer density would result? Assume $V_G - V_T = 0.3\ V$

from 1b) $C_G = 1.33 \times 10^{-6}$

$$N_i = \frac{C_G (V_G - V_T)}{q} = \frac{1.33 \times 10^{-6} (0.3)}{1.6 \times 10^{-19}} = 2.5 \times 10^{12}\ cm^{-2}$$

1i) If we wanted to use the InGaAs for RF applications, we would want to know the "self-gain." Using values from the two figures, estimate the self-gain for the Tins = 6nm device.

$$A_{vi} = -g_m / g_{ds} \simeq \frac{1400 \times 10^{-6}}{200 \times 10^{-6}} \simeq 7$$

(200 × 10⁻⁶ from part 1c)

1j) If we wanted to use the InGaAs for RF applications, we would also want to know the gain-bandwidth product, f_T. Estimate f_T for the Tins = 6nm InGaAs device. HINT: you may wish to use a quantity that you computed earlier.

Two ways

$$f_T \simeq \frac{g_m}{2\pi C_G} \qquad f_T \simeq \frac{1}{2\pi t_t} \qquad t_t = \frac{L}{\langle v \rangle}$$

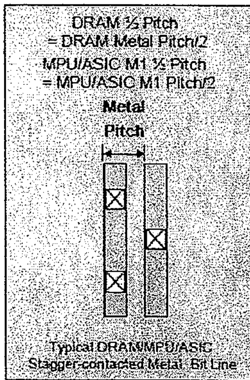
$$\simeq \frac{1400 \times 10^{-6}}{2\pi \cdot 9 \times 10^{-7} \cdot W \cdot L} = 309\ GHz$$

Problem II

The 2007 Edition of the ITRS lists the following parameters for the 2007 global wiring layer:

Minimum global wiring pitch:	210 nm
Global wiring A/R (for Cu):	2.3
Capacitance per unit length for global wires	2.2 pF/cm
Effective resistivity of minimum pitch global Cu wire:	2.73 μΩ-cm

The ITRS Executive Summary provides the figure below.



You should also recall that: $\tau_w = 0.5 R_L C_L L_w^2$

2a) Using the information provided above, determine the resistance per unit length of the minimum pitch Cu global wire in Ω/cm.

$$R = \rho \frac{L}{A_w} = \frac{\rho}{A_w} \cdot L \qquad R_L = \frac{\rho}{A_w} \ \Omega/cm$$

$$A_w = \frac{210 \times 10^{-7}}{2} \times \frac{2.3 \times 210 \times 10^{-7}}{2}$$

$$= 2.54 \times 10^{-10}\ cm^2$$

$$R_L = \frac{2.73 \times 10^{-6}}{2.54 \times 10^{-10}} = 1.08 \times 10^{4}\ \Omega/cm$$

2b) Compute the delay of a 1 mm long minimum pitch global Cu wire.

$$\tau_w = \frac{1}{2}(1.08\times10^4)(2.2\times10^{-12})(10^{-1})^2$$

$$\doteq 119\ ps$$

2c) The expression, $\tau_w = 0.5 R_L C_L L_w^2$, cannot be used when the wire is too short. Explain why it cannot be used.

this expression describes a signal "diffusing" across an interconnect. It cannot "diffuse" faster than the speed of light.

Problem III

The 2007 Edition of the ITRS lists the following parameters for the high performance, planar, bulk MOSFET at 2012 as:

Physical gate length:	14nm
Rsd:	180 Ω-μm
Drain extension Xj:	7nm
Drain extension sheet resistance:	1160 Ω/square
Contact maximum resistivity	5.6E-08 Ω-cm^2

3a) Using the information provided and the fact that the electron mobility in heavily doped silicon is about 100 cm^2/V-s, estimate the necessary doping density for the drain extension.

$$\rho_{ext} = \frac{\rho(\Omega\text{-cm})}{x_j} = \frac{1}{N_D q \mu_n x_j}$$

$$N_D = \frac{1}{q\mu_n x_j} \cdot \frac{1}{\rho_{ext}} = \frac{1}{1.6\times10^{-19} \cdot 100 \cdot 7\times10^{-7} \cdot 1160}$$

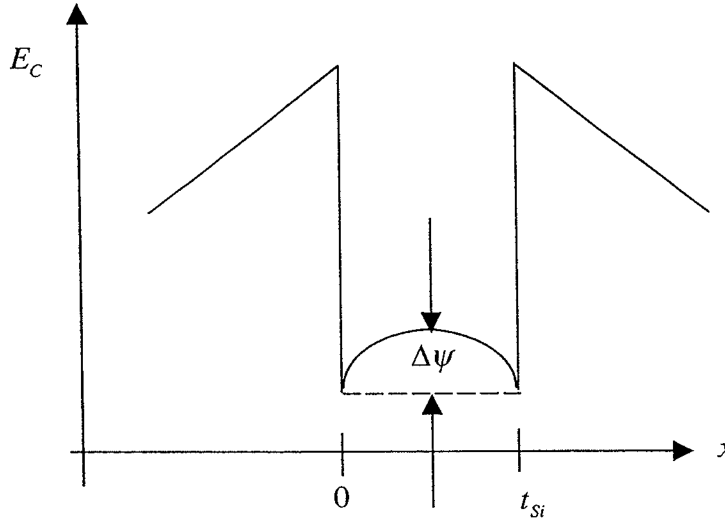
$$= 7.7\times10^{19}\ /\text{cm}^3$$

3b) Assume that the silicided contact is 72 nm long (in the direction of current flow, and then estimate the part of the series resistance due to the silicide-silicon contact resistance (in Ω-μm).

$$R_C = \frac{\rho_c}{A_c} = \frac{5.6\times10^{-8}}{72\times10^{-7}\cdot10^{-4}} = 78\,\Omega$$

Problem IV

This problem concerns a fully depleted, double gate structure as shown below. Under some conditions, the potential drop, $\Delta\psi$, within the undoped silicon film is small, and the structure is "volume inverted." Under other conditions, $\Delta\psi$ is large, and separate inversion layers form at the top and bottom of the silicon film. The purpose of this problem is to gain some insight into what controls $\Delta\psi$ and how the magnitude of $\Delta\psi$ determines whether or not structure is volume inverted.

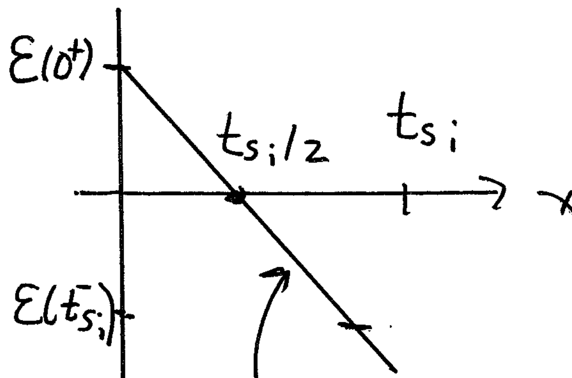


In general, the inversion layer electrons are distributed non-uniformly across the silicon body, but for this problem, we will assume that the total inversion layer charge, Q_I is distributed uniformly from 0 to t_{Si}.

4a) Assume that the device in biased in strong inversion, and sketch the electric field from 0 to t_{Si}.

$$\Rightarrow \rho(x) \simeq \frac{Q_I(x)}{t_{Si}} \simeq \text{constant}$$

$$\frac{d\mathcal{E}}{dx} = \frac{\rho}{\epsilon_{Si}} \simeq \text{constant} < 0$$



$$\frac{d\mathcal{E}}{dx} = \frac{Q_I}{t_{Si}\epsilon_{Si}}$$

IV) continued

4b) Give an expression for $E(0^+)$ and $E(t_{Si}^-)$ in terms of the total inversion layer charge in the silicon, Q_I.

$$\frac{d\mathcal{E}}{dx} = \frac{Q_I}{t_{Si}\epsilon_{Si}}$$

$$\int_{\mathcal{E}(0^+)}^{\mathcal{E}(t_{Si}^-)} d\mathcal{E} = \frac{Q_I}{t_{Si}\epsilon_{Si}} \int_0^{t_{Si}} dx$$

$$\mathcal{E}(t_{Si}^-) - \mathcal{E}(0^+) = \frac{Q_I}{\epsilon_{Si}}$$

by symmetry

$$\mathcal{E}(0^+) = -\mathcal{E}(t_{Si}^-)$$

$$\Rightarrow \mathcal{E}(0^+) = -\mathcal{E}(t_{Si}^-) = -\frac{Q_I}{2\epsilon_{Si}}$$

4c) Develop an expression for $\Delta\psi$.

$$\Delta\psi = \frac{1}{2} \cdot \mathcal{E}(0^+) \cdot \frac{t_{Si}}{2}$$

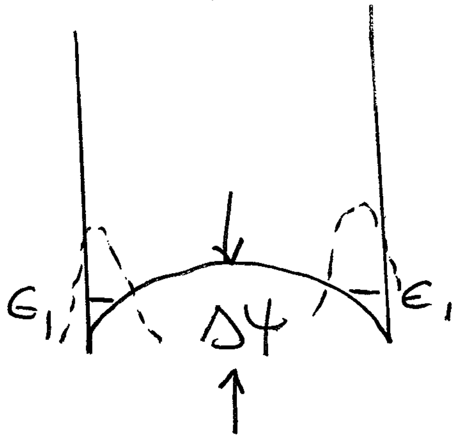
$$= \frac{t_{Si}}{4} \times \left(-\frac{Q_I}{2\epsilon_{Si}}\right)$$

$$= -\frac{Q_I t_{Si}}{8\epsilon_{Si}}$$

IV) continued

4d) One can argue, that for volume inversion to occur, we should require $q\Delta\psi > \varepsilon_n$ (handwritten correction: $<$) where $\varepsilon_n = \hbar^2 n^2 \pi^2 / 2m^* t_{Si}^2$. Explain why this is a reasonable argument.

what happens if $q\Delta\psi > \epsilon_1$?



if $\Delta\psi$ too big, wavefunction will be localized near each interface, so

$\Delta\psi < \dfrac{\epsilon_1}{q}$ for volume inversion

4e) Develop an expression that shows when volume inversion occurs and use your expression to explain ~~why it occurs for very high gate voltages or for very thin silicon bodies.~~ when it occurs.

$$\Delta\psi < \epsilon_1$$

$$\frac{|Q_I| t_{Si}}{8\epsilon_{Si}} < \frac{\hbar^2 \cdot 1^2 \pi^2}{2m^* t_{Si}^2} \Rightarrow \boxed{|Q_I| t_{Si}^3 < \frac{4\epsilon_{Si} \hbar^2 \pi^2}{m^*}}$$

when $\Delta\psi$ is large, volume inversion does not occur. This can happen in two ways:

1) large $|Q_I|$ (V_G) which gives a high electric field and therefore a large $\Delta\psi$.

2) large t_{Si}, which gives a bigger $\Delta\psi$.