

5.1

from eq 5.3 & 5.4

$$\tau = \frac{C V_{dd}}{4} \left(\frac{1}{\omega_n I_{nsat}} + \frac{1}{\omega_p I_{psat}} \right) \quad \text{--- (1)}$$

$$C = k (\omega_n + \omega_p) \quad \text{--- (2)}$$

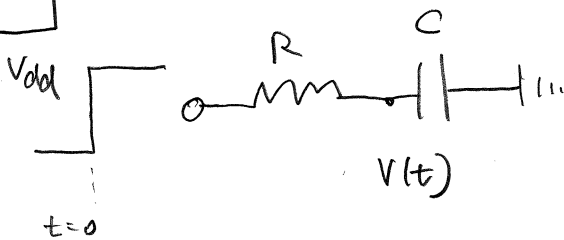
from (1) and (2),

$$\begin{aligned} \tau &= \frac{k V_{dd}}{4} \left(\frac{\omega_n + \omega_p}{\omega_n I_{nsat}} + \frac{\omega_n + \omega_p}{\omega_p I_{psat}} \right) \\ &= " \left(\frac{1}{I_{nsat}} + \frac{1}{I_{psat}} + \frac{1}{I_{nsat}} (\omega_p / \omega_n) + \frac{1}{I_{psat}} (\omega_p / \omega_n) \right) \end{aligned}$$

min. delay occurs when the last two terms are equal.

$$\therefore \omega_p / \omega_n = (I_{nsat} / I_{psat})^{1/2}$$

5.2



$$V_{dd} = V(t) + I(t)R = V(t) + RC \frac{dV(t)}{dt}$$

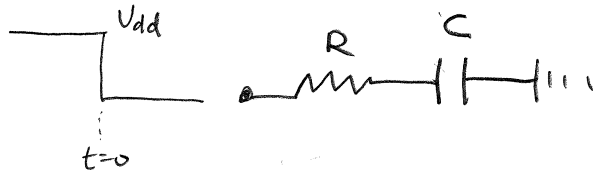
$$V(t) = V_{dd} (1 - e^{-t/RC})$$

$$E_{diss} = \int_0^{\infty} I^2 R dt = \int_0^{\infty} \left(\frac{V_{dd} - V(t)}{R} \right)^2 R dt = \frac{V_{dd}^2}{R} \int_0^{\infty} dt e^{-2t/RC} = \frac{1}{2} C V_{dd}^2$$

E_{diss} is independent of R .

$$E_{\text{stor}} = \int_0^{V_{\text{dd}}} Q dV = C \int_0^{V_{\text{dd}}} V \cdot dV = \frac{1}{2} C V_{\text{dd}}^2.$$

Now switch to 0.



$$0 = V(t) + RC \frac{dV}{dt}, \quad V = V_{\text{dd}} e^{-t/RC}$$

$$E = \int_0^{\infty} RI^2 dt = \frac{V_{\text{dd}}^2}{R} \int_0^{\infty} e^{-2t/RC} dt = \frac{1}{2} C V_{\text{dd}}^2$$

The energy stored in capacitor is dissipated in R

5.7

$$\tau = C_L + C_{\text{out}} \quad - \text{eq 5.35}$$

$$\tau_{\text{bmin}} = 2C_{\text{out}} + 2\sqrt{C_{\text{in}}C_L} \quad - \text{eq 5.37}$$

$$\text{if } \tau > \tau_{\text{bmin}} \Rightarrow C_L + C_{\text{out}} > 2C_{\text{out}} + 2\sqrt{C_{\text{in}}C_L}$$

$$\therefore C_L > (\sqrt{C_{\text{in}}} + \sqrt{C_{\text{in}} + C_{\text{out}}})^2$$

Buffer help reduce the delay under this condition

5.8

the width of the successive buffer : k_1, k_2, \dots, k_n

switching resistance : $R_{sw}, R_{sw}/k_1, R_{sw}/(k_1 k_2), \dots$

output capacitance : $C_{out}, k_1 C_{out}, k_1 k_2 C_{out}, \dots$

input capacitance : $k_1 C_{in}, k_1 k_2 C_{in}, \dots$

the delay of the n-th stage

$$\tau_{b,n} = \frac{R_{sw}}{k_1 k_2 \dots k_{n-1}} (k_1 k_2 \dots k_{n-1} C_{out} + k_1 k_2 \dots k_n C_{in})$$

$$= R_{sw} (C_{out} + k_n C_{in})$$

the delay of the last stage

$$\tau_{b,n+1} = \frac{R_{sw}}{k_1 k_2 \dots k_n} (k_1 k_2 \dots k_n C_{out} + C_L)$$

The total buffer delay is

$$\tau_{b,total} = \sum_{i=1}^n \tau_{b,i} + \tau_{b,i+1}$$

$$= R_{sw} \left((n+1) C_{out} + (k_1 + \dots + k_n) C_{in} + \frac{C_L}{k_1 k_2 \dots k_n} \right)$$

5.9

for a given product $k_1 k_2 \dots k_n$, the sum $k_1 + k_2 + \dots$

$+ k_n$ is a minimum when $k_1 = k_2 = \dots = k_n = k$.

$$\therefore \tau_{b,total} = R_{sw} \left((n+1) C_{out} + n k C_{in} + \frac{C_L}{k^n} \right)$$

we can find a minimum by differentiating it w.r.t. k

when $k = (C_L/C_{in})^{1/(n+1)}$,

$$\tau_{bmin} = R_{sw} \left((n+1) C_{out} + (n+1) C_{in} \left(\frac{C_L}{C_{in}} \right)^{1/(n+1)} \right)$$

5.10

$k = (C_L/C_{in})^{1/(n+1)}$ then $(n+1) = \ln(C_L/C_{in}) / \ln k$

$$\tau_{bmin} = R_{sw} \cdot \frac{\ln(C_L/C_{in})}{\ln k} (C_{out} + k C_{in})$$

when $\frac{d\tau_{bmin}}{dk} = 0$, τ_{bmin} has a minimum.

$$\therefore k [\ln(k) - 1] = \frac{C_{out}}{C_{in}} \quad \text{--- (1)}$$

n is the closest integer to $n = \frac{\ln(C_L/C_{in})}{\ln k} - 1$

Because $C_{out} + k C_{in} = k \ln(k) C_{in}$ from (1),

$$\tau_{bmin} \approx k R_{sw} C_{in} \ln(C_L/C_{in})$$