Giant Isotope Effect in Hot Electron Degradation of Metal Oxide Silicon Devices

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Abstract— **A giant isotope effect of hot electron degradation was found by annealing and passivating integrated circuits of recent complementary metal oxide silicon (CMOS) technology with deuterium instead of hydrogen. In this paper, we summarize our experience and present new results of secondary ion mass spectroscopy that correlate deuterium accumulation with reduced hot electron degradation. We also present a first account of the physical theory of this effect with a view on engineering application and point toward rules of current and voltage scaling as obtained from this theory.**

Index Terms— **Charge carrier processes, CMOS integrated circuits, deuterium materials/devices, hydrogen materials/devices, MOS devices, semiconductor-insulator interfaces, transistors.**

I. Introduction

A large body of literature exists on hot electron and hydrogen related degradation of MOS devices. Degradation has been identified to be due to trap generation in the oxide [1], [2] as well as at the Si-SiO_2 interface [3] and the interface to polysilicon gates [4]. While numerous experimental facts of the degradation have found a large variety of explanations, the actual mechanism of the damage has only been cursorily addressed. For damage within the oxide, electron hole defect recombination and the corresponding energy release have been identified as the likely cause [1], [2]. At the Si-SiO_2 interface and the interface with polysilicon it is the release of hydrogen [3]–[5] and the creation of dangling bonds that have been identified as culprits by experiments of various levels of sophistication including nuclear magnetic resonance. However, the actual mechanism as to how the energy of electron-hole recombination or the energy of hot electrons (or holes) creates the defects has not been researched to any significant detail. We recently found a new large isotope effect for hot electron degradation by using deuterium instead of hydrogen for interface passivation [6], [7]. This effect has been confirmed [8], shining light on at least one of the actual degradation mechanisms and is the central theme of this paper.

The isotope effect can be used to distinguish hydrogen related hot electron damage from other mechanisms. It was initially discovered during scanning tunneling microscope (STM) experiments dealing with passivation and de-passivation of silicon surfaces in ultrahigh vacuum (UHV) [9]–[13]. These experiments showed that it takes a certain number of electrons (typically of the order of 10^6–10^8) having a certain energy (in the electron volt range) to remove hydrogen from the (100) silicon surface. The same experiments performed with the isotope deuterium instead of hydrogen required roughly a factor of one hundred more electrons to remove deuterium for electron energies above ~4 eV. Recent STM experiments now show that this isotope effect increases dramatically for electron energies below 4 eV [11].

These basic STM experiments led to investigations of hot electron degradation of CMOS devices that were annealed in a deuterium atmosphere [6], [7]. Again a large isotope effect was found with transistor lifetimes being extended by factors of 10–50. Smaller improvements were observed under circumstances of large background hydrogen or reduced deuterium diffusion (e.g., nitride spacers). Various experiments by major chip producers have confirmed our first findings and we have developed a theoretical framework based on electronic desorption theory that explains these effects.

The purpose of this paper is to present an overview of our experimental findings and to outline a first principles theory of hot electron degradation. This work has direct implications for device scaling and the possibility or impossibility to significantly reduce these effects by using lower voltages. The basic desorption mechanism toward which the isotope effect points is the creation (by hot electrons) of vibrational excitations of hydrogen bound to silicon (or polysilicon) at an interface. These vibrations and collisions with electrons having a few electron volts of energy which can then lead to desorption of the hydrogen, creating atomic hydrogen and a dangling bond. The freed atomic hydrogen subsequently can create further damage. The desorption mechanism itself determines critical energies and current densities and is therefore important for understanding and controlling degradation.

We first review the STM experiments, the STM isotope effect, a theory of this effect and implications of these experiments for predicting degradation. The next section reviews degradation mechanisms in CMOS devices and the recent findings of the isotope effect, including measurements of the interface deuterium concentration as found by secondary ion mass spectroscopy (SIMS). The final sections summarize our current theoretical understanding of hydrogen and deuterium desorption as well as possible consequences for device scaling and improving transistor lifetimes by using deuterium during various processing steps.

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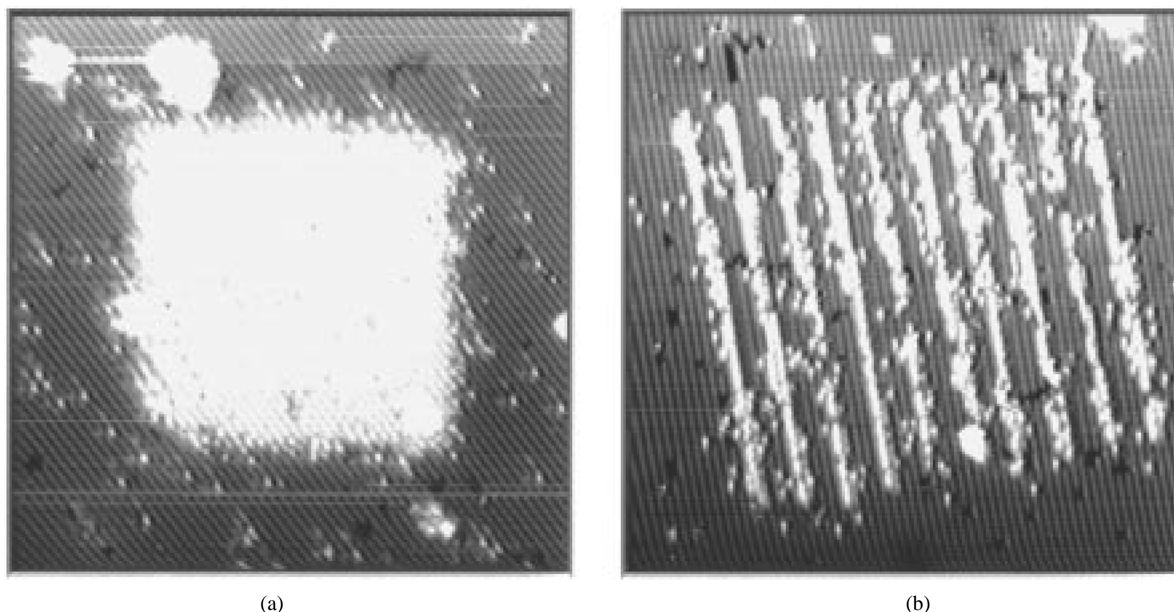


Fig. 1. A demonstration of STM depassivation of hydrogen from Si(100) surfaces. (a) A 500 Å × 500 Å STM image of a H-passivated Si(100) surface where the central 290 Å × 290 Å region has been depassivated by raster scanning with the tip while biasing the sample at 5.5 V and using a current of 1 nA. (b) 1 nm wide lines patterned on a 38 Å pitch using 4.5 V and 2 nA (data from [9]).

II. STM Desorption of Hydrogen and Deuterium: A Giant Isotope Effect

The study of hydrogen and deuterium passivated silicon surfaces by UHV STM has established new connections between basic surface science and the degradation of $Si-SiO_2$ interfaces in MOSFET's. Originally developed as an atom-scale lithography technique [9] (see Fig. 1) for H-passivated Si(100) surfaces, the STM experiments also indicated the existence of two electron energy regimes for hydrogen desorption [10]. For electron energies above ∼6 eV hydrogen desorption is independent of current and voltage with a critical dose of about 400 000 electrons required to desorb each H atom. Below 6 eV the desorption yield falls rapidly and below 4 eV a strong dependence of desorption yield on both current and voltage is observed [10]. Recent low temperature UHV STM experiments show similar behavior as seen in Figs. 2 and 3 [11]. Fig. 2 shows a strong onset for both hydrogen and deuterium desorption at ∼6–7 V (tip negative), corresponding probably to the direct excitation of the Si-H(D) bonding-to-antibonding transition. Above 6 V the desorption is independent of both current and voltage, requiring $\sim 4 \times 10^5$ or 2×10^7 electrons to desorb a hydrogen or deuterium atom respectively. These yields are (according to the theory described below) determined by the average kinetic energy acquired by the H(D) atom while in the antibonding state. At lower voltages (see Fig. 3) the desorption yield exhibits a strong dependence on both voltage and current. This behavior is well explained by the multiple vibrational excitation model advanced by Avouris' group [12]. At lower voltages the STM electrons have sufficient energy to excite the Si-H(D) oscillator [0.25 eV (H), 0.18 eV (D)] leading to a hot ground state. The low hydrogen mass gives this vibrational state a long lifetime (10 ns at 300 K) since its high frequency results in poor coupling to the bulk silicon phonon modes. Consequently, at high STM current densities, multiple excitations of the vibrational mode can exceed the decay rate, leading to desorption from the ground state potential. It is interesting to note that this occurs for STM current densities in the range of $\sim 10^5$ A/cm^2, a value that is comparable to the possible current density at the $Si-SiO_2$ interface in a MOSFET.

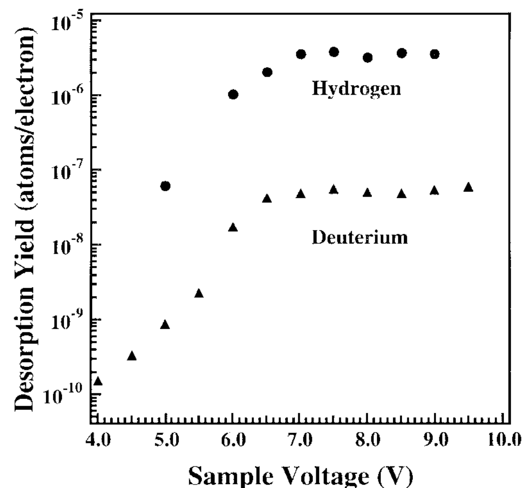


Fig. 2. The hydrogen and deuterium desorption yields in the electronic excitation regime as a function of voltage, determined from low-temperature STM measurements (data from [11]).

As seen in Fig. 2, a dramatic isotope effect is observed in the STM experiments when hydrogen is replaced by deuterium [11], [13]. The desorption efficiency for deuterium from Si(100) is about a factor of 50 lower than hydrogen for energies above ∼5 eV. An isotope effect this large cannot be explained by differences in hydrogen and deuterium zero-point energies or by a host of other effects involving e.g., diffusion. On the other hand, the isotope effect we observe is consistent with an electronic excitation and vibrational heating mechanism.

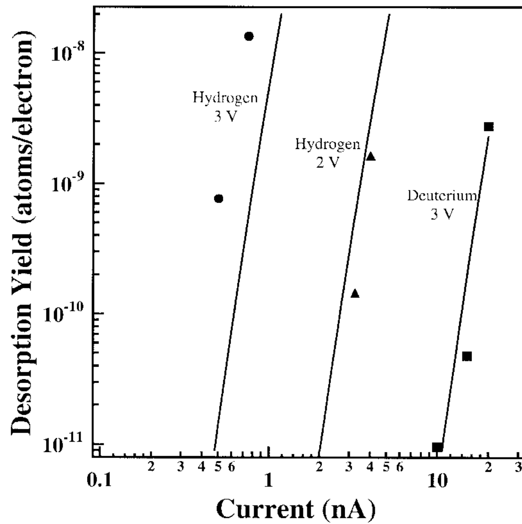


Fig. 3. Current and voltage dependence of the hydrogen and deuterium desorption yields in the low-voltage vibrational heating regime. The solid lines are fits to Avouris' vibrational heating model ([12]) (data from [11]).

In the electronic excitation regime, STM electrons colliding with the Si-H(D) bonding electron can transfer sufficient energy to promote it to the antibonding state. In this state the electron is more probable to be found in such positions so as to exert a repulsive force F_d which accelerates the H away from the Si atom along the excited state potential. Desorption can occur either directly from the excited state or, for shorter excited state lifetimes, by the hydrogen atom overcoming the ground state potential barrier if they previously acquired sufficient kinetic energy while in the excited state. An analysis of the isotope effect expected in this case has been published by Avouris *et al.* [13] and is identical in concept to the theories put forward by Menzel and Gomer [14] and Redhead [15]. Structural calculations based on quantum molecular dynamics methods [16] confirm these results. Basically, the kinetic energy $E_{\rm ta}$ of the hydrogen (keeping the silicon fixed) after an acceleration time t_a is given from Newton's laws as

$$E_{\rm ta} = \frac{F_d^2 t_a^2}{2M_H}. \tag{1}$$

If there is a critical kinetic energy $E_{\rm cr}$ necessary for desorption, then it can be reached after time $t_{\rm cr}$ which can be calculated from (1)

$$t_{\rm cr} = \frac{\sqrt{2M_H E_{\rm cr}}}{F_d}. \tag{2}$$

The probability $P_{\rm ex}$ that the electron stays in the excited antibonding state is typically given by a lifetime

$$P_{\rm ex} = \exp[-(t/t_{lif})]. \tag{3}$$

The probability for desorption P_{ds} is then

$$P_{ds} = \exp[-(\sqrt{2M_H E_{cs}}/F_d t_{lif})]. \tag{4}$$

For the same lifetime of the excited state one obtains from (4) considerable isotope effects depending on the factor that accompanies the mass in the exponent. The slower motion of deuterium also causes additional quenching of the excited state [13].

The data in Fig. 2 show that the large isotope effect persists in the transition region from 4 to 6 eV. The recent low temperature STM desorption experiments indicate that the isotope effect increases dramatically at lower voltages as seen in Fig. 3 [11]. In this regime, as discussed above, multiple excitations of the Si-H(D) vibrational mode result in desorption if the excitation rate, which depends on current density, exceeds the decay rate, which depends on energy transfer to bulk phonon modes. Since the Si-H vibrational energy at $\sim$0.25 eV is higher than its Si-D counterpart, it exhibits significantly weaker coupling to the bulk silicon phonon modes [13]. This accounts, at least in part, for the much longer vibrational lifetime for Si-H (10 ns) than for Si-D (0.25 ns). As pointed out by Van de Walle and Jackson [17], the isotope effect may also be compounded by the coincidence of the Si-D bending mode at 0.0570 eV with the 0.0574 eV TO phonon at the X point for silicon. The Si-H bending mode at 0.081 eV would not couple energy nearly as effectively to this phonon mode.

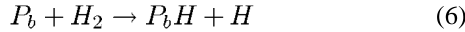
The STM desorption experiments show that both single and multiple excitation events can lead to desorption. At higher electron energies ($> \sim$5 eV) the desorption is dominated by single events and no significant current or voltage dependence is observed for the desorption. Below 5 eV the desorption yield decreases significantly as the vibrational heating regime is entered and multiple excitations begin to dominate the desorption process. The recent low-temperature STM desorption experiments [11] shed interesting light on the underlying desorption mechanisms. In the high-voltage single particle regime the desorption yield shows no temperature dependence between 300 and 11 K. However, in the vibrational heating regime (e.g., at 3 V) there is a very strong temperature dependence with, for example, hydrogen being over two orders of magnitude easier to desorb at 11 K than at 300 K. This may be qualitatively explained by an increase in the vibrational lifetime at low temperatures resulting from a reduced coupling to the bulk phonon modes. In light of the following discussion, this result implies that MOS transistors will degrade more rapidly at lower temperatures. Such behavior has been observed as reported recently by Song and MacWilliams [18].

In the following, we will make a case that hydrogen desorption by hot electrons in MOS transistors follows similar lines to STM desorption. This comparison of the STM study to device engineering also suggests an isotope effect in transistor degradation as long as it involves energetic electrons and hydrogen. Indeed we have shown a large isotope effect in transistor lifetime.

III. Degradation of Transistors and Reliability Involving Hydrogen

Low temperature post-metal anneals (350–450 °C) in hydrogen ambients have been successfully used in MOS fabrication technologies to passivate the silicon dangling bonds and consequently to reduce Si/SiO_2 interface trap charge density [19]–[23]. This treatment is imperative from a fabrication

standpoint since silicon dangling bonds at the Si/SiO_2 interface are electrically active and lead to the reduction of channel conductance and also result in deviations from the ideal capacitance-voltage characteristics. Electron spin resonance (ESR) measurements performed in conjunction with deep level transient spectroscopy (DLTS) and capacitance–voltage (C–V) measurements have elucidated the role of hydrogen in this defect annihilation process. The passivation process is described by the equation



$$P_b + H_2 \rightarrow P_bH + H \quad (6)$$

where P_bH is the passivated dangling bond [24]–[27]. These measurements indicate that for the oxides grown on Si(111), the density of the interface trap states in the middle of the forbidden gap decreases from 10^{11}–10^{12} cm^{-2} eV^{-1} to about 10^{10} cm^{-2} eV^{-1} after the post-metal anneal process step [19]–[26]. The Si(100)/SiO_2 material system, which is technologically more significant, exhibits the same qualitative behavior [28], [29]. The necessity of post-metallization anneal processing for CMOS technologies is demonstrated in Fig. 4(a) and (b) where the measured NMOS threshold voltage (V_{th}) and transconductance (g_m) distributions of a wafer annealed in forming gas (10% H_2) is compared with an untreated wafer. The high mean value and variation of the threshold voltage and reduced channel mobility across the untreated wafer is a clear indication of the unacceptable levels of interface trap density for CMOS circuit operation and stability.

The first observations of hot carrier (holes or electrons with large kinetic energies) related damage of the Si/SiO_2 interface was made in silicon n-p-n bipolar transistors stressed under strong base-emitter reverse bias. The base-emitter junctions of these structures were covered with SiO_2. Collins [30] and McDonald [31] noted that the properties of the Si/SiO_2 interface along the perimeter of a strongly reverse-biased base-emitter junction was electrically altered over time. The change in the electrical properties of the Si/SiO_2 interface was described as an enhancement in the interface (surface) recombination velocity which results in an excess base recombination (nonideality factor $n = 2$) current. The importance of hydrogen in the electrical degradation process for the Si/SiO_2 system was demonstrated by Nicollian *et al.* [32] in a series of experiments performed on MOS capacitors. SiO_2 layers were grown on p-type silicon substrates in a dry ambient and later exposed to tritiated water. Cr–Au dots or Hg probes were used as the metal contact. An avalanche plasma was set up to inject electrons into the SiO_2 layer. The β activity and the C–V characteristics of the samples were monitored. With these experiments, Nicollian *et al.* showed that there was a one-to-one correspondence between the hydrogen lost (i.e., reduced β activity) and negative charge produced in a hydrated SiO_2 layer in the presence of electron currents. Subsequently, other researchers observed threshold voltage instability and channel transconductance degradation in MOS transistors [33]–[35] where hot carriers were generated using the source-drain electric field.

The current industry practice for evaluating the intrinsic reliability of a MOS transistor involves two distinct accelerated

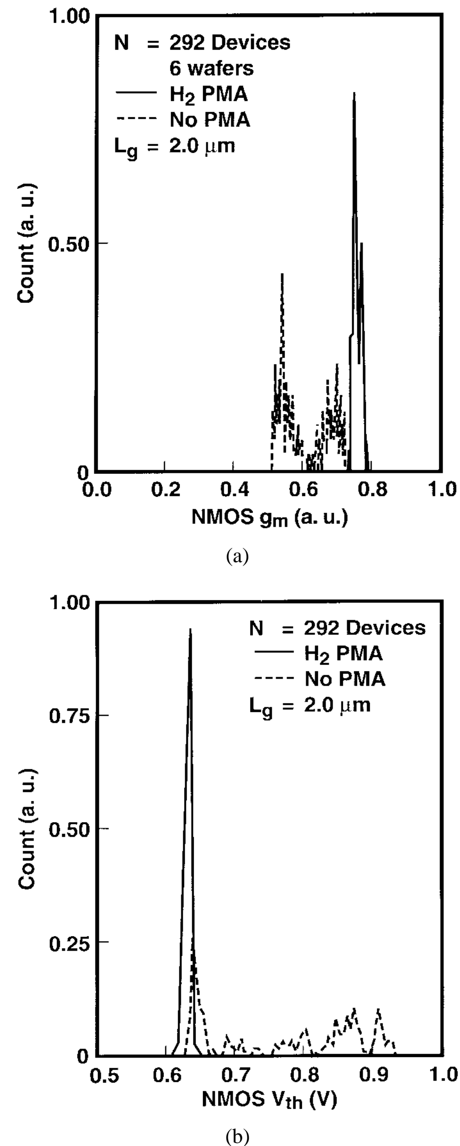


Fig. 4. Histogram demonstrating the effect of forming gas anneals on the NMOS transistor: (a) transconductance and (b) threshold voltage.

electrical stress test methodologies (including certain intermediate methodologies). Although it is unlikely that the physical mechanisms responsible for gate oxide wear-out is identical in each of these cases, hydrogen appears to play some role in both modes of degradation. In the first stress configuration, the Si/SiO_2 system is degraded via large electrical fields across the gate oxide (e.g., $|V_G| \gg V_D$) [36]–[38]. Threshold voltage shifts in MOS capacitor structures are observed. The damage induced in this degradation mode is due to both charge trapping in the oxide and the creation of Si/SiO_2 interface trap states. Our initial studies have not clearly identified an isotope effect for this mode of stress test [39]. Poindexter and Gerardi have used deuterated water and investigated field generated P_b centers, also with negative results [40].

In this paper, we only discuss the second stress configuration, namely the *channel hot carrier aging of NMOS transistors, where we have discovered the large isotope effect.* In the channel hot carrier stress test, the Si/SiO_2 interface is

degraded by hot carriers that are traversing the device from source to drain. The carriers gain kinetic energy from the source-drain electric field and the device is biased under peak substrate current conditions (e.g., $V_D \approx 1/2V_G$). DC, ac, or pulsed dc wave-forms are most commonly used. Channel hot carrier degradation in MOS transistors manifests itself in the form of threshold voltage ($V_{\rm th}$) instability, transconductance ($g_m = dI_{\rm DS}/dV_{\rm GS}$) degradation, and increase in the sub-threshold slope ($S_i = d \ln I_{\rm DS}/dV_{\rm GS}$ at $V_{\rm GS} < V_{\rm th}$) over time. The asymmetry of the C–V characteristics under source-drain reversal indicates that the damaged region is localized near the drain end (pinch-off region) of the transistor. This mode of accelerated stress tests performed on NMOS transistors typically results in localized oxide damage, which has been correlated to Si/SiO_2 interface trap states [41]–[45]. Moreover, it has been suggested that the generation of the interface trap states is due to hot carrier stimulated hydrogen desorption and de-passivation of the silicon dangling bonds [3], [4].

Various technological advances have been made to address the problem of MOS transistor degradation due to channel hot carriers. The most significant and lasting progress in fabrication technology to alleviate the channel hot carrier problem has been the development of lightly-doped source-drain (LDD) and gate side-wall spacer processes [46]–[48]. The LDD region is used to reduce the strength of the electric field in the channel direction. These advances have been integrated in all submicron CMOS technologies at the cost of added process complexity and intricate device design [49]. However, processing requirements for good short channel behavior and high performance, namely, shallow source-drain junctions, reduced overlap capacitance, and low source-access resistance, are all at odds with hot carrier immune device design which makes alternate methods to improve hot electron degradation desirable.

A plausible argument and hope for future improvements has been that the hot carrier degradation effect can be scaled away by reducing the supply voltage (constant field scaling). However, this argument does not appear to be valid since device feature size scaling accompanies supply voltage scaling in ULSI CMOS technologies to achieve improved performance and increased packing density. Gate oxide thickness is also reduced to maintain the device current density at low supply voltage operation. Takeda et al have observed device degradation in a no-LDD NMOS transistor structure with gate lengths of 0.3 μm at 2.5 V [50]. Chung *et al.* observed hot carrier degradation for a 0.15-μm gate length transistor (with no LDD regions) at 1.8 V [51]. A current state-of-the-art high-performance 1.8 V–0.18 μm CMOS technology with good quality gate oxide exhibits hot carrier degradation effects and requires precise lightly-doped drain engineering [52]. The existence of degradation at low voltages points to the multiple vibrational excitation mechanism of H desorption at the Si/SiO_2 interface and hints to a dependence of the desorption mechanism on both voltage (electric field) and current density as described below.

Circuit solutions to eliminate hot carrier degradation effects in transistors, although proposed, involve further circuit design

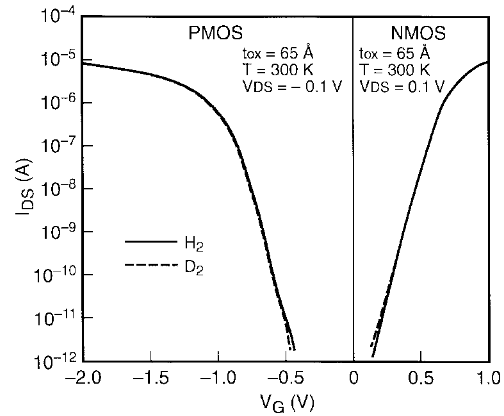


Fig. 5. Drain current versus gate voltage for NMOS and PMOS transistors annealed in forming gas with deuterium and hydrogen ambients. The anneal time is 1 h and performed at 400 °C.

and layout complications [53], [54] and ever present circuit related voltage overshoots actually increase degradation. Obviously, hot carrier induced transistor degradation will continue to be a major constraint for the design of high performance sub-0.25-μm CMOS technologies.

IV. The Isotope Effect in NMOS Transistor Degradation

NMOS transistors fabricated with Lucent Technologies 0.35- and 0.5-μm CMOS technology [55], [56] were used in the accelerated hot carrier dc stress experiments. After the first level of metal processing, uncapped wafers as well as wafers capped with Si_xN_y were subjected to a hydrogen or deuterium anneal process. The anneal process was done at 400–450 °C for 0.5 to 2 h. The percentage of molecular deuterium (hydrogen) in the forming gas was set at 10%.

Fig. 5 shows the transfer characteristics of uncapped NMOS and PMOS transistors annealed in deuterium and hydrogen ambients at 400 °C and 1 h. Prior to hot electron stress, transistors annealed in either ambient are electrically indistinguishable. This proves that deuterium and hydrogen are equally effective in reducing the interface trap charge density, resulting in equivalent device function. Hence, deuterium can be substituted for hydrogen post-metal anneal processes in semiconductor manufacturing.

We now show that these devices annealed either in deuterium or hydrogen, although appearing identical in pre-stress electrical tests, will exhibit markedly different degradation dynamics.

Accelerated hot carrier stress experiments were performed on NMOS transistors at peak substrate current conditions ($V_G \approx 0.4\ V_{\rm DS}$). Two independent experimental set ups each consisting of a probe station, a computer, and a HP4145 network analyzer were used to collect the data. The degradation of the transistors were monitored periodically during electrical stress by recording the linear transconductance, threshold-voltage, subthreshold slope, and drain current (in saturation and linear regime). We point out that no improvement in NMOS transistor hot electron lifetimes was observed in wafers which were annealed in deuterium after the wafers had been

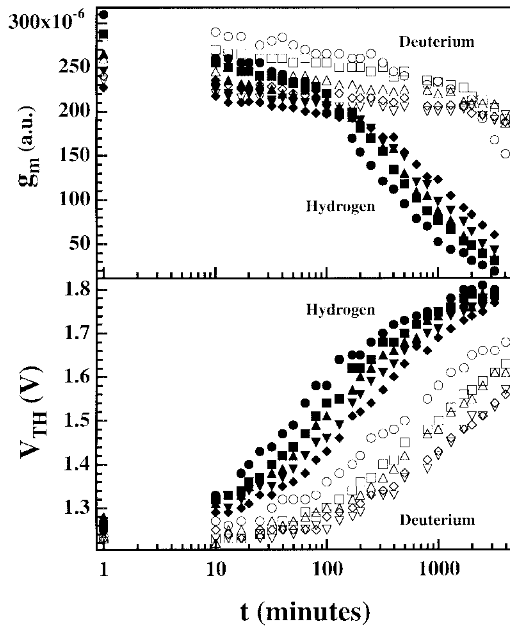


Fig. 6. Comparative time-dependent degradation of the transconductance g_m (top graph) and threshold voltage $V_{\rm th}$ (bottom graph) for five NMOS transistors annealed in hydrogen (solid symbols) and deuterium (empty symbols). The annealing process was performed in a 90% N_2 : 10% $H_2(D_2)$ ambient at 400 °C for 1 h.

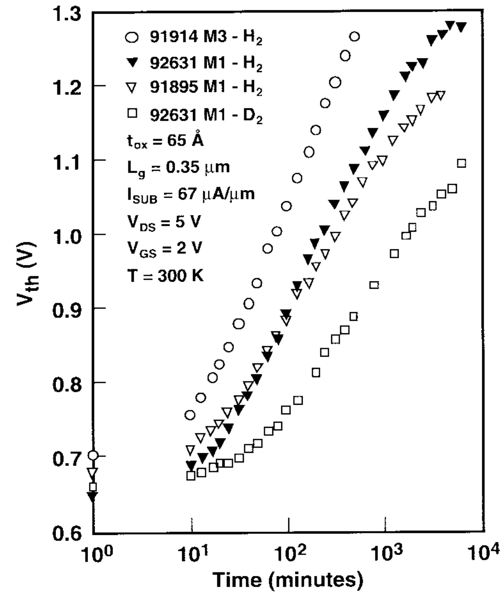


Fig. 7. Degradation of $V_{\rm th}$ versus time. The transistors were fabricated using a development version of Lucent's 0.35-μm CMOS technology where $L_G = 0.35\ \mu$m, $I_{\rm ON} = 600\ \mu$A/μm, $V_{\rm th} \sim 0.65$ V. LDD regions are implanted with arsenic.

capped with Si_xN_y. As we will discuss below this is an expected result since Si_xN_y provides a barrier for the diffusion of hydrogen as well as deuterium.

Fig. 6 shows results from our original experiment [6]. The transconductance and threshold voltage degradation is given as a function of time for NMOS transistors with gate lengths ranging from 0.5 to 0.7 μm. The stress condition is $V_{\rm DS} = 5$ V and $V_{\rm GS} = 2$ V. All of these transistors are from the same wafer and processed identically (up to first level of metal) except for the ambient they were annealed in, i.e., deuterium versus hydrogen forming gas (10%–90% N_2) at 400 °C. To enhance the hot carrier effects, Lucent's 0.5-μm CMOS technology [56] was modified by 1) reducing the gate oxide to 55 Å, 2) increasing the doping in the p-well (note the high initial threshold voltage), and 3) replacing the lightly doped regions with a heavily doped (arsenic) source-drain extension region. Wafers annealed in deuterium show much more resilience to channel hot carrier stress. If we use 20% g_m degradation as a lifetime criterion, transistors annealed in deuterium have lifetimes 10–50 times longer than those annealed in hydrogen. Likewise, a factor of 10 improvement in lifetime is extracted for a degradation criterion of 200 mV in $V_{\rm th}$. This was confirmed for more than 80 other transistors fabricated on this wafer.

To further confirm these pronounced effects, a second lot using an experimental version of Lucent's 0.35-μm 3.3 V CMOS technology [55] was processed up to first level of metal $(M1)$. Fig. 7 shows the $V_{\rm th}$ degradation as a function of stress time. A hydrogen annealed device from another lot was also aged. As a further consistency check, data for a hydrogen annealed device but processed up to third level of metal $(M3)$ is shown. It is known that a device processed through many levels of interlevel dielectric and metal layers will have the worst aging characteristics (as verified here). The comparison of time dependent g_m degradation is demonstrated in Fig. 8 for devices with effective gate lengths of 0.37 and 0.48 μm. Fig. 9 shows the traditional lifetime versus substrate current for 10 and 20% g_m degradation criteria. Data was collected at stress voltages of $V_{\rm DS} \approx 4.2$–4.6 V. A peak substrate current specification of $I_{\rm SUB} = 2000$ nA/μm at $V_{\rm DS} = 3.3$ V is used to estimate the lifetime of the NMOS transistor at worst-case dc (peak substrate current) operating conditions. It is noted that the substrate current specification for this technology can be increased by a factor of 2 while achieving equivalent hot carrier lifetime when deuterium is substituted for hydrogen in the post-metal anneal process. In all of the cases discussed above, the deuterium annealed transistors are much more robust under channel hot electron stress.

A third batch of anneal-stress experiments were performed for final verification. Results are summarized in Fig. 10 for NMOS transistor lifetime. The criterion for lifetime in this figure is taken as the dc stress time required to induce a 50 mV $V_{\rm th}$ shift. Once again deuterium annealed transistors were more resilient under hot electron duress.

It is important to correlate the observed improved hot carrier reliability to the location and quantity of deuterium in the wafer. SIMS analysis through the first interlevel oxide and silicon was performed on two uncapped samples as shown in Fig. 11. One wafer was annealed in forming gas (10% molecular hydrogen), while the other sample was annealed in forming gas comprising 10% molecular deuterium. A Cameca IMS-3f system with oxygen primary beam 60 μm^2 was used for analysis. $^{18}O^+$ is monitored to locate the SiO_2/Si interface. The D^+ concentration is inferred from the difference between the $2H^+$ (2H denotes the SIMS signal at a mass-to-charge ratio of 2) profiles for wafers annealed in deuterium and

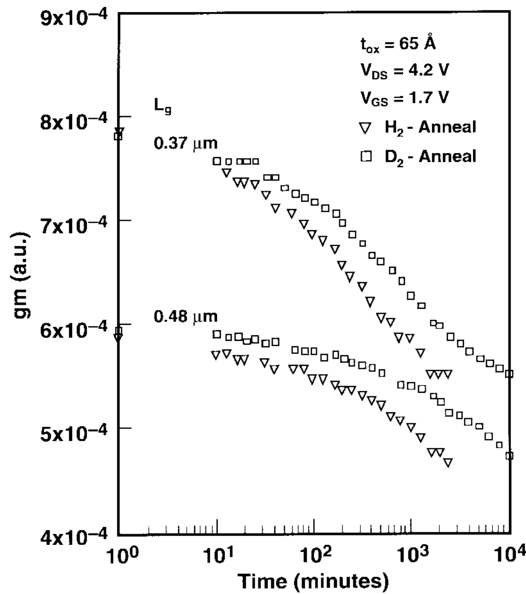


Fig. 8. Comparison of time dependent transconductance degradation of NMOS transistors that are annealed in a hydrogen versus deuterium ambient.

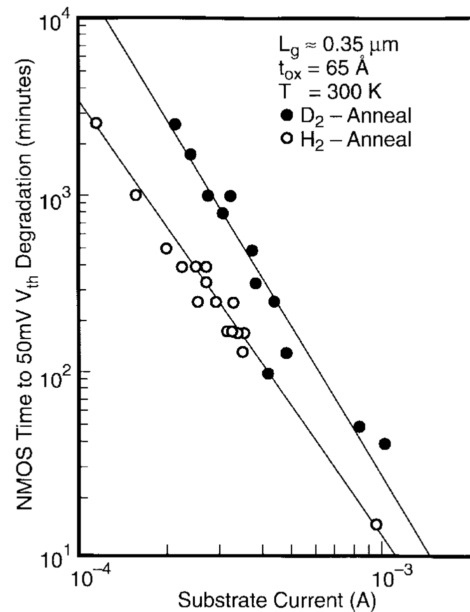


Fig. 10. Hot electron degradation lifetime versus substrate current.

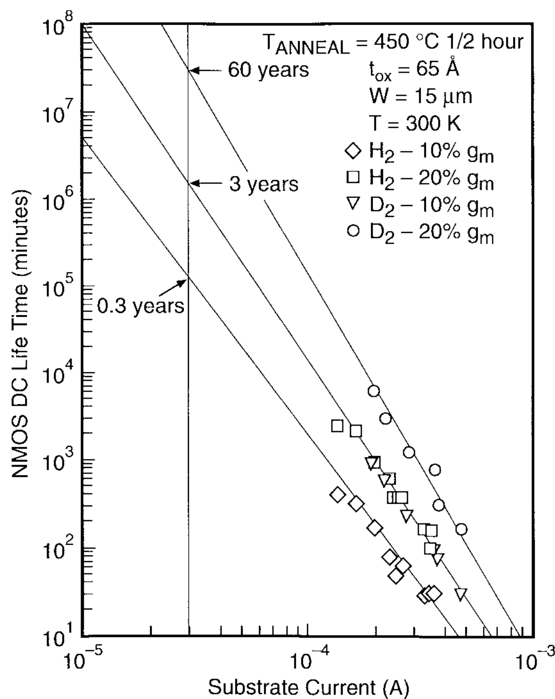


Fig. 9. Hot electron degradation lifetime versus substrate current. Stress voltages of $V_{\mathrm{DS}} \sim 4.2$–4.6 V. A substrate current specification of $I_{\mathrm{SUB}} = 2000$ nA/μm at $V_{\mathrm{DS}} = 3.3$ V is assumed.

hydrogen. First, no deuterium was detected in samples if the sinter process step was performed on wafers that were capped with $\mathrm{Si}_x\mathrm{N}_y$. As discussed above, these devices showed no improvement in their resilience against channel hot carrier damage. It is well known that $\mathrm{Si}_x\mathrm{N}_y$ forms a barrier (although penetrable) for deuterium. This has practical implications for technologies that use sidewall spacers composed of silicon nitrides. Second, deuterium was not detected under large areas $(200 \times 200\ \mu\mathrm{m}^2)$ of polysilicon in wafers which were annealed in deuterium and were not capped with $\mathrm{Si}_x\mathrm{N}_y$. These areas are much larger than the $0.5\ \mu\mathrm{m} \times 15\ \mu\mathrm{m}$ feature sizes studied by SIMS analysis as shown in Fig. 11. This indicates the finite lateral diffusion length of deuterium in the transistor gate oxide and channel region. However, deuterium is detected in the interlevel oxide at concentrations of 10^{19} cm^{-3} and was found to accumulate at Si/SiO_2 interfaces with a surface concentration of 10^{14} cm^{-2}. This SIMS study suggests that deuterium diffuses rapidly through the interlevel oxides and the gate sidewall spacers to passivate the interface states in the transistor channel region. However, the exact lateral spread (reach) of diffused deuterium in the transistor-channel and gate-oxide region is not certain.

In summary, a clear isotope effect appears in transistor lifetimes during accelerated stress tests. The degradation times are typically delayed by a factor of 10 for deuterium as compared to hydrogen anneals. We have found single devices that showed even better lifetime improvements up to factors of 50 and more. Our continued work has shown that whenever a large deuterium content (approaching or exceeding the hydrogen densities) at the interface can be detected, large corresponding improvements in transistor lifetimes are measured [57]. There are several possibilities that prevent a large deuterium accumulation at the interface compared to hydrogen. The presence of silicon nitrides in the form of caps or side-wall spacers at the gate electrode almost always diminishes the isotope effect. We believe that this is due to large hydrogen content of nitrides that may influence the hydrogen concentration at the interface (particularly close to the source-drain edges). Furthermore, nitrides represent a diffusion barrier for deuterium. Accurate assessment of these effects can only be made by partially or totally substituting deuterium for hydrogen in device fabrication processing steps.

Many researchers have related to us experiences that some improvements in hot carrier degradation depend sensitively on oxide chemistry and may be found for one type of oxide and

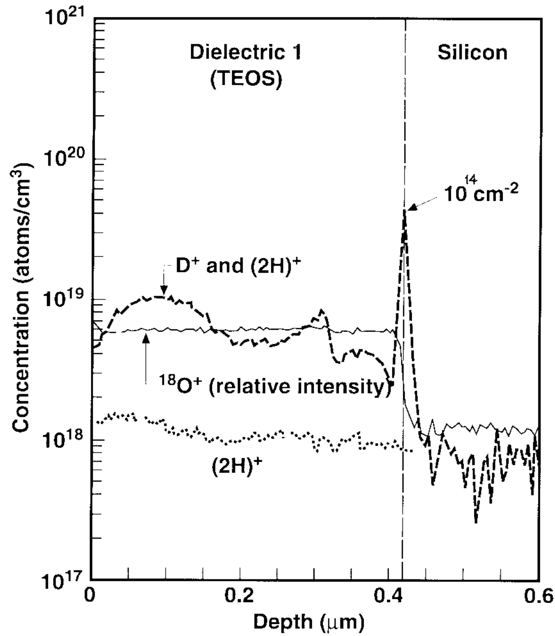


Fig. 11. SIMS profiles for deuterium, hydrogen, and oxygen. $^{18}O^+$ is monitored to locate the SiO_2/Si interface. The D^+ concentration can be inferred from the difference between the $2H^+$ profiles for wafers annealed in deuterium and hydrogen. 2H denotes the SIMS signal at a mass-to-charge ratio of 2 (SIMS data from F. Stevie).

not for others or even in one transistor but not in others. In this context we would like to point out that in our experiments the oxide chemistry has not been changed. The chemistry of deuterium and hydrogen is basically the same, including the diffusion constant in SiO_2, which is virtually identical for H_2 and D_2 [58]. The only difference is in the desorption, i.e., in a type of chemical "reaction velocity." It is probably for this reason that the isotope effect was easily observed by several chip fabrication laboratories. In our opinion, it will work for any oxide and device in which the passivation and de-passivation of dangling bonds by hydrogen play a role since this situation is analogous to the STM experiments for Si surfaces in UHV. It may also play a role in other situations involving more complex hydrogen compounds. The effect of changed "reaction velocities" for hydrogen and deuterium, with the rest of the chemistry unchanged, is very well established and even enters the chemistry of deuterium production from lake-water. We expect the isotope effect, therefore, to be a general property of the transistor degradation that involves hydrogen.

V. Theory of Hot Electron Transistor Degradation Involving Hydrogen and Deuterium

We propose a theory of hydrogen related hot electron degradation in transistors similar to the STM desorption theory of Section II. Naturally, the parameters of the theory for the free silicon surface will differ from those of the Si/SiO_2 interface. For example, the critical kinetic energy $E_{\rm cr}$ for desorption is estimated from density functional theory [16] to be around to 3.8 eV. The presence of the oxide may change this number. A lowering can be suggested from the proximity of oxygen and the possibility of forming an O-H bond. This bonding energy would have to be deducted from the $E_{\rm cr}$ of the free surface. Of course such a bond may involve more complex chemistry. From these possibilities we can only guess that the presence of SiO_2 on top of silicon may facilitate the desorption process. Similarly, the force F_d that is typically exerted [16] at the free silicon surface may be changed by the chemical environment of the interface and even the energy of the excited state, estimated for the free surface Si-H bond to be around 6 eV, may be significantly changed, lowered or increased by the chemical environment. As a zero order approach we may assume that the parameters are close to those of the free surface but distributed around them because of the presence of the surrounding chemical environment.

From these simple considerations we expect degradation to depend sensitively on the energy of the hot electrons (voltage, electric field in the channel and oxide) for single electron desorption events with two thresholds, one soft around 6.0 eV for the excited states (soft because of the uncertainty principle and the fact that there are many excited states within a few eV even for the free surface) and one threshold around the desorption energy of 3.8 eV but still fluctuating because of interface chemistry [16]. If multiple electron desorption becomes possible, the thresholds will soften further and may vanish entirely at extremely high current densities since vibrational excitation does not call for any strict threshold except the characteristic energy of vibration which is 0.25 eV for Si–H.

The two desorption theories, that can explain the large isotope effect in both STM desorption and transistor degradation, do not hint toward a hard threshold for the process to occur if the degradation is indeed happening due to channel electrons at the Si/SiO_2 interface. We are, of course, aware that there are proven degradation mechanisms that involve hot electrons in the oxide and desorption of hydrogen close to the gate electrode (polysilicon or metal) or within the SiO_2 [3]. We also know that the strength of the isotope effect can change considerably with the value of the parameters that enter (4) (e.g., $t_{lif} \rightarrow \infty$ gives always desorption and negligible isotope effect). The particular bias conditions in our transistor experiments, however, do not permit much heating of the electrons in the oxide and a model that invokes the hot channel electrons to create the damage directly at the interface appears to be likely. Clear proof of such assumptions is difficult to achieve since electrons of very high energy can always be present due to electron-electron interaction or ionization feedback [59] and therefore hot electron damage in the oxide cannot be ruled out. Also, even if the hydrogen is released only at the Si/SiO_2 interface it will diffuse at the interface and into the oxide and create further degradation in form of dangling bonds (H_2 creation).

With all these cautions, we believe that at least a significant portion of the degradation is caused by hot source-drain channel electrons via the mechanism of electronic desorption of hydrogen (deuterium) from the interface. For high current densities, multiple vibrational excitations are possible which give rise to reduced thresholds for the desorption process. Currently, STM measurements have been performed down to 2 eV and still show desorption. It is important to realize that

existing methods of predicting hot electron reliability are based on comparing degradation with other processes that happen at elevated electron energy, including impact ionization and the emission of hot electrons into SiO_2. The hot electron degradation is usually measured in "accelerated stress tests" at higher voltages, current densities, etc. and then extrapolated to the actual operating conditions. At the lower voltages, impact ionization and substrate current decay significantly and so does then the extrapolated degradation. However, if at voltages below 3 V the degradation mechanism, that may have a threshold below 3 eV, is compared to processes that have a 3 eV threshold (or higher), then the lifetimes at the true operating conditions may be considerably overestimated.

An intriguing new direction appears to be the use of the STM desorption measurements and the isotope effect to predict transistor lifetimes from accelerated stress tests. The STM experiments provide the number of electrons of a given energy and current density required to desorb hydrogen or deuterium (see Figs. 2 and 3). One therefore can think of interpolation schemes in which tables of STM desorption data are used to accurately map transistor lifetimes measured during stress tests to those which will be exhibited under normal operating conditions. Furthermore, we envision the use of this method to predict the lifetimes of new devices that result from continued scaling to lower voltages and higher channel current densities. To accurately apply this method, Monte Carlo simulations of electron energies in MOSFET's can be performed to extract the numbers of high energy electrons in the channel current distribution. Such a process is by no means entirely trivial because of various problems, such as accurately determining the STM current densities. However, this approach appears to be more promising than the comparison of degradation to other physical mechanisms (such as impact ionization) whose character (threshold) may be different. We believe that such considerations will be of particular importance for low voltage operation.

VI. Summary and Conclusions

Channel hot carrier degradation in NMOS transistors is a major intrinsic reliability constraint for achieving high performance. In Fig. 12, NMOS transistor performance and the allowable minimum channel length for commercially available CMOS technologies for ASIC applications (separately optimized for 3.3 or 5 V operation) are shown [60]. Two features stand out. First, there are no 5 V CMOS technologies with minimum gate lengths below 0.40 μm. For the 3.3 V CMOS technologies, this limit is 0.25 μm. Note that the nominal (target) transistor gate lengths will be typically 0.06 μm to 0.1 μm larger than these values and are determined by process margins in gate length control. Since constraints imposed by short channel effects (subthreshold leakage and threshold voltage roll-off) can be circumvented by drain engineering, the most significant barrier for gate length scaling is the limitation imposed by hot carrier effects (that is the peak substrate current specification).

Second, transistor drive currents are maintained at about 450–600 μA/μm although the operating voltage is reduced

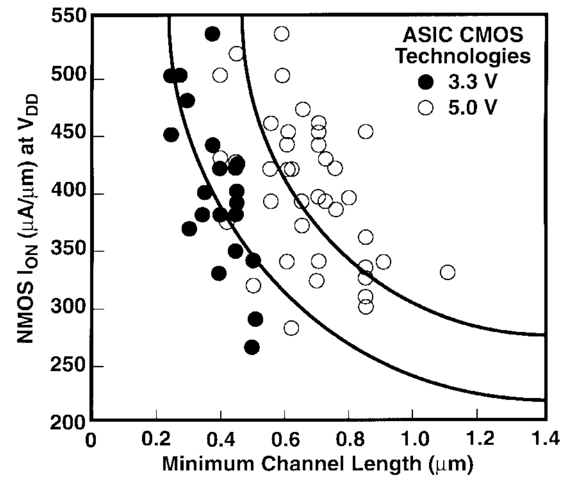


Fig. 12. NMOS transistor saturation (drive) current of ASIC technologies as compiled and published by Brassington [60].

from 5 V to 3.3 V. The reason for this is that device gate length and oxides are being scaled aggressively in constant field scaling. This upward trend of transistor drive currents will continue into the future. (For example, the drive current of the NMOS transistor in Lucent's 0.25-μm 2.5 V CMOS technology is 660 μA/μm [61], 60 μA/μm larger than the 0.35-μm 3.3 V CMOS technology [55].) In this context, we find it particularly significant that the theory of hot electron damage based on vibrational excitations or a mixture of vibrational excitation and single hit desorption theory predicts both a dependence on voltage and current density. Clearly, at high current densities multiple excitations and scatterings are possible before the vibrating Si-H(D) bond returns to equilibrium. As we see from ongoing STM experiments and from the results described above, the dependence of desorption on current density is quite pronounced for very high current densities as they may be realized for 0.1-μm (or below) designs. The scaling of the voltage is then probably insufficient to reduce hot carrier degradation significantly, particularly not for aggressive designs. The isotope effect and its consistent application to theory and experiment thus promises a detailed understanding of the degradation physics from atomic processes to scaling rules.

The impact of this study on existing sub-0.5-μm CMOS technologies is obvious, especially for those technologies where acceptable degradation criteria are barely met. The potential benefits of our discovery for competitive device design can be summarized as follows. In these estimations we target an equivalent channel hot carrier degradation criterion such as 10% g_m degradation in one year. 1) Transistor gate length can be scaled by about 0.1 μm as evident from Fig. 8, 2) the margin for operating voltage can be increased by 0.5 V, at least under accelerated stress conditions, as shown in Fig. 13, and 3) the peak substrate current specification can be increased by about a factor of 2 (see Figs. 9 or 13).

Other benefits include fabrication process simplifications, reduced device optimization-design cycle time, and diminished costs of device development and fabrication. We anticipate that these benefits will increase as devices are scaled to even

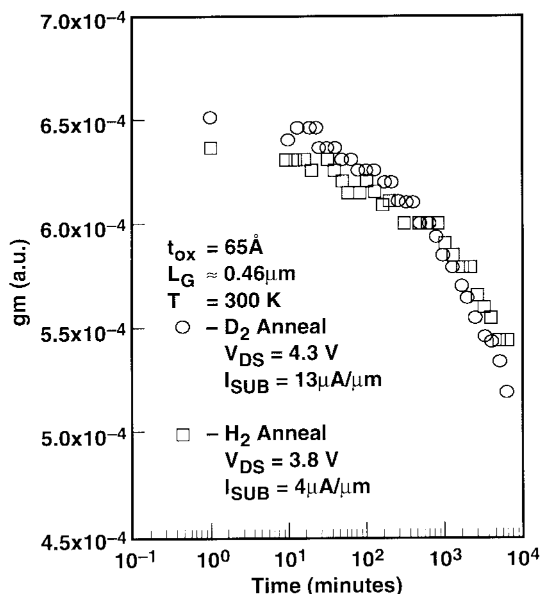


Fig. 13. Comparison of time dependent transconductance degradation of NMOS transistors. Equivalent degradation characteristics is obtained for the transistor annealed in a deuterium ambient and stressed at a much higher drain bias.

smaller feature sizes.

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