

Swaroop Ghosh

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EDUCATION

- **PhD [2004-present]: School of ECE, Purdue University, IN, USA**

Expected Graduation: May 15, 2008
Primary Research Area: VLSI Circuit and Micro-architecture
Secondary Research Area: Microelectronics and Nanotechnology
Research Advisor: Prof. Kaushik Roy

Thesis: Integrated Fault-aware Adaptive Design and Self-Calibration Methodology for Low-Power and Fault-Tolerant Nano-scale Systems

Graduate Courses: Solid State Devices, Computational Models and Methods, Advanced VLSI Design, Advanced VLSI Devices, Digital Signal Processing, Introduction to complex analysis, Advanced linear algebra

- **Master of Science [2002-2004]: ECECS Department, University of Cincinnati, OH, USA**

Primary Research Area: VLSI Design and Testing
Secondary Research Area: Low Power Design
Research Advisor: Prof. Wen-Ben Jone

Thesis: Scan Chain Fault Identification using Weight-based m-out-of-n Codes

Graduate Courses: Design and analysis of algorithms, Introduction to Operating System, Physical VLSI design, VLSI system design, Automata and formal languages, VLSI design and automation, Low Power VLSI design, Topics in VLSI design, VLSI testing and validation, Intro to Computer Architecture

- **Bachelor of Technology [May 2000]: Indian Institute of Technology, Roorkee, India**

Major: Electrical Engineering
Thesis Advisor: Prof. H. K. Verma and Prof. Vinod Kumar

Thesis: Design and Development of Remote Data Acquisition Module

RESEARCH INTERESTS

- **Low-power, fault tolerant and adaptive system design for nanoscale technologies.**
 1. Modeling of failures at system level and providing fault tolerant, adaptive solutions to avoid the failures or compute in presence of defects.
 2. Design methodologies to address power and process variation tolerance in logic circuits and embedded memories.
- **On-chip calibration, diagnosis and self-repair for improving reliability and yield**
 1. Developing process sensors to detect/localize failures and apply on-chip corrective steps (adaptive clocking/source biasing/adaptive voltage scheduling) to avoid the failures.
 2. Design-for-test methodologies to reduce test cost and improve yield.
- **Hybrid systems using emerging low-cost, low-power nano-electronic devices**
 1. Optimization of nano-devices and developing compact models for circuit simulation.
 2. Application of the optimized devices to create hybrid and reconfigurable system for low power, fault tolerance, and on-line test/verification.
- **Non-silicon nano-electronics and application to bio-implantable devices**
 1. Novel biologically-inspired computing platforms for robust and low-power system design.
 2. Bio-implantable, miniature, ultra low-power devices for medical applications.

WORK EXPERIENCE

- **June-August 2007: Co-op engineer at Advanced Micro Devices (AMD) Inc, Sunnyvale, CA**
 1. Memory testing at the RTL level for AMD's upcoming flagship processor.
 2. Scan partitioning to reduce scan power and supply voltage droop
- **May-August 2007: Summer intern at Intel Corporation, Portland, OR**
 1. Sleep transistor variability analysis in L2-cache in 65nm process and its test implications.
- **August 2000-July 2002: VLSI design Engineer at Mindtree Technologies, Bangalore, India**
 1. Design and test of Bluetooth Baseband Controller

2. Distance measurement mode implementation in Baseband Controller
3. Design and test of AHBC (Advance High Performance Bus Controller) Arbiter

TEACHING EXPERIENCE

- **Fall 2004-Spring 2005: Teaching Assistant for the undergraduate (senior year) course “Introduction to electronic design and analysis.”**

Course Content: basic electrical characteristics of common semiconductor devices (pn-junctions, MOSFET's, and BJT's), analyze/design of D.C. bias circuits, utilizing D.C. and A.C. models of semiconductor devices in both analysis and design, single and multistage amplifiers at low, mid and high frequencies, CAD tool (e.g., SPICE) for circuit analysis and design

Responsibilities: helping/teaching students, recitations once a week, prepare exams, quizzes, homeworks/solutions.

RESEARCH EXPERIENCE

Ph.D. Dissertation

Goal: Low-power and fault-tolerant nano-scale systems in presence of process variation and high defect densities.

Solution Strategy: Integrated fault-aware adaptive design and self-calibration methodology. The pre-Silicon fault-aware design ensures low power operation under process variation. Furthermore, the design also keeps options of post-Silicon tuning of certain parameters for adapting the failures if manufacturing defects are being detected in manufacturing test. In contrast to conventional low power fault tolerant techniques, our design philosophy achieves highly reliable nano-scaled systems while staying under the power/performance envelope. To further improve the reliability of the system, we use 3D hybrid technology with “integrated low cost reconfigurable test circuits designed using TFT”. The TFT test circuits reduce the test overhead from Silicon die and monitor the critical sections of system for online test and verification. This approach is elucidated as follows:

- **Fault-Aware Low-Power Adaptive Design Using Critical Path Isolation for Timing Adaptiveness (CRISTA)**
 1. CRISTA methodology to isolate critical paths, make them predictable and avoid the possible errors by adaptive clock stretching. CRISTA is used for correct computation under aggressive supply scaling in order to achieve low power operation. The CRISTA design also enables post-Silicon self-correction.
 2. Employed CRISTA at the micro-architectural level (both *In-Order* and *Out-Of-Order* processor) to obtain low power and robust pipeline designs.
 3. Designed hybrid adders and multipliers that further leverage CRISTA for low power dissipation under aggressive voltage scaling at rated frequency. These hybrid units can be a part of execution units of high speed, low power, and variation-tolerant processors.
 4. Designed a **test chip in IBM 130nm technology** to implement a two-stage low voltage pipeline in order to demonstrate the feasibility of CRISTA under process variation.
- **Self-Calibrating Systems for Fault Tolerance**
 1. Pre-Silicon design using CRISTA with isolated critical paths. If manufacturing test or on-chip speed binning suggest failure of critical paths due to bridging defects then adaptive clock stretching is enabled to avoid delay failures. Designed a **test chip (IBM 130nm technology)** of built-in delay sensor for efficient speed binning.
 2. Developed a fault tolerant scheme that can leverage the inherent redundancy present in high speed arithmetic units in time efficient manner to compute in presence of faults. The proposed methodology can be used to design fault tolerant pipelines in high performance systems.
 3. Employed CRISTA to design low-overhead temperature-adaptive systems. The supply voltage is dynamically scaled during die-overheating while maintaining the rated clock frequency. The delay failures at scaled supply are adaptively tolerated by adaptive clock stretching
 4. Exploiting the above methodology for successful prevention of die-overheating while maintaining rated frequency and tolerance to delay failures at micro-architectural level (*In-order* processors). A prototype of high speed temperature tolerant pipeline with temperature sensor for adaptive supply scaling is in progress.
 5. Developed an adaptive source biasing system and auto-repair scheme for low power and fault tolerant cache. Performed sleep transistor variability analysis in L2 cache of Intel's 65nm processor and explored its test implications. The optimal choice of adaptive source biasing and body biasing to reduce power with robustness to failures is in progress.
- **Low Cost, Reconfigurable and Hybrid Electronic System Using Poly-Si Thin-Film Transistors**
 1. Developed optimized TFT devices and SPICE compatible models for low-cost and ultra low-power digital operation. Using this setup we simulated basic logic building block for power/performance estimation.
 2. Developed a low cost, generic and fully reconfigurable hybrid 3-D integrated system using Thin-Film-Transistors for test cost reduction, improved controllability/observability, online test and verification. The test architecture can be configured as any DFT/BIST or sensors and integrated with bulk-Si to create a hybrid system for improving the reliability of the underlying Silicon die.
- **Other Projects**
 1. Developed an integrated tester-on-chip consisting of low overhead delay sensors to improve the test coverage, test time and delay fault diagnosis. The delay sensors are also used for fast speed binning of high performance dies.
 2. A novel CAD framework using Shannon expansion and dynamic supply gating to improve test power, IDDQ testability, test cost and parametric yield.

M.S. Dissertation

Goal: Scan Chain Fault Identification in the Presence of Signal Integrity Issues.

Solution Strategy: Implementation of Weight-based m-out-of-n Codes

1. Developed scan chain fault identification scheme using weight-based m-out-of-n codes.
2. Developed a serial interfacing technique for testing embedded multi-port memory arrays.
3. Developed an embedded core test generation methodology using broadcast test architecture and netlist scrambling.
4. Worked on psuedo-exhaustive testing of interconnect noises of high speed deep submicron VLSI circuits.

MAJOR ACHIEVEMENTS

- Summer Research Fellowship granted by University of Cincinnati for summer quarter (July - August 2003).
- Recipient of University Graduate Scholarship and Research Assistantship at University of Cincinnati, Ohio.
- Recipient of University Merit Scholarship, IIT Roorkee, India (1996-2000).
- R.D. Verma Merit Scholarship awarded in sophomore year of undergraduate study at IIT Roorkee, India.
- Shamji Memorial Trust Merit Scholarship awarded in senior and junior year of undergraduate study at IIT Roorkee, India.
- Second Prize in annual exhibition of Hobbies club for electronic project at IIT Roorkee.

PUBLICATIONS

Journal papers (published/accepted)

1. **Swaroop Ghosh**, Swarup Bhunia and Kaushik Roy, "CRISTA: A new paradigm for low-power and robust circuit synthesis under parameter variations using critical path isolation", *Trans. Comput. Aided Design and Systems (TCAD)*, Nov 2007.
2. **Swaroop Ghosh**, Swarup Bhunia and Kaushik Roy, "Low-power and testable circuit synthesis using Shannon decomposition based structural transformation", *ACM Trans. on Design Automation Electronic Systems (TODAES)*, Sept 2007
3. **Swaroop Ghosh**, Swarup Bhunia, Arijit Raychowdhury, and Kaushik Roy, "A novel delay fault testing methodology using low-overhead built-in delay sensor", *Trans. Computer Aided Design and Systems (TCAD)*, Dec 2006.
4. Vinod Narayanan, **Swaroop Ghosh**, W. B. Jone and S. R. Das, "A built-in self-testing method for embedded multi-port memory arrays", *IEEE Trans on Instrumentation and Measurement (TIM)*, Oct 2005, v54, pp. 1721-1738.
5. Jia-Hui Jiang, Wen-Ben Jone, Shih-Chieh. Chang and **Swaroop Ghosh**, "Embedded core test generation using broadcast test architecture and netlist scrambling", *IEEE Trans on Reliability(Reliability)*, Dec 2003, v52, pp. 435-443.

Journal papers (under review/preparation)

6. **Swaroop Ghosh**, Debabrata Mahapatra, Georgios Karakonstantis and Kaushik Roy, "Low-voltage high-speed robust hybrid arithmetic units using adaptive clocking", *Trans on VLSI (under review)*.
7. **Swaroop Ghosh**, Saibal Mukhopadhyay, Keejong Kim and Kaushik Roy, "Low power memories for reduction of hold failures in nano-scaled technologies", (in preparation).
8. Patrick Ndai, Nauman Rafique, **Swaroop Ghosh**, Swarup Bhunia, Mithuna Thottethodi and Kaushik Roy, "Trifecta: A non-speculative scheme to exploit common, data-dependent subcritical paths", *Transactions on VLSI (to be submitted)*.
9. Jing Li, Aditya Bansal, **Swaroop Ghosh** and Kaushik Roy, "An Alternate Design Paradigm for Low Power, Low-Cost Systems using Scaled LTPS TFT", *ACM Trans. on Emerging Devices*, (under review).
10. **Swaroop Ghosh**, Arijit Raychowdhury, and Kaushik Roy, "An efficient speed binning methodology for parametric yield improvement in nano-scale technology", (Under review in *Journal on Electronic Testing: Theory and Applications*).

Conference papers

Computer-Aided Design

11. **Swaroop Ghosh**, Jung-Hwan Choi, Patrick Ndai, and Kaushik Roy, "O²C: Occasional Two-Cycle operations for dynamic thermal management in high performance embedded In-Order microprocessors", Under Review.
12. **Swaroop Ghosh**, Patrick Ndai, and Kaushik Roy, "A novel low overhead fault tolerant Kogge-Stone adder using adaptive clocking", *Design, Automation and Test in Europe (DATE)*, 2008.
13. **Swaroop Ghosh** and Kaushik Roy, "Exploring High-Speed Low-Power Hybrid Arithmetic Units at Scaled Supply and Adaptive Clock-Stretching", to appear in *Asia-Pacific Design Automation Conference (ASPDAC)*, 2008.
14. **Swaroop Ghosh**, Swarup Bhunia and Kaushik Roy, "Low overhead circuit synthesis for temperature adaptation using dynamic voltage scheduling", *Design, Automation and Test in Europe (DATE)*, 2007.
15. **Swaroop Ghosh** and Kaushik Roy, "Low-power, process- and temperature tolerant logic design for scaled technologies", *SRC TECHCON*, 2007.
16. **Swaroop Ghosh**, Saibal Mukhopadhyay, Keejong Kim and Kaushik Roy, "Self-calibration technique for reduction of hold failures in low-power nano-scaled SRAM", *Design Automation Conference (DAC)*, 2006.
17. **Swaroop Ghosh**, Swarup Bhunia and Kaushik Roy, "A new paradigm for low-power and robust circuit synthesis under parameter variations using critical path isolation", *International Conference on Computer-Aided Design (ICCAD)*, 2006.

18. Saibal Mukhopadhyay, **Swaroop Ghosh**, Keejong Kim and Kaushik Roy, "Low-power and process tolerant memories in sub-90nm technologies", International System-on-Chip Conference (*SOCC*), 2006.

Circuits and VLSI Testing

19. Jing Li, **Swaroop Ghosh** and Kaushik Roy, "A generic and reconfigurable test paradigm using low-cost integrated Polysilicon TFTs", International Test Conference (*ITC*), 2007.
20. **Swaroop Ghosh**, Pooja Batra, Keejong Kim and Kaushik Roy, "Low-power and process tolerant pipeline design in scaled technologies", Custom Integrated Circuits Conference (*CICC*), 2007.
21. **Swaroop Ghosh**, Swarup Bhunia, and Kaushik Roy, "Shannon expansion based supply-gated logic for improved power and testability", Asian Test Symposium (*ATS*), 2005.
22. Arijit Raychowdhury, **Swaroop Ghosh**, Swarup Bhunia, Debjyoti Ghosh, and Kaushik Roy, "A Novel Delay Fault Testing Methodology using Low-overhead Built-in Delay Sensor", European Test Symposium (*ETS*), 2005.
23. **Swaroop Ghosh**, Kowen Lai, Wen Ben Jone and Shieh-Cheih Chang, "Scan chain fault identification using weight-based m-out-of-n codes for SoC circuits", Asian Test Symposium (*ATS*), 2004.
24. **Swaroop Ghosh**, Patrick Ndai, Swarup Bhunia and Kaushik Roy, "Tolerance to small delay defects by adaptive clock stretching", International On-Line Testing Symposium (*IOLTS*), 2007.
25. **Swaroop Ghosh**, Swarup Bhunia, A. Raychowdhury and Kaushik Roy, "Delay fault localization in test-per-scan BIST using Built-in Delay Sensor", International On-Line Testing Symposium (*IOLTS*), 2006.
26. Arijit Raychowdhury, **Swaroop Ghosh**, and Kaushik Roy "A Novel On-chip Delay Measurement Hardware for Efficient Speed-Binning", International On-Line Testing Symposium (*IOLTS*), 2005.
27. Vinod Narayanan, **Swaroop Ghosh**, Wen Ben Jone and Sunil Ranjan Das, "A Built-In Self-Testing Method for Embedded Multiport Memory Arrays", Instrumentation and Measurement Technology Conference (*IMTC*), 2004.

Posters

1. **Swaroop Ghosh** and Kaushik Roy, "Low-power, process- and temperature tolerant logic design for scaled technologies", SRC TECHCON, 2007.
2. **Swaroop Ghosh**, Debabrata Mohapatra, Georgios Karakonstantis and Kaushik Roy, "CRISTA: A process-tolerant, low voltage design methodology using adaptive clocking for high-performance processors", GSRC Annual Symposium, 2007. overhead
3. Nilanjan Banerjee, **Swaroop Ghosh**, Georgios Karakonstantis, Dababrata Mohapatra, Jung Hwan Choi, Kaushik Roy, "Yield-Centric Design Framework for Low Voltage Robust Systems", GSRC Annual Symposium, 2007.
4. **Swaroop Ghosh**, Swarup Bhunia and Kaushik Roy, "A new paradigm for low-power and robust circuit synthesis under process variations using critical path isolation", GSRC Annual Symposium, 2006.

PATENTS

1. Jing Li, **Swaroop Ghosh** and Kaushik Roy, "Generic and reconfigurable test paradigm using low-cost integrated Polysilicon TFTs", Patent filed with Purdue University.
2. **Swaroop Ghosh**, Saibal Mukhopadhyay, Keejong Kim and Kaushik Roy, "Self-calibration technique for reduction of hold failures in low-power nano-scaled SRAM", Patent filed with Purdue University.
3. **Swaroop Ghosh**, Swarup Bhunia and Kaushik Roy, "A new paradigm for low-power and robust circuit synthesis under parameter variations using critical path isolation". Patent filed with Purdue University.

PRESENTATIONS

1. "Low circuit synthesis for temperature adaptation using dynamic voltage scheduling", Design, Automation and Test in Europe (*DATE*), 2007.
2. "Process Variation Tolerant Low Power DCT Architecture", Design, Automation and Test in Europe (*DATE*), 2007.
3. "Process tolerant beta-ratio modulation for ultra-dynamic voltage scaling", Design, Automation and Test in Europe (*DATE*), 2007.
4. "Carbon Nanotube Electronics: Devices and Possible Circuit and Systems Implications", Design, Automation and Test in Europe (*DATE*), 2007.
5. "Low-power, process- and temperature tolerant logic design for scaled technologies", SRC TECHCON, 2007.
6. "Low-power and process tolerant pipeline design in scaled technologies", Custom Integrated Circuits Conference (*CICC*), 2007.
7. "CRISTA: A Low-Power Process- and Temperature-Tolerant Adaptive Methodology for Scaled Technologies", LSI Technologies, 2007.
8. "Self-calibration technique for reduction of hold failures in low-power nano-scaled SRAM", Design Automation Conference (*DAC*), 2006.
9. "A new paradigm for low-power and robust circuit synthesis under parameter variations using critical path isolation", International Conference on Computer-Aided Design (*ICCAD*), 2006.

10. "Sleep transistor variability analysis in Tulsa processor's L2 cache and its test implications", Advanced Test Technology Group, Intel, Oregon, 2006.
11. "A Novel On-chip Delay Measurement Hardware for Efficient Speed-Binning", International On-Line Testing Symposium (*IOLTS*), 2005.
12. "Process Variation Tolerant Online Current Monitor for Fault Immune Systems", International On-Line Testing Symposium (*IOLTS*), 2005.
13. "Reliability Analysis and Yield Prediction of High Performance Pipelined Circuit with respect to Delay Failures in sub-100nm Technology," International On-Line Testing Symposium (*IOLTS*), 2005.

GRADUATE COURSE PROJECTS

- Designed test chip (in 1.2um TSMC) of palindrome recognizer and string reverser circuit.
- Tested the palindrome recognizer chip in VLSI testing project.
- Designed combinational and sequential circuits and implemented low power techniques in low power design course projects.
- Implemented a LC-2 microprocessor in VLSI system design course project.
- Implemented partitioning algorithms like, FM, GA, SA in VLSI design automation project.
- Design and development of Remote Data Acquisition Module.

TECHNICAL SKILLS

- Languages/HDLs: Verilog, C, Perl, FORTRAN, 8085, 8086, 8031
- Operating Systems: UNIX, Windows
- EDA Tools: Cadence Ambient, NC-Verilog, Verilog-XL, Synplicity synthesis tool, Xilinx Alliance Tool, Vericover, Arm Development suite, Quartus-II, Tektronics Logic Analyzer, Bluetooth protocol analyzer
- Circuit Design Tools: HSPICE, Cadence IC Design suite, Magic, Irsim
- Mathematical Software: MATLAB

ASSOCIATION WITH PROFESSIONAL INSTITUTIONS

Member:

- Student member of the Institute of Electrical and Electronics Engineers (IEEE).
- Student member of Semiconductor Research Corporation (SRC).
- Student member of Gigascale Systems Research Center (GSRC).
- Student member of Focus Center Research Program (FCRP).

Referee:

- IEEE Transactions on Circuits and Systems (TCAS-I, TCAS-II).
- VLSI Test Symposium (2005), Asian Test Symposium (2004), Intl. Conf. on Computer Aided Design (ICCAD 2007), Design, Automation and Test in Europe (DATE 2006, 2007, 2008), Intl Test Conference (ITC 2006, 2007).

REFERENCES

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- Prof. Wen-Ben Jone, 836B Rhodes, University of Cincinnati, OH 45221, USA
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- Mr. Sandeep Bharathi, One AMD place, Sunnyvale, CA, USA
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- Mr. Michael Spica, Cypress Semiconductor, 10147 W. Emerald Street Suite 100 Boise, ID 83704 USA
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