
Gate Sizing to Radiation Harden Combinational Logic

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Single-Event Upset (SEU)

- ✓ **State change due to high energy particles: high-energy neutrons or alpha particles**
 - ✓ **SEU's growing more prominent in scaled technologies. With the fixed critical charge,**
 - ❖ **Smaller node capacitance**
 - ❖ **Smaller operation voltage (V_{DD})**
 - ✓ **Memory elements are more susceptible to SEU's: Growing impact on the combinational logic circuits**
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Radiation Hardening Techniques

✓ Device

- ❖ Extra doping layer, well structures (isolation)
- ❖ Buried layer: internal electric field

✓ Circuit

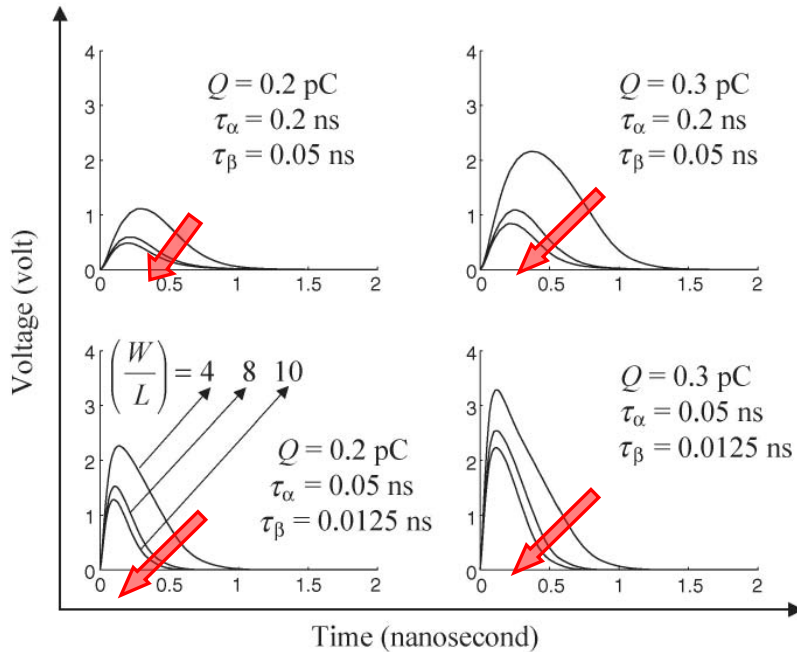
- ❖ Feedback elements: slowing propagation
- ❖ Avoid using dynamic logic and floating nodes
- ❖ Soft-error-tolerant latches

✓ System

- ❖ fault detection: error detection and correction codes
- ❖ fault tolerance

Sizing-based Radiation Hardening is proposed

Sizing and SEU Vulnerability



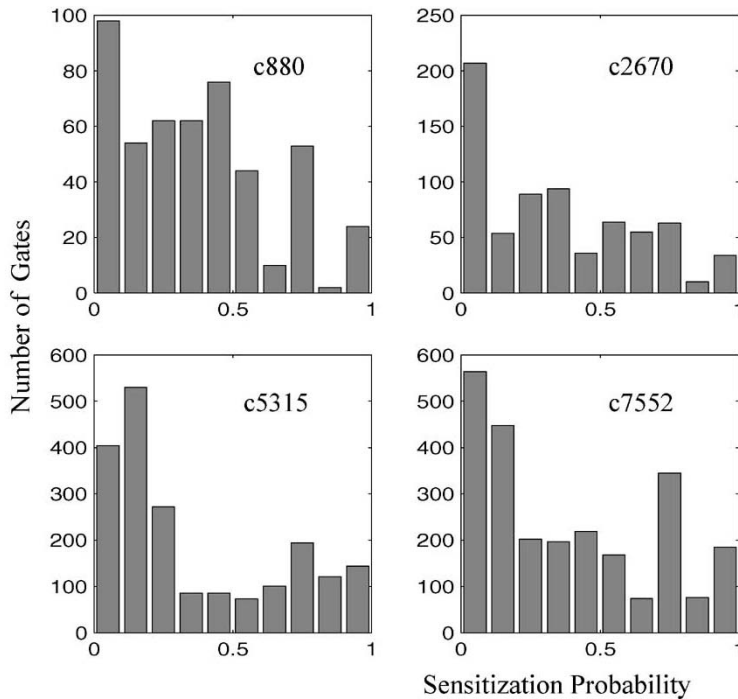
$$I_{in}(t) = \frac{Q}{(\tau_a - \tau_b)} \left(e^{-\frac{t}{\tau_a}} - e^{-\frac{t}{\tau_b}} \right)$$

- ✓ **Effect of sizing on SEU**
 - ❖ **Q**: Injected charge
 - ❖ **τ_a**: collection time of junction
 - ❖ **τ_b**: ion-track establishment time

- ✓ **Larger sizes reduce the susceptibility of node to SEU's**

- ✓ **Still, we can't apply upsizing to all the logic gates: area, delay & power overheads**

SEU Masking Factors



- ✓ **A metric of SEU susceptibility for different logic gate**
 - ❖ **Logical: functional sensitization**
 - ❖ **Electrical: attenuation**
 - ❖ **Temporal: timing window**
- ✓ **Logic gates with higher sensitization probability is more vulnerable to SEU's: Primary target of resizing**

Computing Optimal Size

$$C_{total} \left(\frac{dV_{out}}{dt} \right) = I_{in}(t) - \left(\frac{W}{L} \right) I_D(V_{out})$$

Calculate t_{MAX} at $V_{out} = 0.5V_{DD}$

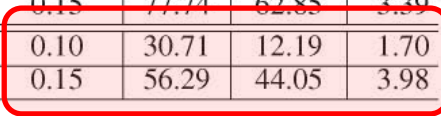
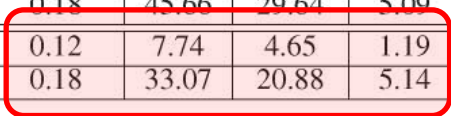
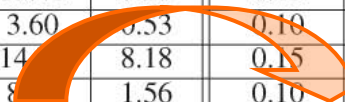
$$\left(\frac{W}{L} \right)_{min} = \frac{I_{in}(t_{max})}{I_D(0.5V_{DD})}$$

- ✓ Each target gate is sized using the optimal solution
 - ✓ Optimal size is applied to each gate in the order of sensitization probability
 - ✓ When the target coverage is met or order constraint is violated, algorithm stops
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Simulation Results

Name (PIs, POs, gates)	Circuit Function	Targeted Gates (%)	100 nm Technology				70 nm Technology			
			Charge (pC)	Overhead (%)			Charge (pC)	Overhead (%)		
				Area	Power	Delay		Area	Power	Delay
x2 (10, 7, 56)	Logic	58.9	0.12	5.38	5.25	1.84	0.10	34.41	13.23	2.34
			0.18	34.41	23.78	6.13	0.15	63.44	49.90	7.34
cu (14, 11, 59)	Logic	44.1	0.12	4.76	1.84	0.00	0.10	18.10	9.04	1.44
			0.18	21.90	17.49	3.28	0.15	40.00	35.46	6.41
b9 (41, 21, 211)	Logic	48.8	0.12	6.70	4.90	1.08	0.10	24.30	13.19	2.33
			0.18	27.09	22.56	2.55	0.15	44.13	44.77	2.36
c432 (36, 7, 320)	Priority decoder	55.3	0.12	9.93	5.81	2.39	0.10	29.08	14.72	0.66
			0.18	36.17	25.22	6.73	0.15	58.33	48.51	1.01
c880 (60, 26, 512)	ALU and control	60.7	0.12	7.28	4.12	1.19	0.10	35.32	12.54	0.00
			0.18	34.37	21.33	4.58	0.15	64.32	47.68	0.08
c499 (41, 32, 650)	Error correcting	66.1	0.12	11.63	6.24	2.66	0.10	35.41	11.37	2.49
			0.18	43.13	23.05	8.49	0.15	62.79	45.89	3.48
c1355 (41, 32, 653)	Error correcting	61.1	0.12	13.22	6.83	0.82	0.10	30.36	12.26	2.35
			0.18	43.49	24.09	5.25	0.15	56.32	43.88	6.63
c1908 (33, 25, 699)	Error correcting	51.5	0.12	9.05	4.69	1.06	0.10	31.90	11.20	1.89
			0.18	32.09	16.03	3.19	0.15	51.68	36.12	2.48
c2670 (233, 140, 756)	ALU and control	51.3	0.12	1.84	0.60	0.00	0.10	27.68	6.11	2.41
			0.18	25.08	13.34	5.00	0.15	51.30	33.51	10.40
c3540 (50, 22, 1467)	ALU and control	54.9	0.12	10.75	7.38	1.46	0.10	35.62	18.78	2.50
			0.18	36.89	27.92	4.78	0.15	63.55	57.38	2.89
c5315 (178, 123, 2115)	ALU and selector	59.1	0.12	4.28	2.55	0.68	0.10	31.77	10.14	0.36
			0.18	29.56	17.80	1.50	0.15	57.96	43.37	0.48
c7552 (207, 108, 2534)	ALU and control	57.5	0.12	4.83	2.72	0.42	0.10	23.98	8.17	1.46
			0.18	28.91	15.43	2.25	0.15	53.17	38.31	2.60
i10 (257, 224, 2646)	Logic	39.8	0.12	5.68	3.60	0.53	0.10	23.68	8.97	0.82
			0.18	24.19	14.00	8.18	0.15	43.36	29.07	6.13
c6288 (32, 32, 4507)	16-bit multiplier	68.9	0.12	12.90	8.00	1.56	0.10	43.29	19.87	2.68
			0.18	45.66	29.64	5.09	0.15	77.74	62.85	3.39
Average Overhead (%)			0.12	7.74	4.65	1.19	0.10	30.71	12.19	1.70
			0.18	33.07	20.88	5.14	0.15	56.29	44.05	3.98

Technology Scaling Trend



Drawbacks

- ✓ **Large overhead in area: 57% for 70nm**
 - ✓ **Compatibility with standard cell library**
 - ✓ **Compatibility with the current synthesize algorithm (e.g., sizing for delay)**
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