

A Design Approach for Radiation- hard Digital Electronics

R. Gard and N. Jayakumar

Design Automation Conference 2006

Simulation Setup

- Charge deposited (Q) at a node is given by

$$Q = 0.01036 \cdot L \cdot t$$

where : L is Linear Energy Transfer (MeV/cm²/mg)
 t is the depth of the collection volume (μm)

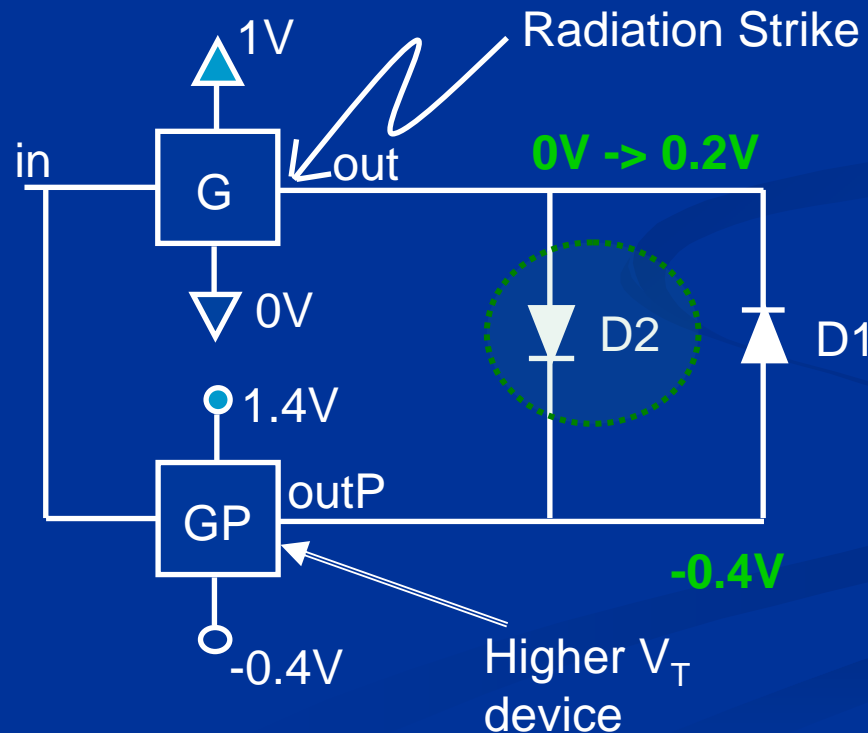
- Resulting current pulse is described as

$$I(t) = \frac{Q}{(\tau_\alpha - \tau_\beta)} (e^{-t/\tau_\alpha} - e^{-t/\tau_\beta})$$

where: τ_α is the collection time constant
 τ_β is the ion track establishment constant

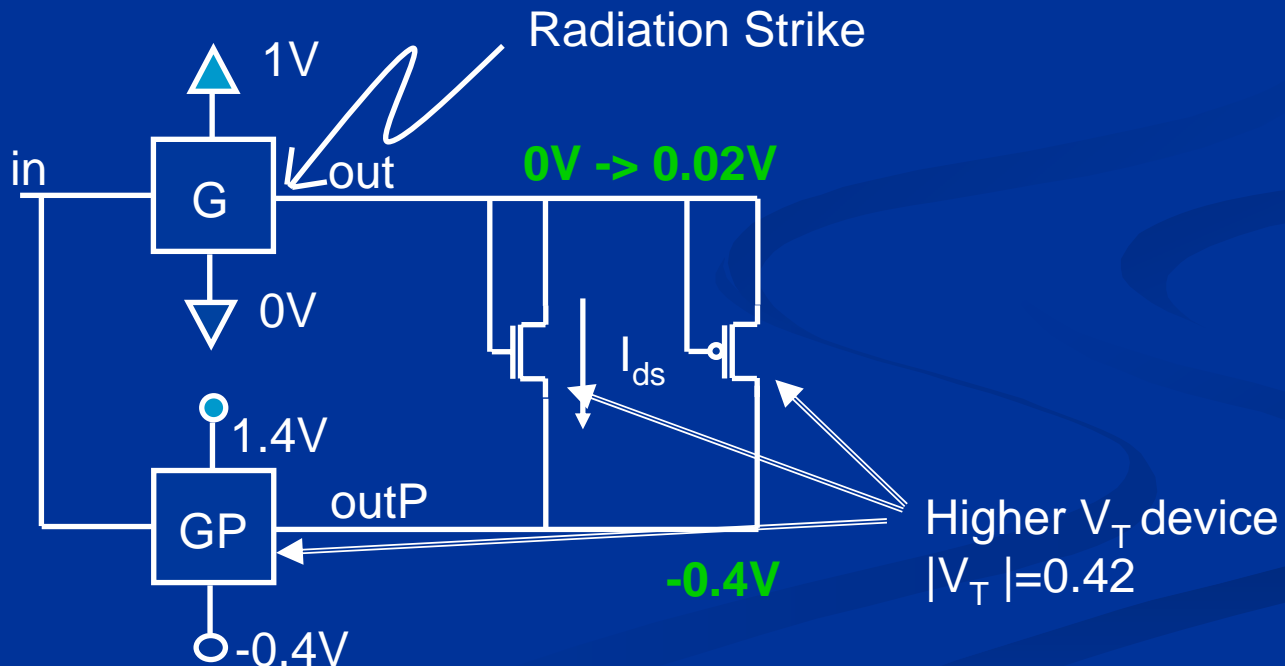
Radiation Hardened Cell

- Radiation hardening of standard cell
 - PN Junction Diode based SEU Clamping Circuits
 - Additional gate GP used as a shadow gate

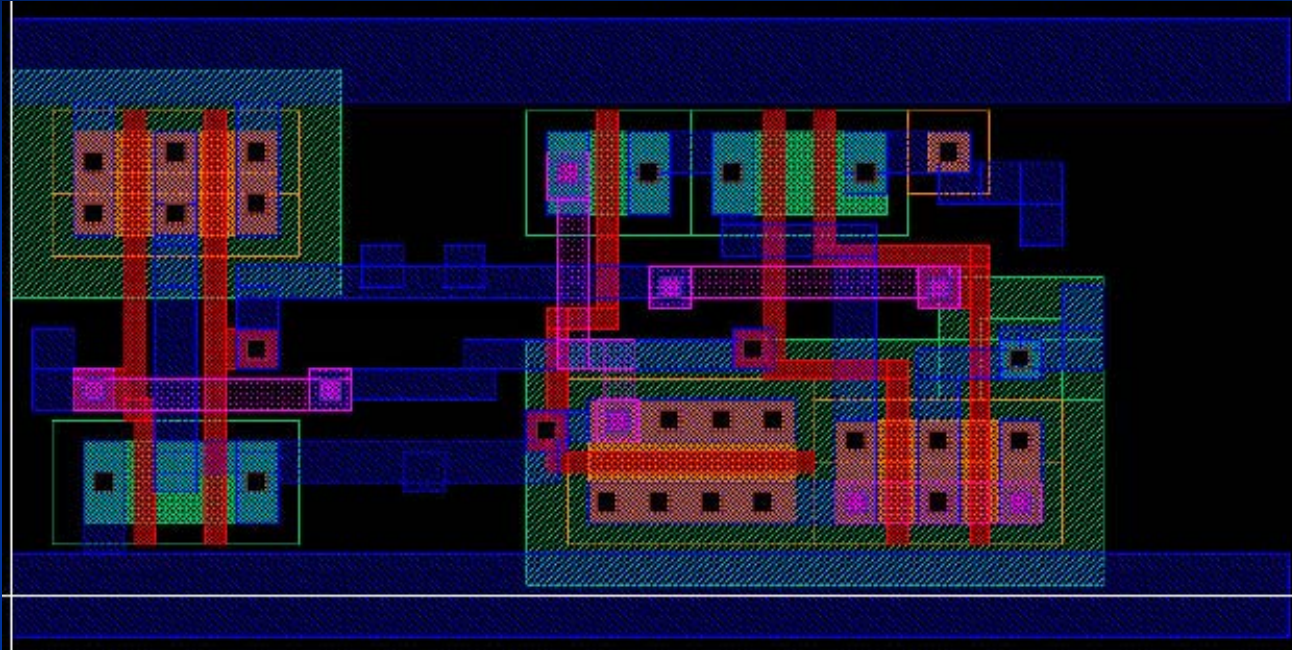


Radiation Hardening

- Radiation hardening of standard cell
 - Diode-connected Device based SEU Clamping Circuits

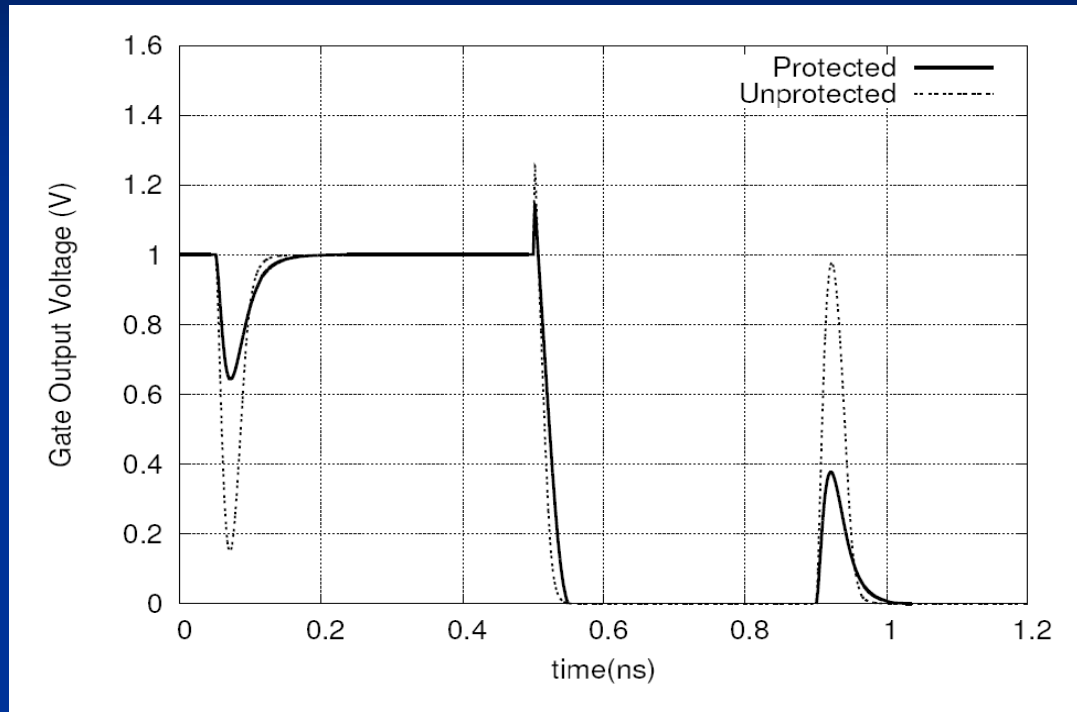


Diode-based RAD-hard Cell



- Designed a radiation hardened library of cells.
 - Diode connected devices were used
 - Slightly worse protection performance than PN junction diode based protection, but
 - Had a lower area penalty.

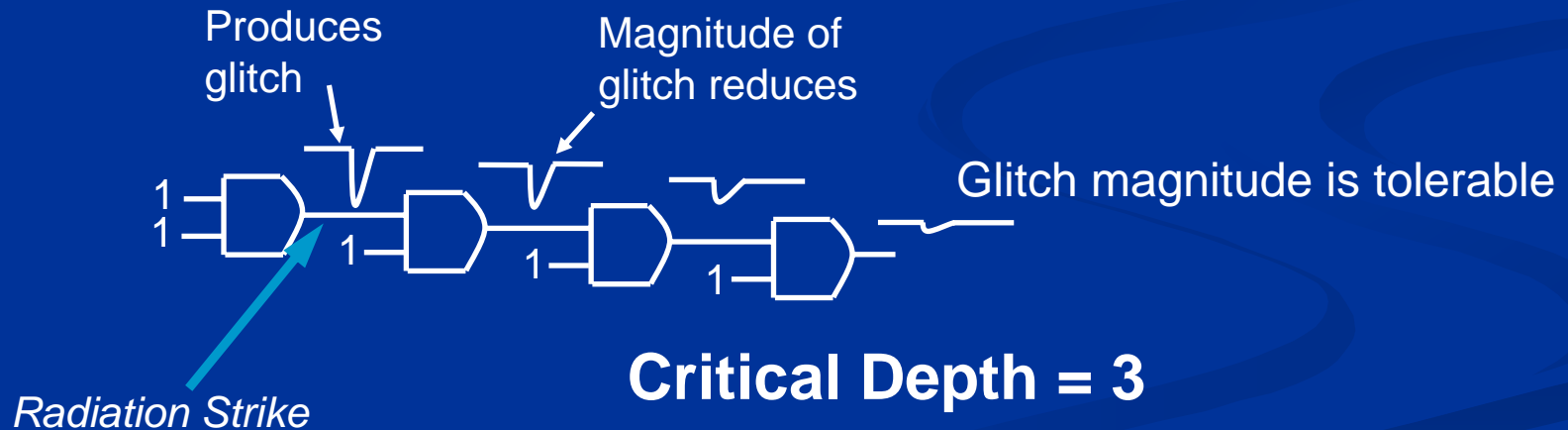
Protection Performance



- Radiation strike at output node. $Q = 4fC$, $t_a = 10ps$
- Good protection performance.
- 4% overhead in delay. More than 100% overhead in area.

RAD-HARD Algorithm

- Critical depth for a gate
 - Computed for each hardened cells
 - Consider 2 input AND gate



Simulation Results

Ckt.	Delay Mapped			Delay Mapped		
	Regular	Hardened	%Ovh	Regular	Hardened	%Ovh
alu2	959.113	976.987	1.86	1439.44	1728.9	20.11
alu4	1247.762	1259.695	0.96	2470.09	3343.15	35.35
C1355	711.149	720.345	1.29	1728.9	2279.11	31.82
C1908	1085.28	1093.79	0.78	1799.46	2279.11	26.66
C3540	1414.443	1424.782	0.73	4022.1	5077.99	26.25
C499	711.149	720.345	1.29	1728.9	2279.11	31.82
C880	1405.322	1554.847	10.64	1397.26	2252.45	61.2
dalu	1056.534	1077.134	1.95	3310.85	3986.66	20.41
des	1615.74	1645.817	1.86	12139.63	15074.93	24.18
frg2	792.849	836.477	5.5	2611.21	4057.69	55.4
i2	363.611	382.298	5.14	872.61	948.64	8.71
i3	172.865	184.777	6.89	495.51	566.44	14.32
C7552	2005.371	2070.491	3.25	7953.07	9576.58	20.41
i10	1931.211	2002.74	3.7	7705.32	11291.18	46.53
AVG			3.28			30.22

- 3.28% overhead in delay
- 30.22% overhead in area

Conclusion

- A novel circuit design approach for radiation hardened circuits is proposed.
- Shadow gates and protecting diode-connected devices used for RAD-hard cell.
- An efficient algorithm is proposed replace fewer gates to help minimize the area and delay penalties.
 - Only 30% area penalty and 4% delay penalty on average