Estimation of NBTI Degradation Using I_{DDQ} Measurement

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Abstract

Negative Bias Temperature Instability (NBTI) has emerged as a major reliability degradation factor in nano-scale CMOS technology. In this paper, we analyze the impact of NBTI degradation in both the maximum operating frequency (f_{MAX}) and the total standby leakage current (I_{DDQ}) of digital CMOS circuits. Our analysis shows that due to NBTI, both f_{MAX} and I_{DDQ} reduce with time with a fix exponent of 1/6 ($\sim t^{1/6}$). Based on this analysis, we develop temporal f_{MAX}-I_{DDQ} model and apply it to several ISCAS'85 benchmark circuits designed using BPTM 70nm file. Results show that f_{MAX} and I_{DDQ} can reduce by more than 8% and 30% in 3 years operation time, respectively. Furthermore, we show that f_{MAX} and I_{DDQ} degradations are highly correlated throughout the operating lifetime, and using this fact, one can avoid expensive f_{MAX} testing and predict f_{MAX} degradations as a function of I_{DDQ} measures.

[*Keywords:* Temporal Reliability, NBTI, I_{DDQ}, f_{MAX}]

Introduction

For past decades, temporal reliability of MOSFET device has been considered as one of the key issue in the device engineering field. Reliability degradation in MOSFET device can be due to several physical mechanisms such as Hot Carrier Injection (HCI), Negative Bias Temperature Instability (NBTI) [4,15], Time Dependent Dielectric Breakdown (TDDB), radiation induced damage, etc. Such degradations can cause performance degradations (e.g., timing or power) or even an unrecoverable malfunction in fabricated chip during its operation. As a result, it is becoming more important to be able to characterize and predict the temporal behavior of digital circuits through efficient characterization procedures.

In this work, we focus on an efficient characterization methodology of NBTI in PMOS transistors: one of the dominant reliability degradation factors in nano-scale MOSFET devices. In bulk MOSFET structure, undesirable *Si* dangling bonds exist due to structural mismatch at the *Si*-SiO_2 interface. These dangling bonds act as charged interfacial traps. Conventionally, hydrogen passivation is applied to the *Si* surface after the oxidation process to transform dangling *Si* atoms to *Si-H* bonds. However, with time, these *Si-H* bonds can break during operation (ON-state, negative gate bias for the PMOS). The broken bonds act as interfacial traps and increase the threshold voltage (V_t) of the device, thus affecting the performance of the IC. NBTI impact gets even worse in scaled technology due to higher operation temperature and the usage of ultra thin oxide (i.e., higher oxide field).

Recently, efficient post-silicon testing/characterization techniques have been proposed in the literature to characterize the MOSFET reliability degradations. In [10], TDDB was characterized by tracking a temporal standby leakage shift of a circuit. Based on the IC measurement data, it was validated that I_{DDQ} has a highly correlated behavior with the degradation of the silicon dioxides. On the other hand, in [9], it was shown that the NBTI degradations have a direct impact on the critical speed path (f_{MAX}) of a circuit. By adjusting the Fluorine implants, researchers have examined the possibility of f_{MAX} testing on characterizing the lifetime NBTI behavior of CMOS devices. Reddy & Krishnan et. al. [7,14] further explored f_{MAX} degradation under NBTI and proposed an efficient parametric modeling scheme for efficient testing. In [12], an analytical justification proving that the maximum circuit delay degradation due to NBTI closely follows the same power dependency with respect to the time as the V_t degradation is proposed.

From above discussions, we observe that all prior research works on NBTI impact have focused on characterizing the NBTI degradation in terms of maximum operating frequency f_{MAX}. However, in a normal testing environment, test cost (both in terms of time and complexity) for f_{MAX} testing is far higher than I_{DDQ} testing [13]. Hence, it would be meaningful to explore the possibilities of characterizing NBTI degradations in the post-Silicon test phase using I_{DDQ}. In this work, we demonstrate the analytical basis of I_{DDQ} testing for the post-Silicon NBTI degradation based on the temporal f_{MAX}-I_{DDQ} correlation. Specifically,

1. An analytical temporal model of circuit I_{DDQ} considering the NBTI degradation is proposed. Further, it is shown and proved that the percentage degradation in circuit I_{DDQ} closely follows that of V_t degradation in a single PMOS transistor.

2. Using this relationship, we also show that I_{DDQ} degradation is highly correlated with the f_{MAX} degradation throughout the device lifetime. This correlation can be used to predict and characterize the NBTI through I_{DDQ}. Hence, on-chip I_{DDQ} measure can be used to predict NBTI degradation.

The rest of the paper is organized as follows. In the following section, we explain the physics of NBTI and model the temporal V_t degradation in PMOS transistors in a compact analytical form. Also, the impact of temporal V_t degradation on maximum operating frequency f_{MAX} and total circuit leakage I_{DDQ} is analyzed and modeled. Using the proposed model, we then establish a correlation of f_{MAX} and I_{DDQ} degradation over a device lifetime. Furthermore, using this relationship, the possibility of I_{DDQ} testing as an alternative to the f_{MAX} testing is proposed. Finally, we conclude the paper.

Temporal Performance Degradation Under NBTI

In this section, we analyze the impact of NBTI on temporal performance degradation at both device and circuit level. In the first part of the section, we develop an analytical expression for the temporal V_t degradation in PMOS transistor due to NBTI based on the Reaction-Diffusion (R-D) framework proposed in [1,3,8]. Based on the transistor level degradation model, in the later part of the section, we will show how time dependent increase in V_t affects the maximum operating frequency f_{MAX} and the standby leakage current I_{DDQ} at the circuit level.

Temporal V_t increase

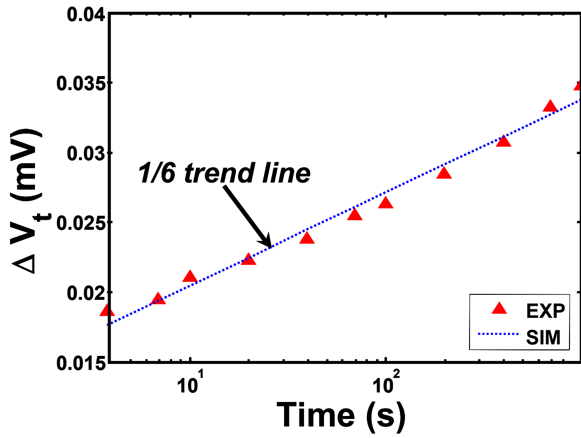

FIGURE 1. COMPARISON BETWEEN EXPERIMENTAL DATA FROM [6] AND OUR PROPOSED MODEL.

TABLE 1. AC DEGRADATION FACOTR α_S FOR DIFFERENT SIGNAL PROBABILITIES S_i. α_S SCALES DOWN THE BOND BREAKING RATE k_F.

Signal Probability (S_i)	AC degradation factor $\alpha_S(S_i)$
0.25	0.50
0.50	0.71
0.75	0.87

NBTI is the result of trap generation at *Si-SiO*$_2$ interface in negatively biased PMOS transistors at elevated temperatures. The interaction of inversion layer holes with hydrogen-passivated *Si* atoms can break the *Si-H* bonds, creating interface traps and neutral atomic *H* atoms, which can diffuse away from the interface (through the oxide) or can anneal an existing trap. The generation of interface trap has been modeled using the Reaction-Diffusion (R-D) framework [1,3,4] and showed a power dependency on time with a fixed time exponent of 0.25. However, an atomic-*H* only model has recently been shown to be inadequate to interpret experimental data. Rather, it is now believed that the broken *H* atoms form H_2 molecules, which requires a generalization of the classical R-D model.

General physical mechanism of H_2 based NBTI degradation is explained in [3,8]. Generation of interfacial traps and the reverse annealing of *Si-H* bond can be expressed as follows,

$$\frac{dN_{IT}}{dt} = k_F(N_0 - N_{IT}) - k_R N_{IT} N_H^{(0)}, \tag{1}$$

where N_{IT} is the density of interfacial trap, N_0 is the initial *Si-H* bond density and $N_H^{(0)}$ is the hydrogen density at the interface. k_F and k_R represent *Si-H* dissociation rate constant and reverse annealing rate, respectively. N_{IT} can be obtained by integrating the number of generated hydrogen molecules (H_2) inside the oxide and can be computed as,

$$N_{IT} = \int_0^{\sqrt{D_{H_2}t}} N_{H_2}(y,t)dy = \frac{N_{H_2}^{(0)}}{2}\sqrt{D_{H_2}t}, \tag{2}$$

where t is the elapsed time, D_{H2} is the diffusion coefficient of H_2. $N_{H2}(y,t)$ and $N_{H2}^{(0)}$ are the H_2 density in y (vertical depth toward the oxide) at time t and H_2 density at the interface (y=0), respectively. Density of H_2 and H can be connected through the rate equation (i.e., $H+H \rightarrow H_2$) and can be expressed as,

$$k_1 N_H^{(0)2} = k_2 N_{H_2}^{(0)} \rightarrow N_H^{(0)} = \sqrt{\frac{k_2}{k_1} N_{H_2}^{(0)}}, \tag{3}$$

where k_1 and k_2 are the rate constants. Next, by applying Eq. (2) to Eq. (3), surface hydrogen density can be expressed as,

$$N_H^{(0)} = \frac{\sqrt{2N_{IT}}}{(D_{H_2}t)^{1/4}}\left(\frac{k_2}{k_1}\right)^{1/2}. \tag{4}$$

Finally, by merging Eqs. (1)~(4), we can solve for N_{IT} as,

$$N_{IT}(t) = \left(\frac{k_1}{2k_2}\right)^{1/3}\left(\frac{k_F N_0}{k_R}\right)^{2/3}\left(D_{H_2}t\right)^{1/6} \propto t^{1/6}, \tag{5}$$

where we can observe that the trap generation has a power dependency on time with a fixed exponent of **1/6**.

In a real circuit operation, the effective ON-time of transistors is bounded by its input signal probability. In our work, we define the Signal Probability S_i at the input of gate i as a fraction of operating cycle which contributes to the NBTI degradation, that is, logic LOW in CMOS since PMOS transistors mainly get affected by NBTI. Depending on S_i, bond-breaking rate k_F is being scaled down by the AC degradation factor α_S. α_S values for various S_i's are computed using the R-D framework [3]. Table 1 shows several AC degradation factors for different signal probabilities. Considering this, trap generation N_{IT} can be now transformed into an increase in V_t as follows,

$$\Delta V_t(t) = (m+1)\frac{qN_{IT(t)}}{C_{OX}} = K_C \times \alpha(S_i)^{2/3} \times t^{1/6}, \tag{6}$$

where m is a mobility degradation factor and K_C is a constant factor from Eq. (5). Fig. 1 shows a comparison between our model and the experimental data from [6] where we can observe a good match over a wide range as well as the power dependency of V_t degradation with a fixed time exponent of **1/6**.

f_{MAX} degradation

Using the temporal V_t model proposed in the previous section, we can now estimate the f_{MAX} degradation in the circuit. It was shown in [12] that the increase in maximum circuit delay also follows the same exponent of V_t degradation as follows,

$$\Delta\tau_{ckt}(t)/\tau_{ckt}(t) \propto t^{1/6} \tag{7}$$

where $\tau_{ckt}(t)$ is the maximum circuit delay at time t, and $\Delta\tau_{ckt}(t)$ is increase in maximum circuit delay ($=\tau_{ckt}(t) - \tau_{ckt}(0)$) after time t. Using this result, it can be shown that the degradation in f_{MAX} can be also expressed as a power of time with a fixed exponent of **1/6** as

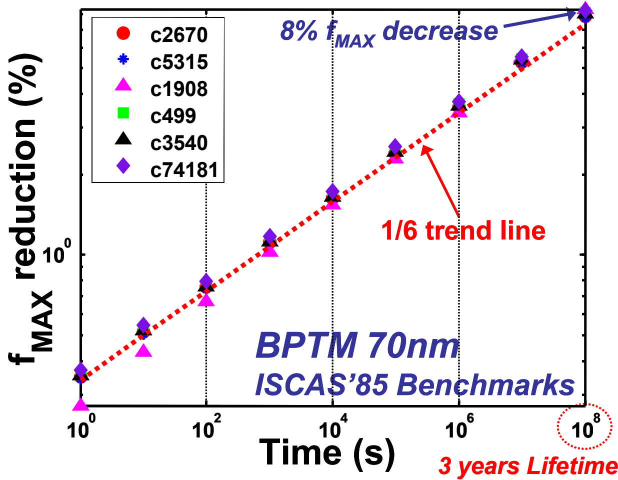

FIGURE 2. TEMPORAL f_{MAX} DEGRADATION FOR 3 YEARS IN SEVERAL ISCAS'85 BENCHMARK CIRCUITS.

TABLE 2. RISING DELAY DEGRADATION IN SEVERAL STANDARD CELLS. EACH CELL IS DESIGNED USING BPTM 70NM TECHNOLOGY FILE.

Logic Cell	fanin	Delay (ps)		Degradation (%)
		t=0	3 years	
INV	1	13.77	16.77	21.81
NAND	2	16.86	19.88	17.93
NAND	3	19.57	22.45	14.75
NOR	2	17.26	21.89	26.79
NOR	3	23.80	30.19	26.87

follows,

$$\frac{\Delta\tau_{ckt}(t)}{\tau_{ckt}(0)} = \left(\frac{1}{f_{MAX}(t)} - \frac{1}{f_{MAX}(0)}\right) / \left(\frac{1}{f_{MAX}(0)}\right) = \frac{\Delta f_{MAX}(t)}{f_{MAX}(0)} \propto t^{1/6} \tag{8}$$

where $f_{MAX}(t)$ is the maximum operating frequency at time t, and is in reciprocal relationship with $\tau_{ckt}(t)$ (i.e., $\tau_{ckt}(t) = 1/f_{MAX}(t)$).

The f_{MAX} degradation behavior introduced in Eq. (8) was verified through a timing simulation. First, V_t model introduced in Eq. (6) was integrated into an analytical delay model proposed in [18]. All relevant parameters in Eq. (6) are calibrated for the BPTM 70nm technology node [2]. Delay computation was verified with HSPICE simulation and showed negligible errors. NBTI impact on the rising delays of several standard cells is summarized in Table 2 (i.e., note that in a single cell-level, rising delays are only affected by NBTI). Then, we developed a NBTI-aware Static Timing Analysis (STA) [19] tool to compute the maximum circuit delay after desired operating time. STA is a standard method of computing worst case circuit delay by propagating the maximum gate delay from the primary inputs to outputs in a logical order. STA has shown its effectiveness in estimating circuit delay in the pre-Silicon design phase and has been widely used in the industry. Fig. 2 shows the temporal f_{MAX} degradations for several ISCAS benchmark circuits obtained from our STA. As predicted by Eq. (8), f_{MAX} also shows a power dependency to time with a fixed exponent of **1/6**. In a 3 years time period, we can observe up to 8% decrease in f_{MAX}.

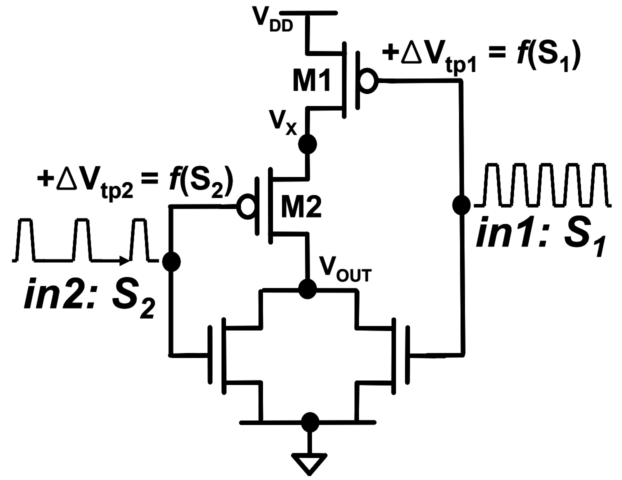

FIGURE 3. LEAKAGE COMPUTATION IN 2 INPUT NOR GATE

I_{DDQ} degradation

As discussed in the previous section, I_{DDQ} of a circuit is measured as a total standby leakage current at a fixed DC input. As PMOS V_t increases with time due to NBTI, leakage current through those PMOS transistors decrease exponentially, and as a result, I_{DDQ} also reduces with time.

In order to develop an accurate I_{DDQ} model, we first start by generating temporal leakage model for each standard cell. In our work, we only considered the subthreshold leakage current as the major contribution of overall I_{DDQ}. This assumption is based on the fact that unlike other leakage components (e.g., gate, junction leakages), subthreshold leakage is most susceptible to the V_t changes [17]. Fig. 3 shows an example of a 2 input NOR gate. Depending on the signal probabilities (S_1 and S_2) of the input signals *in1* and *in2*, degradation in PMOS V_t's (ΔV_{tp1} and ΔV_{tp2}) can be computed using Eq. (6) for any given operation time.

On computing each ΔV_{tp}, degradation in cell leakage can be calculated under the framework proposed in [11]. First, nominal leakage (i.e., at time 0) values for different input vectors (e.g., 00, 01, 10 and 11 for 2 input gates) are characterized using HSPICE simulations. Then, the nominal leakage values are factored according to V_t degradations as follows,

$$\begin{aligned} I_{01}(t) &= I_{01}(0) \times 10^{-\Delta V_{tp2}/S} \\ I_{10}(t) &= I_{10}(0) \times 10^{(-\Delta V_{tp2}\lambda_D - \Delta V_{tp1})/S} \\ I_{11}(t) &= I_{11}(0) \times 10^{[(-\Delta V_{tp2} - \Delta V_{tp1})\lambda_D - \Delta V_{tp1}]/S} \end{aligned} \tag{9}$$

where S and λ_D are subthreshold slope and DIBL factor, respectively. $I_{01}(t)$ and $I_{01}(0)$ represent cell leakage for input vector '01' (in1:0 and in2:1) at time 't' and '0' (nominal leakage), respectively. Similar notation applies for I_{10} and I_{11}. Note that I_{00} component does not suffer from NBTI for NOR type gates since no PMOS transistors are on the leakage path (i.e., similarly, for 2 input NAND gates, I_{00}, I_{01}, and I_{10} does not suffer from NBTI). For NAND type gates, the only time dependent component I_{11} can be computed as,

$$I_{11}(t) = \frac{I_{11}(0)}{2} \times \left(10^{-\Delta V_{tp1}/S} + 10^{-\Delta V_{tp2}/S}\right) \tag{10}$$

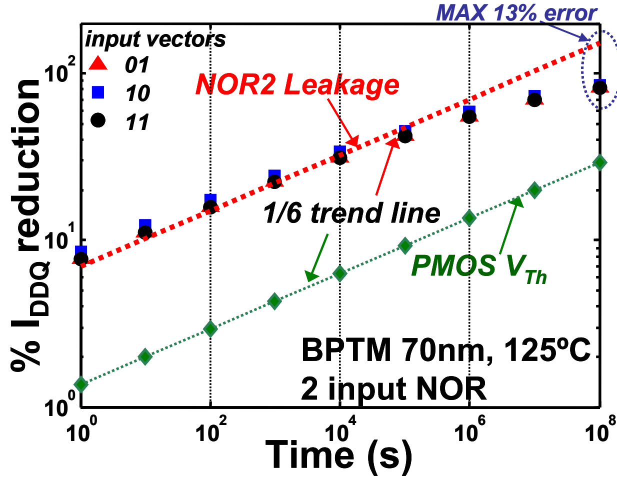

FIGURE 4. LEAKAGE DEGRADATION OVER 3 YEARS IN 2 INPUT NOR GATE FOR DIFFERENT INPUT VECTORS.

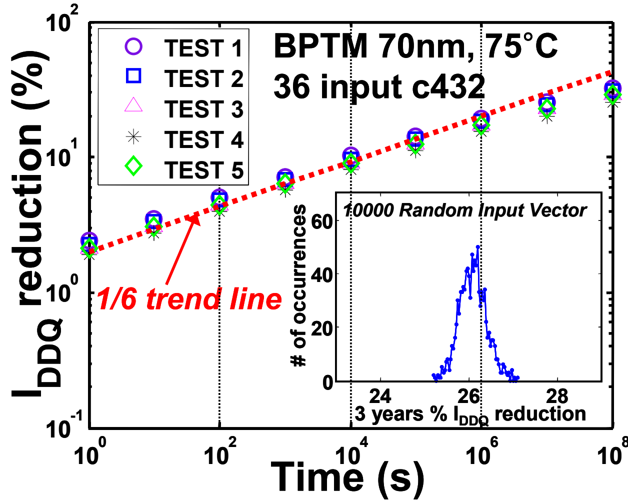

FIGURE 5. LEAKAGE DEGRADATION OVER 3 YEARS IN ISCAS C432 BENCHMARK FOR 5 DIFFERENT TEST INPUT VECTORS.

where ΔV_{tp1} and ΔV_{tp2} represent V_t degradation in two parallel transistors of PUN side of 2 input NAND gate. Fig. 4 shows the percentage reduction in 2 input NOR leakage for 3 years time period for different input vectors obtained from our model. For this example, each PMOS transistor is equally degraded due to 50% signal probability of inputs (Eq. (6)). The resulting leakage reduction clearly follows the **same power law as the f_{MAX} degradation with a same exponent of 1/6**. This behavior can be explained by the following analysis. Using an analytical expression of subthreshold leakage current [17], leakage reduction R_{leak} in a single PMOS transistor can be written as follows,

$$I_{leak}(t) = \beta(m-1)v_T^2 e^{\frac{V_g - V_t(t)}{mv_T}}\left(1 - e^{-\frac{V_{ds}}{v_T}}\right)$$
$$R_{leak} = \frac{\Delta I_{leak}(t)}{I_{leak}(0)} = 1 - e^{-\Delta V_t(t)/mv_T} \tag{11}$$
$$= \frac{\Delta V_t(t)}{mv_T} - \frac{1}{2}\left(\frac{\Delta V_t(t)}{mv_T}\right)^2 + \ldots$$

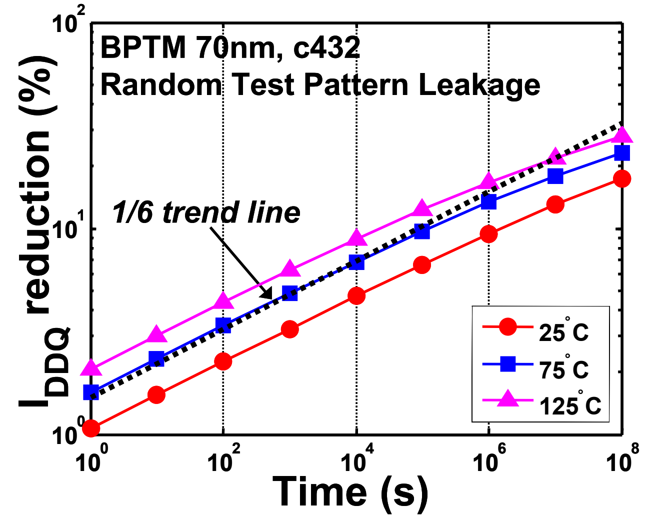

FIGURE 6. I_{DDQ} DEGRADATIONS OVER 3 YEARS IN ISCAS C432 BENCHAMRK FOR 3 DIFFERENT STRESS TEMPERATURE.

where m is the body-effect coefficient and v_T is the thermal voltage ($=kT/q$). When ΔV_t are fairly less than the denominator mv_T (approximately 40mV at 125̊C), leakage reduction R_{leak} can be approximated by the first term which shows a linear dependency with respect to ΔV_t. This is the reason why leakage reduction shows a power dependency to operating time with a fixed exponent of 1/6 as shown in Fig. 4. Note that the 1/6 trend line deviates from the simulation result as ΔV_t grows significantly large and higher order terms in Eq. (11) get significant. However, even in such cases, the error by assuming the same fixed exponent produces a worst case error less than 15%. Similar analysis and results can be applied to all other standard cells (e.g., inverter, NAND) to obtain a temporal cell leakage model. Comparison between the results obtained from our model and from HSPICE simulation showed negligible error (i.e., MAX 8% error) for all standard cells.

Additional analysis has been done to consider degradation in subthreshold slope due to NBTI. Using the simple formulation introduced in [16], reduction in subthreshold slope can be represented in a time dependent form as follows,

$$S(t) = 2.3kT\left(1 + \frac{C_{dm} + C_{IT}}{C_{OX}}\right)$$
$$\Delta S(t) = 2.3kT\left(\frac{\Delta C_{IT}(t)}{C_{OX}}\right) = 2.3kTq\left(\frac{\Delta N_{IT}(t)}{C_{OX}}\right) \propto t^{1/6} \tag{12}$$

where C_{dm} and C_{IT} represent maximum depletion capacitance and interfacial trap capacitance, respectively. It was shown by Eq. (5) that interfacial trap density N_{IT} has power dependency to time, and as a result, increase in subthreshold current also reveals the same power dependency to time. However, in our specific example (i.e., BPTM 70nm node), due to a large difference between C_{IT} and C_{OX}, only a negligible change in subthreshold slope has been observed in reality (i.e., less than 1% in 10^{10} seconds). Hence, in our work, without loosing accuracy, we applied a constant subthreshold slope value for entire time range of analysis. However, note that our proposed model can easily incorporate the impact of subthreshold slope degradation due to NBTI in general.

TABLE 3. SIMULATION RESULTS FOR ISCAS'85 BENCHMARK CIRCUITS. R_{LEAK} AND R_{FREQ} ARE THE PERCENTAGE DEGRADATION IN F_{MAX} AND I_{DDQ}, RESPECTIVELY. CORRELATION BETWEEN F_{MAX} AND I_{DDQ} IS MEASURED BY CONSTANT K FACTOR FOR TWO SAMPLE TEMPERARUES 75°C AND 125°C.

Circuits	No. of Gate	f_{MAX} (GHz)		R_{freq}	IDDQ (uA) @75°C		R_{leak}	K_{75}	IDDQ (uA) @125°C		R_{leak}	K_{125}
		t=0	*t=10^8		t=0	*t=10^8			t=0	*t=10^8		
c74181	95	3.70	3.39	8.2	7.58	5.37	29.2	3.6	25.81	16.94	34.4	4.2
c432	178	1.74	1.61	7.5	14.29	10.57	26.1	3.5	48.69	33.71	30.8	4.1
c1908	452	1.35	1.24	8.3	34.07	25.87	24.1	2.9	116.13	83.02	28.5	3.4
c880	511	1.90	1.78	6.4	34.23	25.04	26.8	4.2	116.64	79.76	31.6	5.0
c499	516	1.95	1.79	8.1	38.38	28.88	24.8	3.1	130.84	92.61	29.2	3.6
c1355	594	1.74	1.60	7.7	41.35	30.29	26.7	3.5	123.73	83.24	32.7	4.3
c2670	841	1.62	1.49	7.8	51.86	37.63	27.4	3.5	176.90	120.00	32.2	4.1
c3540	932	1.21	1.11	8.0	86.98	65.07	25.2	3.2	296.35	207.70	29.9	3.8
c5315	1900	1.20	1.11	7.7	130.55	95.22	27.1	3.5	444.90	303.06	31.9	4.1
c6288	2421	0.42	0.38	7.8	167.24	122.82	26.6	3.4	567.83	387.36	31.8	4.0
Average				**7.8**			**26.4**	**3.4**			**31.3**	**4.1**

(*10^8 seconds = 3 years)

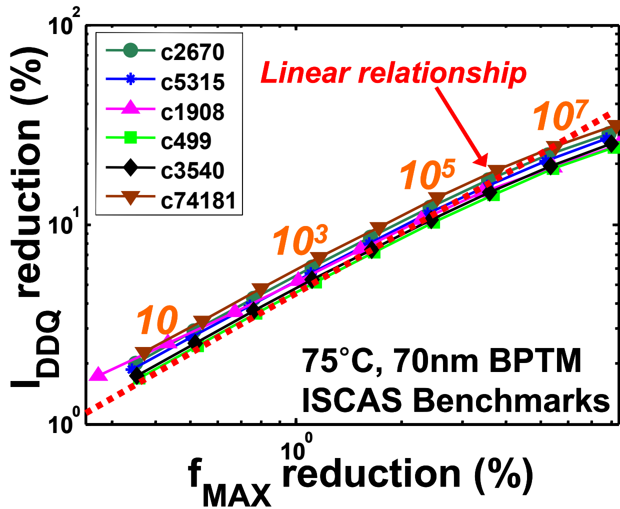

FIGURE 6. LINEAR RELATIONSHIP BETWEEN THE PERCENTAGE DEGRADATION IN F_{MAX} AND I_{DDQ} FOR 3 YEARS OPERATION TIME FOR 6 ISCAS BENCHMARK CIRCUITS.

Gate level characterization can be extended to compute the total circuit leakage (I_{DDQ}). Absolute I_{DDQ} values are usually highly dependent on the input vectors at which the measurement is made [5]. However, as observed from Fig. 4, the % reduction in cell leakage showed similar trend for different input vectors. The same trend was again observed for the circuit-level I_{DDQ} measure as shown in Fig. 5. For this particular example, all 36 inputs of ISCAS c432 benchmark circuit were degraded through a random AC pulse with a 50% signal probability. At each time frame, the input signals are propagated through the circuit to compute signal probability at the nodes inside the circuit. Then, depending on signal probabilities, V_t degradation for all the PMOS transistors are calibrated using Eq. (6). Finally, circuit I_{DDQ} is calculated for a fixed random input vector using the gate level leakage model discussed above. We chose 5 random test input vectors for Fig. 5. For all five test vectors, temporal leakage reduction closely matched the 1/6 trend. Furthermore, we have simulated the percentage reduction in I_{DDQ} for 10000 random input vectors shown as a histogram plot in the subfigure of Fig. 5 and observed that regardless of input vectors, percentage reduction always followed a similar trend (7% difference between MIN and MAX measure). Moreover, the 1/6 trend degradations revealed temperature independence as can be observed from Fig. 6. For a single random test pattern, NBTI degradations were performed for 25°C, 75°C, and 125°C. The results showed that 1/6 trend prevails regardless of the operating temperatures.

The result from Fig. 5 leads to a meaningful conclusion. **By tracking leakage degradation it is possible to predict the lifetime NBTI degradation behavior within a reasonable accuracy**. In addition, the I_{DDQ} reduction curves can be also used to capture an estimate of NBTI time exponent. Similar approach has been made to characterize the NBTI time exponent through the f_{MAX} testing [9]. However, I_{DDQ} measurement will provide an elegant and simple test configurations and reduce test costs compared to the f_{MAX} test. In the following section, we will further discuss how f_{MAX} and I_{DDQ} degradations are correlated.

NBTI CHARACTERIZATION USING TEMPORAL F_{MAX}-I_{DDQ} CORRELATION

In this section, using the proposed temporal f_{MAX} and I_{DDQ} model from the previous section, we first establish a general relationship between f_{MAX} and I_{DDQ} throughout the device lifetime. Using this relationship, in the later part of the section, we propose and efficient NBTI testing procedure using conventional I_{DDQ} testing method.

Temporal f_{MAX}-I_{DDQ} correlation

Analytical models established in the previous section showed that the percentage reduction in both I_{DDQ} and f_{MAX} have a power dependency with respect to the time with a fixed exponent of 1/6. As a result, I_{DDQ} and f_{MAX}'s are linearly correlated as follows,

$$R_{leak} = \frac{\Delta I_{leak}(t)}{I_{leak}(0)} \propto t^{1/6} \propto \frac{\Delta f_{MAX}(t)}{f_{MAX}(0)} = R_{freq}$$
$$R_{freq} = K \times R_{leak} \quad (K\ \text{:constant}) \tag{13}$$

where R_{leak} and R_{freq} are the percentage degradations in f_{MAX} and I_{DDQ}, respectively. ***K*** is a constant scale factor. Eq. (13) presents the key observation of our work, that f_{MAX} reduction can be expressed as a function of I_{DDQ} reduction in a linear form. This relationship is further justified through our simulation results summarized in Table. 3. All the circuits were synthesized using the LEDA standard cell

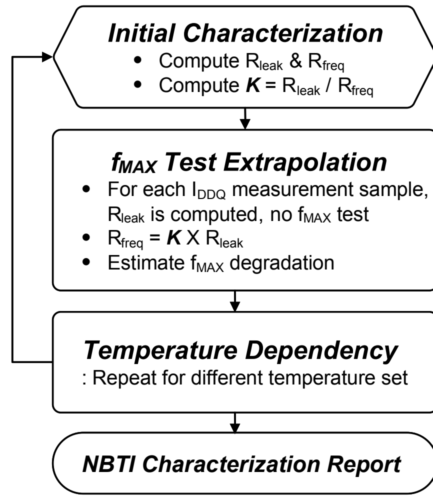

FIGURE 7. NBTI CHARACTERIZATION METHOD BASED ON THE TEMPORAL F_{MAX}-I_{DDQ} CORRELATION

library and properly scaled down for the BPTM 70nm [2] technology node. First, f_{MAX} and I_{DDQ} were estimated for initial design at $t=0$ (Column 3, 6 and 10). I_{DDQ} values are highly dependent on input vectors. However, as shown in section 2, the percentage reduction in I_{DDQ}, R_{leak}'s showed degradation regardless of input vector. Hence, for this analysis, I_{DDQ}'s were computed as an average value from 10000 random input vector samples. Next, for each benchmark circuit, a random AC signal with signal probability of 50% is applied for 3 years ($t=10^8$) time period to each primary input. Finally, using our proposed models, degraded f_{MAX} and I_{DDQ} values are computed (Column 4, 7, and 11). I_{DDQ} results were obtained for two temperature sample at 75°C and 125°C. Scale factors K_{75} (Column 9) and K_{125} (Column 13) were computed as a ratio between R_{freq} and R_{leak}, and can be interpreted as a measure of linearity between R_{freq} and R_{leak} for different circuits. It can be observed that for both temperature samples, the scale factor maintains a near constant for different designs, justifying Eq. (13).

Same trend can be observed through a timed R_{leak} versus R_{freq} plot shown in Fig. 6 for selected benchmarks circuits. Each data point in the plot represents the sampling time from 10^0 to 10^8 (3 years) seconds. Once again, it can be observed that throughout the lifetime, R_{leak} and R_{freq} retains a linear relationship, and the constant factor ***K***'s are nearly same throughout design.

NBTI characterization using on-chip I_{DDQ} testing

The correlation between f_{MAX} and I_{DDQ} can be used to build an efficient NBTI characterization methodology based on I_{DDQ} measurement. Fig. 8 represents the basic flow chart of our proposed method. The method first starts by applying an initial characterization to compute R_{leak} and R_{freq} under fixed temperature NBTI stress. Then using Eq. (13), ***K*** for current temperature is calculated. Using ***K*** constant, R_{freq} under long-term stress is extrapolated from R_{leak}, obtained from I_{DDQ} test. Note that, one can now avoid f_{MAX} test by alternative I_{DDQ} test. Finally, the method iterates through different temperature sets to generate a full NBTI characterization table.

As mentioned, the key contribution of our proposed method is that **by using a simple linear relationship, one can easily estimate NBTI related f_{MAX} degradations by means of I_{DDQ} testing**.

Discrimination of NBTI induced I_{DDQ} signature from other reliability degradation sources

So far, our proposed NBTI characterization method based on the I_{DDQ} measurement has assumed that the NBTI is the major source of reliability degradation in operating ICs. However, in real field, there are number of other sources which degrade the device reliability such as HCI and TDDB. For example, due to TDDB degradation, I_{DDQ} measurement can actually increase with time [10]. Under such assumption, overall I_{DDQ} degradation at time t, $I_{DDQ}(t)$, considering other reliability factors can be expressed as follows,

$$\begin{aligned} I_{DDQ}(t) &= I_{DDQ}(0) + \Delta I_{DDQ}(NBTI) + \Delta I_{DDQ}(TDDB) \\ &\quad + \Delta I_{DDQ}(HCI) + \ldots \\ &= I_{DDQ}(0) + C_{NBTI} t^{1/6} + f_{TDDB}(t) + g_{HCI}(t) + \ldots \end{aligned} \tag{14}$$

where Δ $I_{DDQ}()$ represents temporal change in I_{DDQ} due to different reliability sources. $I_{DDQ}(0)$ is the I_{DDQ} measured at initial test (t=0), and can be used to sort out initial defects and faults (i.e., conventional I_{DDQ} testing). On the other hand, each Δ I_{DDQ} components has a different temporal dependence (i.e. NBTI: n~1/6, HCI: n~1/2-2/3 [20], TDDB: n~ b, the Weibull slope [21]), voltage acceleration and temperature activation. Therefore, based on measurements at several voltages and temperatures, these I_{DDQ} components can easily be isolated. Note that this issue of isolation is not unique to I_{DDQ} measurements, rather f_{MAX} degradation will also require similar measurement to establish the origin of the degradation under multiple degradation mechanism. Moreover, the degradation components are often separated in time (e.g. earlier phase of stress, NBTI degradation tends to dominate, and other sources, for example measurable TDDB induced leakage current arises after certain amount of time) which allows further simplification of the deconvolution process. Hence, our proposed characterization method can be still applied under multiple reliability degradation sources.

CONCLUSION

In this paper, an efficient NBTI characterization methodology based on temporal f_{MAX}-I_{DDQ} correlation is proposed. An analytical I_{DDQ} model for CMOS circuit under NBTI degradation is derived. Simulation results showed that I_{DDQ} degradations in CMOS circuit under NBTI reflects the time dependent characterization of V_t degradation in a single PMOS transistor. Furthermore, we have examined that under NBTI stress, percentage degradations in f_{MAX} and I_{DDQ} are linearly correlated throughout device lifetime. Using this relationship, we proposed an efficient NBTI characterization method. The proposed method avoids complicated f_{MAX} testing and estimates an effective f_{MAX} degradation based on the I_{DDQ} test by using temporal f_{MAX}-I_{DDQ} correlation.

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