

Characterization and Estimation of Circuit Reliability Degradation under NBTI using On-Line I_{DDQ} Measurement*

Kunhyuk Kang, Keejong Kim, Ahmad E. Islam, Muhammad A. Alam, and Kaushik Roy
 School of Electrical and Computer Engineering, Purdue University, West Lafayette, IN, USA
 {kang18, keejong, aeislam, alam, kaushik}@ecn.purdue.edu

ABSTRACT

Negative bias temperature instability (NBTI) in MOSFETs is one of the major reliability challenges in nano-scale technology. This paper presents an efficient technique to characterize and estimate the lifetime circuit reliability under NBTI degradation. Unlike conventional approaches, where a representative f_{MAX} (maximum operating frequency) measurement from timing critical circuitry is used, we propose to utilize the standby circuit leakage I_{DDQ} as a metric to detect and characterize temporal NBTI degradation in digital circuits. Compared to the f_{MAX} based approach, the proposed I_{DDQ} based technique benefits from lower test cost and improved capability of estimating reliability of complex circuitries such as ALUs and SRAM arrays. We have derived an analytical expression for circuit I_{DDQ} from the analytical PMOS V_t degradation model ($\Delta V_t \propto t^{1/6}$). The proposed model is verified with measurement data obtained from a test chip fabricated in 130nm technology. Furthermore, we examine the possible applications of our proposed I_{DDQ} based NBTI characterization. We show that the temporal degradation in static noise margin (SNM) of SRAM array and f_{MAX} of random logic circuits are highly correlated to the I_{DDQ} measurement, and this relationship can be used to predict long term circuit reliability.

Categories and Subject Descriptors

B.8.1 [Performance and Reliability]: Reliability, Testing, and Fault-Tolerance; B.8.2 [Performance and Reliability]: Performance Analysis and Design Aids

General Terms

Reliability

Keywords

Reliability Characterization, NBTI, I_{DDQ}

1. INTRODUCTION

International Technology Roadmap for Semiconductor (ITRS) suggests the failure in time (FIT) of sub-100nm technology nodes to be in the order of 10-100 (failures in 10^9 hours). One of the major technology challenges in achieving

such requirement stems from the increasing temporal reliability concerns in MOSFETs due to negative bias temperature instability (NBTI) [1, 2, 3]. NBTI is a result of continuous trap generation in $Si-SiO_2$ interface of PMOS transistors. In bulk MOSFETs, undesirable Si dangling bonds exist due to structural mismatch at the $Si-SiO_2$ interface. These dangling bonds act as charged interfacial traps. Conventionally, hydrogen passivation is applied to the Si surface after the oxidation process to transform dangling Si atoms to $Si-H$ bonds. However, with time, these $Si-H$ bonds can easily break during operation (i.e., ON-state, negative gate bias for the PMOS). The broken bonds act as interfacial traps and increase the threshold voltage (V_t) of the device, thus affecting the performance of the IC. NBTI impact gets even worse in scaled technology due to higher operation temperature and the usage of ultra thin oxide (i.e., higher oxide field).

For the past few years, there has been a considerable effort to model and characterize the NBTI degradation at transistor level. The analytical models have been able to successfully interpret power-law degradation with fixed exponents [4, 6, 8] and such models have been extensively verified with experimental data proposed in the literature [23]. Due to successful development of device level NBTI model, researchers have been able to examine the impact of NBTI degradation at the IC level using analytical approaches. In [9], a static timing analysis (STA) tool considering the NBTI degradation was proposed. They have shown that the maximum circuit delay degradation due to NBTI closely follows the same power dependency to time as the V_t degradation. Circuit level NBTI models were further improved to consider various technology dependent parameters in [24]. Also, the effect of NBTI relaxation under AC operations has been analytically modeled in [25].

Though analytical approaches show efficiency in determining circuit reliability during the design phase, they still commonly possess fundamental limitations. Unlike single device level degradations, circuit level reliability degradations are complicated function of 1) bias point and signal activities at each and every circuit node, 2) on-chip temporal and spatial temperature gradient [5, 23], 3) electrical interference between nearby devices, and 4) statistical distribution of degradation process. Moreover, most of such parameters tend to affect NBTI mechanism in an exponential manner, which further increases complexity. Therefore, in order to obtain a more realistic insight of NBTI degradation at the circuit level, researchers have often used a post-silicon f_{MAX} measurement based characterization method. In [13], it was shown that the NBTI degradations have a direct impact on the critical speed path (f_{MAX}) of a circuit. By adjusting the Fluorine implants, the possibility of f_{MAX} testing on characterizing the lifetime NBTI behavior of CMOS devices was shown. Reddy & Krishnan et. al. [14, 16] further explored f_{MAX} degrada-

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tion under NBTI and proposed a parametric modeling scheme for efficient testing. Though f_{MAX} based characterization on a fabricated IC can resolve most of the issues with analytical approaches, f_{MAX} signature only captures the reliability degradation in the critical timing paths, neglecting the impact on most of the other parts of the circuit. Also, f_{MAX} test requires a complicated and expensive test/characterization setup. Hence, there is a growing need to develop an efficient method to characterize and project circuit reliability.

In this paper, we propose an efficient NBTI characterization technique based on the measurement of standby circuit leakage I_{DDQ} [19]. I_{DDQ} has been conventionally used as a method for detecting initial faults in ICs after fabrication. However, it has not been realized that I_{DDQ} can sense the time dependent degradation in an IC. Recently, a work by Mason et al. [18] has shown that I_{DDQ} can be used as a temporal signature of time dependent dielectric breakdown (TDDB). However, none of the previous works characterized circuit reliability under NBTI using I_{DDQ} measurement. Compared to the conventional f_{MAX} based characterization, our proposed I_{DDQ} based method benefits from the followings:

1. Provide an in depth reliability measure of a circuit considering each and every device in the design.
2. Test/characterization cost and complexity can be low.
3. The I_{DDQ} based characterization can be applied to a complicated circuitry such as ALU's and SRAM arrays.

Specifically, we first examine the possibility of I_{DDQ} based characterization by using an approximate temporal model of circuit I_{DDQ} considering NBTI. We will show and prove that the percentage degradation in circuit I_{DDQ} closely follows that of V_t degradation in a single PMOS transistor. Proposed I_{DDQ} model will be then verified with measurement data. A test chip was fabricated in a 130nm technology, where we have observed a good match with our proposed model. Finally, we will discuss the implication of our work in more advanced applications. An SRAM array and random logic circuit are chosen as examples to show that temporal I_{DDQ} measurement can be used to predict circuit lifetime for such applications.

The rest of the paper is organized as follows. In section 2, we explain the temporal V_t model used in our work. In section 3, using the temporal V_t model, we propose an analytical temporal I_{DDQ} model under NBTI. Our I_{DDQ} model is verified with measurement data. Section 4 shows that described models can be used to estimate reliability of logic circuits and memories. Finally, we conclude the paper in section 5.

2. PRELIMINARIES: TEMPORAL V_t MODEL UNDER NBTI

In this section, we will introduce the temporal NBTI model which will serve as the basis of our I_{DDQ} model. First, an analytical V_t model using a Reaction-Diffusion framework is reviewed. Second, the impact of AC type stress is analyzed. Then we will discuss the effect of finite delay during measurement and corresponding modification to the temporal V_t model.

2.1 Temporal V_t Model using Reaction Diffusion Framework

NBTI is the result of trap generation at Si/SiO_2 interface in negatively biased PMOS transistors at elevated temperatures. The interaction of inversion layer holes with hydrogen-passivated Si atoms can break the $Si-H$ bonds, creating interface traps and neutral H atoms. Neutral H atoms can

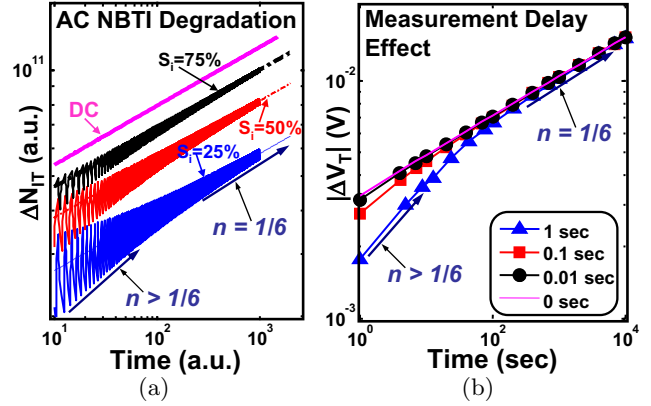


Figure 1: Simulation results for (a) NBTI degradation under AC stress, (b) effect of measurement delay in NBTI degradation.

form H_2 molecules, which can diffuse away from the interface (through the oxide) or can anneal an existing trap. General physical mechanism of H_2 based NBTI degradation is explained in reaction diffusion (RD) framework [2, 4, 6, 7, 8]. Using RD based model, interfacial trap density N_{IT} can be expressed as follows,

$$N_{IT}(t) \simeq C_0(D_{H_2}t)^{1/6} \propto t^{1/6}, \quad (1)$$

where C_0 is a technology dependent parameter and D_{H_2} is the diffusion coefficient of H_2 . We can observe that the trap generation has a power dependency to time with a fixed exponent of $1/6$.

2.2 AC degradation

In a real circuit operation, the effective ON-time of transistors are bounded by its input signal probability. In our work, we define the *Signal Probability* S_i at the input of gate i as a fraction of operating cycle which contributes to NBTI degradation, that is, logic LOW in CMOS since PMOS transistors mainly get affected by NBTI. During the OFF state, NBTI degradation is relaxed by the repassivation process of Si and H atom as follows [25],

$$N_{IT}(t + t_0) = N_{IT}(t_0) / \left(1 + \sqrt{\frac{\xi t}{t + t_0}}\right). \quad (2)$$

Fig. 1(a) plots the time dependent N_{IT} behavior for different signal probabilities. Degradation during the ON states and relaxation in the OFF states are computed using Eq. (1) and Eq. (2), respectively. We can immediately observe the difference between AC and DC degradation in two respects. First, during the early phase, time exponent is lower than $1/6$ as shown in Fig. 1(a). Second, with time, degradation trend slowly converges to the $1/6$ exponent. Both effects are mainly due to the asymmetric nature of the degradation and the relaxation process.

In reality, since the long term behavior of NBTI degradation is of more concern, a simplification is made to properly scale down the original DC curve for different signal probability. Specifically, depending on S_i , bond-breaking rate k_F is being scaled down by the AC degradation factor α_S . α_S values for various S_i 's are computed using the RD framework [7] (i.e., Eqs. (1) and (2)). Similar approach has been proposed by Kumar et al. in [25]. Considering this, long term trap generation N_{IT} can be now transformed into an increase in V_t as follows,

$$\Delta V_t(t) = (m + 1) \frac{qN_{IT}(t)}{C_{OX}} = K_C \times \alpha_S (Si)^{2/3} \times t^{1/6}, \quad (3)$$

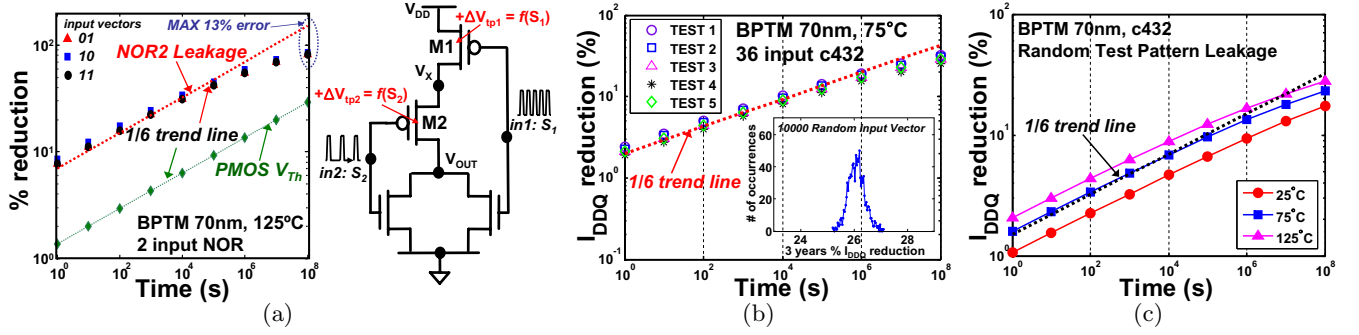


Figure 2: Simulation results for (a) temporal leakage degradation in 2 input NOR gate for different input vectors, (b) I_{DDQ} degradation over 3 years in ISCAS c432 benchmark for 5 different test input vectors, (c) I_{DDQ} degradation over 3 years in ISCAS c432 benchmark for 3 different temperature.

where m is a mobility degradation factor and K_C is a constant factor from Eq. (1). The unified NBTI model has been verified with experimental data [15, 23] and showed a close match.

2.3 Measurement Delay Effect

It was shown in the previous section that due to the impact of relaxation, NBTI degradation trend can change. In reality, this impact is most evident during the real measurement of NBTI [22]. Specifically, due to a finite amount of delay between the stress (e.g., accelerated condition with higher V_{DD} and temperature) and measurement phase, time exponent of NBTI degradations can be significantly larger than 1/6, especially during the early phase [23, 22] of degradation. Fig. 1(b) depicts the simulated plot of NBTI degradation considering the measurement delay. Finite amount of measurement delays (0, 0.01, 0.1, and 1 sec) were applied to each data point. As can be observed, measurement delay can have a significant impact on the degradation trend, especially during the early phase. However, the effect gets relaxed with time, and after certain period, degradation trends converge to a time exponent of 1/6.

3. I_{DDQ} BASED NBTI CHARACTERIZATION

I_{DDQ} of a circuit is defined as the total standby leakage current at a fixed DC input set. As PMOS V_t increases with time due to NBTI, leakage current through those PMOS transistors decrease exponentially, and as a result, I_{DDQ} of a circuit also reduces with time. We will show throughout the discussion in this section that I_{DDQ} of a circuit follows a particular temporal trend. Further, using this trend, we propose a method to characterize NBTI degradation and estimate circuit reliability degradation.

First, the temporal trend of I_{DDQ} will be studied through a simple analytical model. The model itself is rudimentary in some sense, but will provide us with a guideline to setup our characterization method. Then, our proposed model will be verified with measurement data from a fabricated chip.

3.1 Temporal I_{DDQ} model

Actual I_{DDQ} of a circuit depends on its specific topology. In order to setup up a simple expression of circuit I_{DDQ} under NBTI, we have characterized the temporal leakage values for a set of standard cell library designed in BPTM 70nm node [33]. In our work, we only considered the subthreshold leakage current as the major contributor to overall I_{DDQ} . This assumption is based on the fact that unlike other leakage components (e.g., gate, junction leakages), subthreshold leakages is most susceptible to V_t changes [11]. Fig. 2(a) shows an example for a 2 input NOR gate. Depending on the sig-

nal probabilities (S_1 and S_2) of the injected input signals $in1$ and $in2$, degradation in PMOS V_t 's (ΔV_{tp1} and ΔV_{tp2}) can be computed using Eq. (3) for any given operation time.

On computing each ΔV_{tp} , degradation in cell leakage can be calculated under the framework proposed in [20]. First, nominal leakage (i.e., at time 0) values for different input vectors (e.g., 00, 01, 10 and 11 for 2 input gates) are characterized using HSPICE simulations. Then, the nominal leakage values are factored according to V_t degradations as follows,

$$\begin{aligned} I_{01}(t) &= I_{01}(0) \times 10^{-\Delta V_{tp2}/S} \\ I_{10}(t) &= I_{10}(0) \times 10^{(-\Delta V_{tp2}\lambda_D - \Delta V_{tp1})/S} \\ I_{11}(t) &= I_{11}(0) \times 10^{[-(\Delta V_{tp2} - \Delta V_{tp1})\lambda_D - \Delta V_{tp1}]/S}, \end{aligned} \quad (4)$$

where S and λ_D are subthreshold slope and DIBL factor, respectively. $I_{01}(t)$ and $I_{01}(0)$ represent cell leakage for input vector '01' ($in1:0$ and $in2:1$) at time 't' and '0' (nominal leakage), respectively. Similar notation applies for I_{10} and I_{11} . Note that I_{00} component does not suffer from NBTI for NOR type gates since no PMOS transistors are on the leakage path (i.e., Similarly, for 2 input NAND gates, I_{00} , I_{01} and I_{10} does not suffer from NBTI). For NAND type gates, the only time dependent component I_{11} can be computed as,

$$I_{11}(t) = \frac{I_{11}(0)}{2} \times \left(10^{-\Delta V_{tp1}} + 10^{-\Delta V_{tp2}} \right), \quad (5)$$

where ΔV_{tp1} and ΔV_{tp2} represent V_t degradation in two parallel transistors of pull-up network (PUN) side of 2 input NAND gate. Fig. 2(a) shows the % reduction in 2 input NOR leakage for 3 year time period for different input vector obtained from our model. For this example, each PMOS transistor is equally degraded by 50% signal probability using Eq. (3). The resulting leakage reduction clearly follows the same power law as the V_t degradation with a same exponent of 1/6. This behavior can be explained by the following analysis. Using an analytical expression of subthreshold leakage current [11], leakage reduction R_{leak} in a single PMOS transistor can be written as follows,

$$\begin{aligned} I_{leak}(t) &= \beta(m-1)v_T^2 e^{\frac{V_g - V_t(t)}{mv_T}} \left(1 - e^{-\frac{V_{ds}}{v_T}} \right) \\ R_{leak} &= \frac{\Delta I_{leak}(t)}{I_{leak}(0)} = 1 - e^{-\Delta V_t(t)/mv_T} \\ &= \frac{\Delta V_t(t)}{mv_T} - \frac{1}{2} \left(\frac{\Delta V_t(t)}{mv_T} \right)^2 + \dots, \end{aligned} \quad (6)$$

where m is the body-effect coefficient and v_T is the thermal voltage ($= kT/q$). When ΔV_t 's are much less than the denominator mv_T (i.e., approximately 40mV at 125°C), leakage reduction R_{leak} can be approximated by the first term which shows a linear dependency with respect to the ΔV_t . This is the reason why leakage reduction shows a power dependency

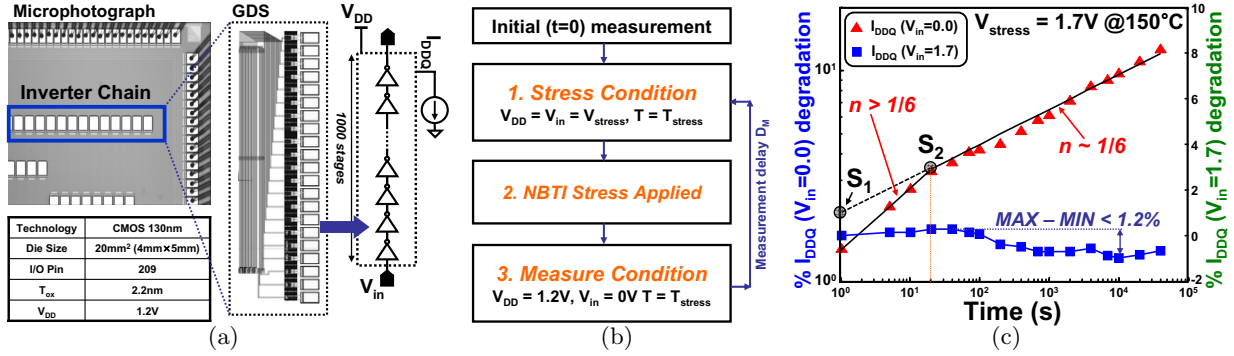


Figure 3: (a) Microphotograph of our fabricated chip, (b) stress and measurement sequence for NBTI experiment (c) I_{DDQ} degradation under NBTI. Degraded I_{DDQ} is measured during $V_{in} = 0$. When $V_{in} = V_{stress}$, I_{DDQ} values are nearly constant.

to operating time with a fixed exponent of $1/6$ as shown in Fig. 2(a). Note that $1/6$ trend line deviates from the simulation result as ΔV_t grows significantly large and higher order terms in Eq. 6 get significant. However, even in such cases, the error by assuming the same fixed exponent produces a worst case error less than 15%. Similar analysis and results can be applied to all other standard cells (e.g., inverter, NAND) to obtain a temporal cell leakage model. Comparison between the results obtained from our model and from HSPICE simulation showed negligible error (i.e., MAX 8% error) for all standard cells.

Additional analysis has been done to consider degradation in subthreshold slope due to NBTI [1]. Using a simple formulation introduced in [21], reduction in subthreshold slope can be represented in a time dependent form as follows,

$$S(t) = 2.3kT \left(1 + \frac{C_{dm} + C_{IT}}{C_{ox}} \right) \quad (7)$$

$$\Delta S(t) = 2.3kT \left(\frac{\Delta C_{IT}(t)}{C_{ox}} \right) = 2.3kTq \left(\frac{\Delta N_{IT}(t)}{C_{ox}} \right) \propto t^{1/6}$$

where C_{dm} and C_{IT} represent maximum depletion capacitance and interfacial trap capacitance, respectively. It was shown by Eq. (1) that interfacial trap density N_{IT} has power dependency to time, and as a result, increase in subthreshold also reveals the same power dependency to time. However, in our specific example (i.e., BPTM 70nm node), due to a large difference between C_{IT} and C_{ox} , only a negligible change in subthreshold slope has been observed (i.e., less than 1% in 10^{10} seconds). Hence, in our analysis, without any loss of accuracy, we applied a constant subthreshold slope value for entire time range of analysis. However, note that our proposed model can easily incorporate the impact of subthreshold slope degradation due to NBTI.

Gate level characterization can be extended to compute the total circuit leakage I_{DDQ} . Absolute I_{DDQ} values are usually highly dependent to the input vectors at which the measurement is made [28]. However, as observed from Fig. 2(a), the % reduction in cell leakage showed a similar trend for different input vectors. The same trend was again observed for the circuit-level I_{DDQ} measure as shown in Fig. 2(b). For this particular example, all 36 inputs of ISCAS c432 benchmark circuit were degraded through random AC pulse signals with 50% input signal probability. At each time frame, input signals are propagated through the circuit to compute signal probability at the nodes inside the circuit. Then, depending on signal probabilities, V_t degradation for all the PMOS transistors are calibrated using Eq. (3). Finally, circuit I_{DDQ} is calculated for a fixed random input vector using the gate level leakage model discussed above. We chose 5 random test input vectors for Fig. 2(b). For all 5 test vectors, temporal leakage

reduction closely matched the $1/6$ trend. Furthermore, we have simulated the % reduction in I_{DDQ} for 10000 random input vectors shown as a histogram plot in the subfigure of Fig. 2(b) and observed that regardless of input vectors, the % reduction always followed a similar trend (i.e., 7% difference between MIN and MAX measure). Moreover, the $1/6$ trend degradations revealed temperature independence as can be observed from Fig. 2(c). For a single random test pattern, NBTI degradations were estimated at $25^\circ C$, $75^\circ C$ and $125^\circ C$. The results showed that $1/6$ trend prevails regardless of the operating temperatures, as expected in [23].

The results from Fig. 2(b) lead us to a meaningful conclusion *by tracking a leakage degradation using an I_{DDQ} test, it is possible to predict the lifetime NBTI degradation within a reasonable accuracy*. In the next section, we will verify our model with measurement data from a fabricated chip.

3.2 Test chip measurement

Proposed I_{DDQ} model was verified with measurement data. A test chip was fabricated in a 130nm 1.2V 6-metal CMOS technology. Each PMOS transistor is designed with a T_{ox} of 2.2nm and V_t of -0.2V at nominal corner. Microphotograph of 20mm^2 test chip and its layout GDS view is shown in Fig. 3(a). A simple 1000 stage inverter chain was selected as a target circuitry. Stress condition for NBTI degradation was controlled by both the V_{DD} and temperature. Note that careful control of stress environment is important, since we intend to characterize only the NBTI induced reliability degradation.

Measurement and stress for each chip was performed in a test sequence shown in Fig. 3(b). After initial measurement, high temperature of T_{stress} ($^\circ C$) and high V_{DD} of V_{stress} (V) are applied as stress condition. V_{in} is set to V_{DD} . After certain stress period, V_{DD} is lowered to the nominal value of 1.2V for the I_{DDQ} measurement. Note that in the previous section, we have applied a random AC stress for the simulation. As a result, we were able to observe the I_{DDQ} degradation regardless of input vectors (i.e., Fig. 2(b) and Fig. 2(c)). In our inverter chain experiment, we can easily determine the worst case stress and measurement condition. We apply a full DC stress to the half number of inverters by setting V_{in} to V_{stress} during the stress, and effectively measure the degraded leakage in PMOS by flipping V_{in} to 0 during the measurement (i.e., PMOS transistors are degraded during input LOW, and degradation can be measured in terms of leakage during input HIGH.). After the I_{DDQ} measurement, cell state is flipped back to the stress condition by applying V_{stress} to V_{in} . Under our setup, delay between stress and measurement was 0.02s. 3(c) shows the measurement made from $T_{stress} = 150^\circ C$ and $V_{stress} = 1.7V$. As can be observed, after 200s, I_{DDQ} degradation closely follows a power function

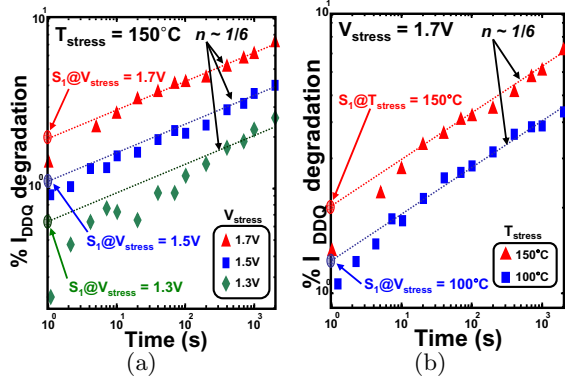


Figure 4: (a) V_{stress} (i.e., oxide field E_{ox}) dependency of NBTI, (b) temperature dependency of NBTI.

of time with an exponent of 1/6, which directly proves that the degradation is due to NBTI mechanism. Time exponent before time 200s shows a value close to 0.25, which is mainly due to the measurement delay [23]. Also note that the I_{DDQ} measured at $V_{in} = 1.7V$ shows a near constant value. As discussed above, the impact of I_{DDQ} degradation can be only observed through the inverted condition ($V_{in}=0$). As a result, if we maintain the $V_{in} = V_{stress}$ condition during the measurement, leakages in degraded inverters will not appear in the total I_{DDQ} .

Due to the regular nature of I_{DDQ} degradation shown in Fig. 3(c), we can easily extract the temporal I_{DDQ} in an empirical form. Two characterization points S_1 and S_2 are essential (Fig 3(c)). S_2 determines the time when the time exponent of I_{DDQ} degradation saturates to 1/6. S_1 is the projected 1/6 exponent line from S_2 to the initial point ($t=1$) of I_{DDQ} degradation. Using S_1 and S_2 , we can write the % degradation in I_{DDQ} as follows,

$$\begin{aligned} \Delta I_{DDQ}(t) &= \Delta I_{DDQ}(S_1)t^{1/6}, \\ \Delta I_{DDQ}(S_1) &= I_{DDQ}(S_2)/t(S_2)^{1/6}. \end{aligned} \quad (8)$$

We will discuss how this extracted model can be used to predict circuit reliability in the next section.

Fig. 4(a) shows the V_{DD} dependency measurement, where a fixed T_{stress} of $150^\circ C$ was used while changing V_{stress} from 1.3V to 1.7V. Fig. 4(b) shows the temperature dependency of NBTI, where a fixed V_{stress} of 1.7V was used while changing temperature from $100^\circ C$ to $150^\circ C$. I_{DDQ} degradation shows perfect correlation to temperature and voltage (i.e., oxide field E_{ox}) dependencies expected from NBTI degradation (section 2). Specifically, field acceleration factor γ of 1 dec/MV/cm [27] and activation energy E_A of 0.7eV (i.e., E_{IT} of 0.125eV) can be computed, which match with reported measurement data [6, 23]. Note that during the experiment, it is crucial to limit the voltage stress within a certain limit. For high electric field E_{ox} , there is a possibility of stress induced leakage current (SILC) [26] or even, in worst case TDDDB, which will overlap and contaminate the NBTI related I_{DDQ} measurement. However, using specific temperature and voltage dependency of each degradation mechanism, it is possible to isolate the effect of NBTI. Exact limit of V_{stress} is determined by the specific technology dependent parameters.

We have verified that our I_{DDQ} model indeed captures the effect of NBTI degradation as predicted in the previous section. In the following section, we show how our NBTI induced I_{DDQ} model can be used to estimate reliability of circuit.

4. NBTI RELIABILITY CHARACTERIZATION IN CIRCUIT

In the previous section, we have verified our proposed model with measurement data. Though the measurement was taken from a simple inverter chain, it clearly shows the effectiveness of our proposed approach. In this section, we will demonstrate our proposed method in more complex circuits. Two relevant examples will be discussed, that is, f_{MAX} degradation in logic circuit and static noise margin (SNM) degradation in SRAM array.

4.1 SRAM arrays: SNM Prediction over time

SNM is defined as the minimum DC noise voltage necessary to change state of an SRAM cell [29]. SNM can be computed as the side length of a maximum square nested between the two voltage transfer characteristics (VTC) (i.e., for each back-to-back inverters) of an SRAM cell. SNM is a critical performance parameter of an SRAM cell, which determines 1) the cell susceptibility to process variation [30, 31], 2) minimum HOLD V_{DD} , and 3) tolerance to on-chip noise sources. Particularly, designers are concerned with the SNM during the READ operations. READ SNM is computed when the two access NMOS transistors are turned ON through the word line. When the two PMOS transistor V_t 's degrade due to NBTI, trip point of each inverter reduces, which makes the cell more susceptible to a destructive READ event. Simulation was performed on SRAM cells designed in 70nm BPTM technology. For simplicity, two input storage nodes of the SRAM cell are assumed to be stressed with 50% signal probability. Using Eq. (3), we can calculate the V_t degradation in each PMOS transistor for 10^8 seconds (=3 years) to be 53mV at $125^\circ C$. Fig. 5(a) shows the result. After 3 years, read SNM degraded by more than 10% from its original value. Interestingly, the % degradation in SNM shows a $t^{1/6}$ trend. This trend can be analytically verified using the framework proposed in [32, 12], however, due to the limited space, detailed derivation and proof are not included in this paper.

By applying the fact that SNM and I_{DDQ} have similar power dependency to time with V_t degradation, we have,

$$\begin{aligned} R_{leak} &= \frac{\Delta I_{leak}(t)}{I_{leak}(0)} \propto t^{1/6} \propto \frac{\Delta SNM(t)}{SNM(0)} = R_{SNM} \\ \Rightarrow R_{SNM} &= K_{SNM} \times R_{leak} \quad (K_{SNM}: \text{constant}) \end{aligned} \quad (9)$$

where R_{leak} and R_{SNM} are the % degradations in total leakage and SNM, respectively. K_{SNM} is a technology dependent parameter which can be characterized in the design phase. The key result of Eq. (9) is that the degradation in SNM's can be characterized by means of leakage degradation, hence can predict the worst case behavior of SRAM cells over time. This approach has been verified through the simulation shown in Fig. 5(b), where in each time step, both the R_{leak} and R_{SNM} are plotted. We can observe that R_{leak} and R_{SNM} maintains a high correlation throughout the lifetime. Therefore, by using the early I_{DDQ} degradation behavior, one can approximate the lifetime degradation of SNM, and hence, the reliability of SRAM cells over time.

4.2 Logic: f_{MAX} Prediction over time

Similar analysis can be applied to the f_{MAX} prediction. It was shown in [9] that f_{MAX} degradation closely follows the 1/6 time exponent. Hence, the following analysis applies,

$$\begin{aligned} R_{leak} &= \frac{\Delta I_{leak}(t)}{I_{leak}(0)} \propto t^{1/6} \propto \frac{\Delta f_{MAX}(t)}{f_{MAX}(0)} = R_{f_{MAX}} \\ \Rightarrow R_{f_{MAX}} &= K_{f_{MAX}} \times R_{leak} \quad (K_{f_{MAX}}: \text{constant}) \end{aligned} \quad (10)$$

where $R_{f_{MAX}}$ is % degradation in f_{MAX} of a circuit. Similar to the SNM analysis, we can characterize and predict the lifetime f_{MAX} degradation by means of I_{DDQ} measurement.

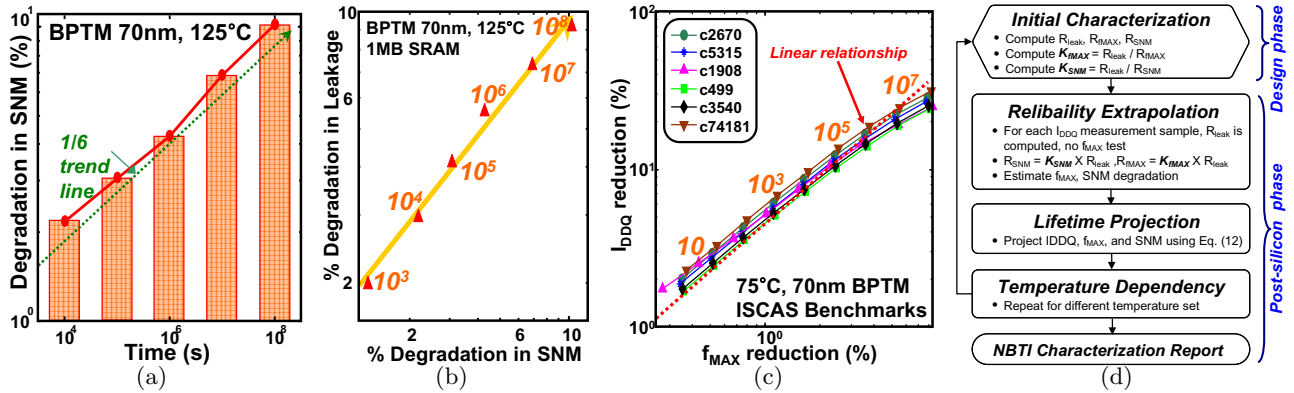


Figure 5: (a) SNM degradation under NBTI, (b) temporal correlation between SNM and I_{DDQ} , (c) temporal correlation between f_{MAX} and I_{DDQ} in several ISCAS'85 benchmark circuits, (d) I_{DDQ} based circuit reliability characterization flow.

Fig. 5(c) shows that f_{MAX} also maintains the high correlation with I_{DDQ} throughout the lifetime.

4.3 Circuit Reliability Characterization Flow

Fig. 5(d) represents the basic flow chart of our proposed method to characterize circuits for NBTI degradation over time. The method first starts by applying an initial characterization (in the design phase) to compute R_{leak} , R_{SNM} , and R_{fMAX} under fixed temperature NBTI stress. Corresponding K_{SNM} and K_{fMAX} are also calculated. Then, through early I_{DDQ} measurement, f_{MAX} and SNM's can be computed and verified using Eqs. (9) and (10). Long term degradation can be estimated using the projected I_{DDQ} model introduced in Eq. (8).

5. CONCLUSIONS

In this paper, we propose a technique to characterize and estimate circuit reliability under NBTI. Using an analytical approach, we have shown that the degradation in circuit I_{DDQ} can be used as a signature of NBTI degradation in a circuit. We have also verified our I_{DDQ} model with measurement data from an inverter chain fabricated in 130nm technology. Using our I_{DDQ} model, we proposed an efficient characterization technique to predict circuit lifetime under NBTI degradation. Specifically, we have selected static noise margin (SNM) of SRAM array and maximum operating frequency (f_{MAX}) of random logic circuit as examples to show how our models can be used to estimate NBTI degradation.

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