A CUSTOM IC FOR AUTOMATIC GAIN CONTROL IN LPC VOCODERS

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ABSTRACT

An automatic gain control technique for the audio input path of a vocoder has been developed based on a digitally controlled audio attenuator placed immediately before the a-d converter. The technique is more flexible than traditional analog approaches in that attenuation changes can be synchronized to vocoder frame boundaries thereby maintaining the integrity of the vocoder frame analysis. The digital controller for the attenuator has been implemented in a custom NMOS integrated circuit and was designed with the MACPITTS silicon compiler, a high level IC design tool. The circuit contains 2190 transistors occupying 4.5 by 5.4 mm.

INTRODUCTION

Due to the limited dynamic range and precision of fixed-point digital computers and analog-digital converters, narrowband speech compression devices operate most effectively over only a limited range of input speech volume levels. One solution to this problem is to increase the word length or use a floating-point format for the digital computation and a-d converter. In vocoder hardware implementations where size, power and cost are considerations, this may not be possible. A more practical approach consists of an audio attenuator which precedes the vocoder a-d converter and conditions the input audio signal so that the dynamic range of the a-d converter and fixed-point computations is not exceeded. Such an approach has historically been implemented in commercially available analog automatic gain control (AGC) devices. This paper describes a digitally controlled AGC technique which is considerably more flexible than traditional analog techniques.

The digitally controlled AGC is based on the Analog Devices AD7110 digitally controlled audio attenuator which is placed after the vocoder audio input pre-emphasis filter, and before the anti-aliasing filter and a-d converter (Fig. 1). The digital controller for the attenuator monitors the digital output from the a-d converter on a sample-by-sample basis and in concert with vocoder frame timing, outputs a digital attenuation value.

The controller is based on a "fast-attack/slow-decay" algorithm. The attenuation increases rapidly when the a-d converter is observed to be saturating. When the input level is too low the attenuation value is decreased gradually. Constraints are placed on the speed at which the attenuation is decreased so as not to respond to normally occurring intonations and pauses in speech. Finally, to maintain the integrity of the vocoder analysis, changes in the digital attenuation value occur only at frame boundaries.

A custom NMOS integrated circuit to implement the digital control of the AGC technique has been designed using the MACPITTS silicon compiler [1]. The MACPITTS compiler uses a high level algorithmic description as input to produce the mask descriptions required for integrated circuit fabrication. The quick design cycle achievable with the MACPITTS program is demonstrated by the fact that the AGC design was completed in approximately 3 weeks by a digital systems designer previously unfamiliar with the MACPITTS design tool. The AGC circuit is described in this paper as well as a fragment of the MACPITTS AGC source program as an example of digital circuit design using the silicon compiler.

AN LPC VOCODER WITH AGC

A very compact LPC vocoder [2] has been adapted to include the AGC technique outlined above. In this system (Fig. 1) the analog input speech is processed through the Analog Devices AD7110 digitally controlled audio attenuator. The AD7110 provides 88.5 db of attenuation in 1.5 db steps determined by a 6-bit binary input code. The analog speech is then converted to an 8-bit μ-255 law PCM code by the transmit half of the AMI S3507A CODEC-with-filters chip and transmitted serially to the digital analysis portion of the vocoder. The PCM code is also fed back to the custom AGC integrated circuit. The AGC IC uses this data as well as vocoder frame timing information to update the audio attenuator digital inputs. The LPC vocoder digital analysis (linear predictive analysis and pitch/voicing estimation) is implemented with two NEC μPD7720 Signal Processing Interface (SPI) single chip microcomputers. The LPC synthesis is realized with a third SPI device while an Intel 8085 minimum configuration 8-bit microprocessor is used for control and communication between the three SPI's and the outside world (host terminal).

THE AGC ALGORITHM

A "fast-attack/slow-decay" algorithm is implemented in the AGC integrated circuit. In this

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approach the attenuation value output from the AGC IC increases rapidly when the analog-digital coder is observed to be saturating. When the input level to the a-d coder is too low the attenuation value is decreased. Constraints are placed on the speed at which the attenuation is decreased so as not to respond to normally occurring intonations and pauses in speech. Finally, to maintain the integrity of the vocoder analysis, changes in the digital attenuation value occur only at vocoder speech frame boundaries.

The AGC algorithm tasks are partitioned into those performed once each sampling interval (typically 125 μs) and those performed once per speech frame (typically 22.5 ms). The sample rate tasks begin with the input of a μ-255 law PCM speech sample and updating a register which holds the maximum PCM value seen during the current frame. Another register maintains a count of the number of input samples which have saturated the a-d coder during the current frame.

The frame rate processing compares the maximum PCM value seen in the sample rate task over the past frame to several thresholds and decides whether to increase, decrease or maintain the current attenuation value. If the maximum input value saturated the a-d coder then we are in the "fast/attack" case and the attenuation is increased by 1.5 db (one binary code step). If several samples saturated the a-d coder during the past frame then more drastic measures are taken and the attenuation is increased by a total of 3 db. If the maximum value seen during the previous frame is more than 6 db below saturation then we are potentially in the "slow-decay" case. In order to not respond to normally occurring pauses or intonation in speech the frame rate processing keeps a count of consecutive frames in which the maximum value to the a-d coder was less then 6 db below saturation. The count is incremented once for each frame in such a case and when enough such consecutive cases (typically 25 frames or about one-half a second of speech) have occurred, the attenuation is decreased by 1.5 db and the decay counter is reset. Since consecutive low level frames are required, any frame whose maximum value was larger than 6 db below saturation will also reset this decay counter. When the maximum value seen in the past frame is more than 30 db below the a-d coder saturation value the frame is declared silence and no attenuation value adaptation is allowed. In addition, the decay count is not affected.

The AGC IC also has a "push-to-talk" input line for use in half-duplex vocoder systems. When asserted, this line has the same effect as silence frames in that no adaptation of the attenuation value is permitted. In all frames, the frame rate processing concludes by resetting the maximum value and saturation count registers used by the sample rate processing.

CUSTOM NMOS AGC IC

The AGC algorithm described above has been implemented in a custom 4 micron linewidth NMOS IC designed with the MACPITTS silicon compiler. The MACPITTS silicon compiler is an integrated circuit design tool which takes as input a high-level algorithmic description and produces mask level descriptions sufficient for IC fabrication as output. Since the MACPITTS user requires minimal knowledge of integrated circuit design and since the MACPITTS design language is highly readable, (e.g., a structured language similar to high level programming languages such as Lisp), IC designs such as the AGC circuit can be completed in a relatively short time by a potentially large community of users. For example, the AGC circuit was designed in approximately three weeks by a digital systems designer previously unfamiliar with MACPITTS.

The MACPITTS compiler uses a target architecture based on a combinatorial control section implemented as a Weinberger array [3] and a data path consisting of registers, combinatorial functional units and multiplexers for interconnect between the data path units. A floor plan of the AGC chip is shown in Fig. 2 depicting the control and data path regions. In the case of the AGC IC an 8-bit data path is specified including four registers, two subtracters, one incrementer, a 1's complement operator and four 1-bit flags. The remaining space in the data path consists of the multiplexers which output to the registers from the functional units. The chip uses 2190 N-channel MOS transistors occupying 4.5 by 5.4 mm and is being fabricated by the DARPA MOSIS silicon foundry facility.

The pin-out of the AGC IC as well as the peripheral circuitry necessary for use in the LPC vocoder audio input path are shown in Fig. 3. The μ-255 law PCM data is input on 8 input lines and the digital attenuation value is output on 6 lines. The remaining input lines include the power, ground, clock, reset, push-to-talk and frame and sample time strobes. In addition, twelve internal values are brought out for prototype test purposes. The peripheral circuitry includes an 8-bit serial-to-parallel converter and latch for the PCM data from the CODEC-with-filters chip, a TTL-to-CMOS level converter for input of the attenuation value to the audio attenuator, and a 3-phase clock generator.

The timing of data input/output and sample-rate ("sample-stuff") and frame-rate ("frame-stuff") processing is shown in Fig. 4. The sample-strobe rising edge initiates the sample-rate processing which, as described above, begins with input of the PCM sample. Similarly the frame-strobe initiates the frame-rate processing which concludes with the output of a new attenuation value if necessary. Since throughput was not a driving constraint in this design, the AGC IC was designed to do the sample-rate and frame-rate processing in a time-serial fashion. Arbitration between sample- and frame-strobes is achieved by storing the rising edge occurrences in separate flags and using a polling mechanism to service them. A benefit of this technique is that sample- and frame-strobes need be only loosely synchronized in time.

MACPITTS DESIGN LANGUAGE EXAMPLE

A section of the AGC source code is detailed (Fig. 5) to give an example of the nature of circuit

design using the MACPITTS compiler. The example used here is the sample-rate processing described above. A flow chart corresponding to this section is given in Fig. 6. Each line in the fragment is executed sequentially, one per AGC IC main clock cycle, and is numbered for explanatory purposes. In line 1 the 1's complement of "mucode" (the μ-255 PCM input) is compared to value of the internal register "maximum" which holds the largest magnitude input seen in the current frame. If mucode exceeds maximum, then maximum is updated. Lines 2-4 update the register "saturation-count" which counts the number of samples in the current frame which have saturated the a-d coder. If saturation-count is at its maximum value (127) then control returns to a loop ("interrupt-wait") which polls for sample- and frame-strobes (line 2). Next, in line 3, if mucode is greater than the a-d code saturation threshold, "SATURATION," then saturation-count is incremented. This concludes the sample-rate task and control returns to the interrupt-wait loop (line 4). The registers mucode and saturation-count were explicitly declared earlier in the program and account for two of the four registers detailed in the data path of Fig. 2. The comparisons and incrementers result in the implicit instantiation by the MACPITTS compiler of the subtracters and the incrementers in the data path. The entire AGC chip MACPITTS specification contains approximately 70 lines of code similar complexity to the example given here comprising a complete source description for the MACPITTS compiler.

CONCLUSION

An automatic gain control (AGC) scheme has been developed for the audio input path of an LPC vocoder. The technique is based on a digitally controlled audio attenuator immediately before the a-d coder. The attenuation is quickly increased when the a-d coder is observed to be saturating. The attenuation is decreased when the average speech input level is too low. The flexibility of the digital control structure is exploited by making attenuation changes only on speech frame boundaries. Unlike continuously adapting analog techniques, this approach minimizes distortion of the vocoder analysis.

The digital control for the AGC has been implemented in a custom NMOS integrated circuit using the MACPITTS silicon compiler. The MACPITTS compiler allows specification of the circuit at the algorithmic description level. This allows designers with minimal detailed knowledge of integrated circuit design to produce custom ICs in very short design cycles. The AGC IC consists of 2190 NMOS transistors occupying 4.5 by 5.4 mm. The circuit is being fabricated using the DARPA MOSIS silicon foundry facility.

REFERENCES

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[2] J. A. Feldman, E. M. Hofstetter, "A Compact, Flexible LPC Vocoder Based on a Commercial Signal Processing Microcomputer," Electro 82, Boston, MA, May 25-27, 1982, session 22/5.

[3] A. Weinberger, "Large Scale Integration of MOS Complex Logic: A Layout Method," IEEE JSSC, SC-2, pp. 182-190, December 1967.

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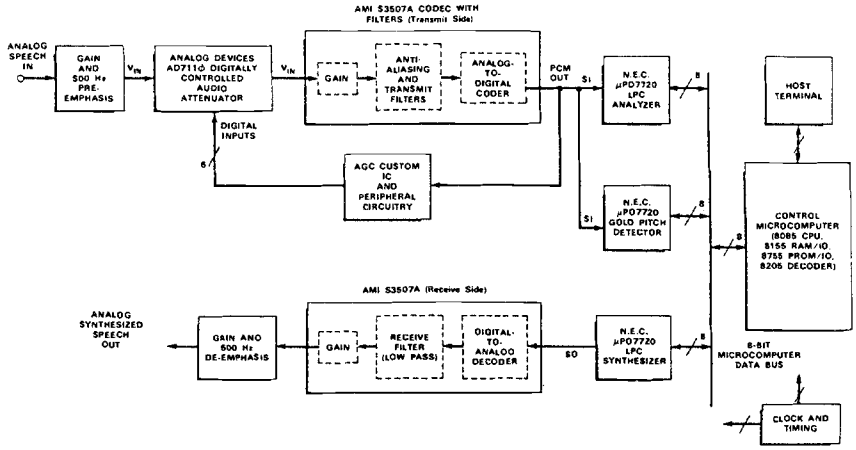

Fig. 1. LPC vocoder with automatic gain control.

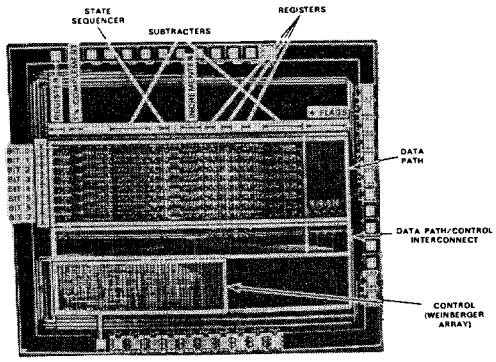

Fig. 2. AGC IC floor plan.

```
sample-stuff

1 (cond ((> (word-not mucode) maximum)
        (setq maximum (word-not mucode))))

2 (cond ((> saturation-count 126) (go interrupt-wait)))

3 (cond ((> word-not mucode) SATURATION)
        (setq saturation-count (+ saturation-count 1))))

4 (go interrupt-wait)
```

Fig. 5. Fragment of AGC MACPITTS source code.

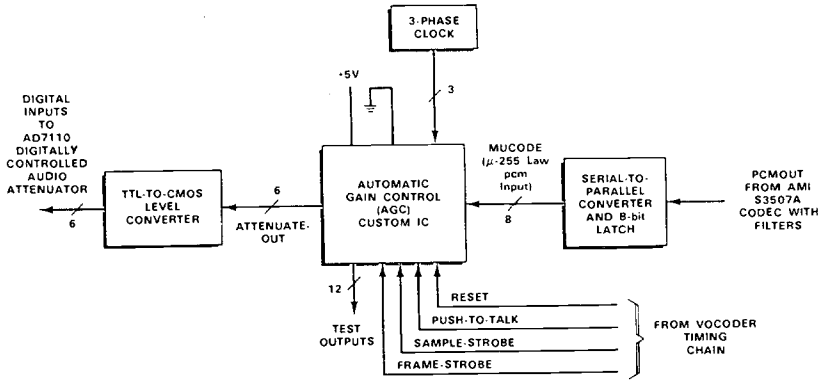

Fig. 3. AGC IC pin-out and peripheral circuitry for use in the LPC vocoder.

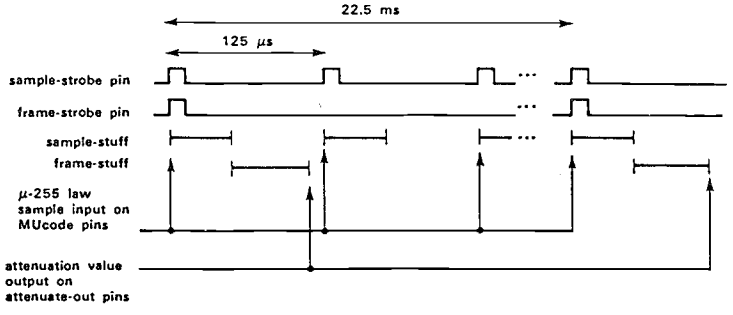

Fig. 4. AGC IC input/output sample-rate ("sample-stuff") and frame-rate ("frame-stuff") processing timing.

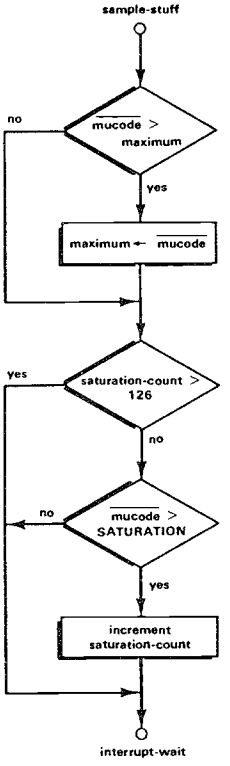

Fig. 6. Flow chart for sample-rate task of AGC algorithm.