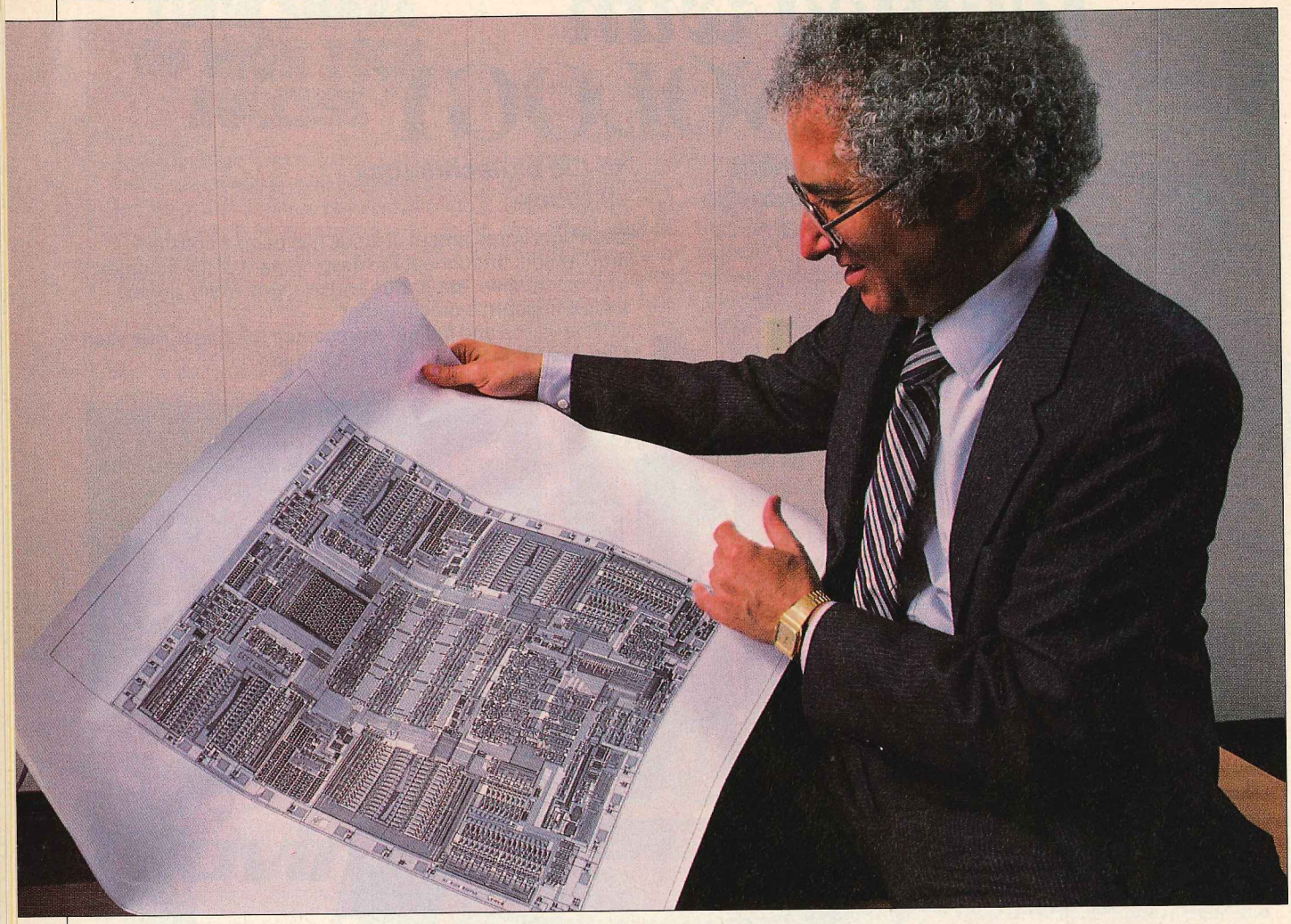

ANDREE ABECASSIS

CHIP DESIGN MADE EASY

A new generation of tools enables nonexperts to design custom integrated circuits cheaply and quickly

♦ by Jeffrey N. Bairstow ♦

Newly developed design automation systems are slashing the costs and reducing the time needed to design complex integrated circuits (ICs). The combination of powerful engineering workstations and novel software tools is making custom chip design economical even for engineers without training in the specialty. By enabling the rapid and routine design of special-purpose ICs, this fast-growing technology—called computer-aided engineering (CAE)—may eventually render standard-component ICs obsolete, thus revolutionizing the semiconductor industry.

Not much more than a decade ago, engineers designed large electronic systems with tens of thousands of discrete transistors mounted on cumbersome printed circuit boards. With the advent of integrated circuit technology that allowed dozens of transistors to be grouped on silicon chips, fewer printed circuit boards were needed, and systems could be housed in smaller enclosures. Today, complex systems can be designed with very-large-scale integrated (VLSI) circuits containing as many as

RICK FRIEDMAN

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half a million transistors on a single chip. But the conventional method of designing such circuits is extremely complex, requiring teams of highly skilled and experienced designers and, often, years of effort.

Until very recently, therefore, only the promise of enormous demand for a specific VLSI chip, such as a microprocessor, could be expected to produce a satisfactory return on investment. Hence system designers have had to build hardware from off-the-shelf ICs, because semiconductor manufacturers could not afford to build application-specific integrated circuits (ASICs) on a custom basis. At the same time, however, market pressures for increased functions and smaller packaging at lower costs have been causing the demand for ASICs to mushroom.

The availability of new automated-design technology, prompted in large part by the changing market dynamics, is altering the economics of designing and building ASICs. According to the market research firm Dataquest (San Jose, Cal.), the market for ASICs will be $14.9 billion, or roughly a third of the total IC market, by the end of the '80s—an astounding growth for a market that barely existed earlier in this decade.

Application-specific ICs produced by automated design tools are already beginning to appear in commercial products. For example, the new MicroVAX computer from Digital Equipment Corp. (Maynard, Mass.) is built on two printed circuit boards totaling only 158 square inches, or about a fifth the size of a comparable VAX computer designed the conventional way. Much of this size reduction is due to the MicroVAX's datapath VLSI chip, which is almost an entire 32-bit microprocessor. Using a prototype tool called a silicon compiler (see "Compilers: a high-level approach to IC design," p. 20), a three-person design team produced this 37,000-transistor IC in only seven months. By contrast, using conventional design methods for a full-custom VLSI chip, the MicroVAX chip would have taken more than seven person-years, or about four times as long. (A generally accepted rule of thumb is 5000 transistors per person-year.)

Solomon Design Automation president Jim Solomon (opposite page): "Automating chip design is the Manhattan Project of CAD—it's probably the only way we'll head off the Japanese threat to take over the integrated circuit business."

Mentor Graphics executive vice-president Gerry Langeler (above): "Our customers' appetite for integrated circuit design automation is insatiable. We've solved the easy problems; now we have to tackle the tough ones."

Not only do full-custom ICs normally require large design teams and many years of effort, but there simply aren't enough skilled IC designers available to devote to application-specific chips. By some estimates, there are only 2000–3000 experienced integrated circuit designers in the world, versus 300,000–400,000 system designers. According to industry estimates, though, perhaps 50% of those system designers could design their own ASICs, given the appropriate design tools.

Most ASICs in use today are not designed as full-custom chips. The most common style is the gate array, a device made up of several thousand primitive logic gates whose interconnections can be defined by the user. Because gate arrays are predefined, they are rarely efficient in their use of silicon. As gate arrays get larger, they become even less efficient, since more gates go unused and more of the silicon area is devoted to the metal interconnections between gates.

Nonetheless, industry experts estimate that in 1984 system engineers completed more than 2500 gate array designs. Moreover, since most aspects of gate array design can be automated, and since efficient tools already exist, that figure is expected to grow rapidly. The three major CAE workstation manufacturers—Daisy Systems (Mountain View, Cal.), Mentor Graphics (Beaverton, Ore.), and Valid Logic Systems (San Jose, Cal.)—all offer gate array design systems, as do several silicon foundries (companies that fabricate custom chips), such as VLSI Technology (San Jose, Cal.) and LSI Logic (Milpitas, Cal.).

For example, Daisy's Gatemaster is based on the company's well-established Logician series of workstations. The software handles schematic design entry, logic circuit simulation, signal-timing check, generation of circuit-testing routines, and physical layout of the silicon chip. According to Daisy, the system supports over 50 libraries of gate array designs from more than 25 silicon vendors. For gate array vendors, Daisy offers the MegaGatemaster, a powerful 32-bit workstation with significant simulation capabilities and an additional microprocessor to handle floating-point arithmetic.

A rapidly growing alternative technology for ASICs is the standard cell approach. Standard cells are predesigned functions such as logic gates, memories, programmed logic arrays, and even microprocessors. The cells are of fixed size and are available to users from a library of functions. A designer selects the logic elements called for in a design and places them, often using the standard cell vendor's own tools, to get the best use of the silicon area and the most logical and efficient interconnections. From the designer's layout, the semiconductor manufacturer combines the cells and produces the chip.

As with gate arrays, all the leading workstation makers offer standard cell tools and libraries. For example, the Mentor Graphics Cadicell software package automates the standard cell

Compilers: a high-level approach to IC design

The silicon compiler appears to hold out the greatest hope for significant automation of VLSI chips for system designers. It produces sets of instructions that can be used, in conjunction with other software tools, to produce masks for chip fabrication.

VLSI Technology, Inc., and Seattle Silicon Technology (SST) have developed relatively complex cell compilers that can be described as silicon compilers, but the first company to market a true silicon compiler is Silicon Compilers, Inc. (SCI). Its product offers the generation of system-level simulation models and the automatic interconnection of compiled modules.

SCI's method of silicon compilation leans heavily on the hierarchical IC design technology developed by Carver A. Mead, a professor at Caltech, and Lynn Conway, former manager of VLSI systems research at Xerox's Palo Alto Research Center. The first compiler—called Bristle Blocks, because it was designed to interconnect cells with predefined input/output patterns—was built by David L. Johannsen, one of Mead's graduate students.

Johannsen became a cofounder of SCI, along with Philip A. Kaufman, former general manager of Intel's microprocessor operations. The company's first product is the Genesil 400 System, which runs on a Digital Equipment Corp. VAX-11/750. A complete four-user system, including the VAX, has a price tag of $545,000, which may be a significant barrier to its adoption by large numbers of system designers. However, CAE observers expect that the Unix-based Genesil, or versions of it, will be available on stand-alone workstations and selling for less than $100,000 by the end of 1986.

Using Genesil is a three-stage process of design, verification, and tooling. For a typical circuit, the designer begins by making a first try at a block

GLEN R. STEINER

Silicon Compilers, Inc., is the first to market, with a highly regarded silicon compiler system running on a Digital Equipment Corp. VAX computer. Sensing a potentially large and lucrative market, other start-ups—such as Seattle Silicon Technology and MetaLogic—are rushing to compete.

layout process and the routing of interconnections. The package is available on Mentor's Apollo-based series of workstations. In addition, Mentor recently reached an agreement with NCR Microelectronics (Ft. Collins, Colo.) to market NCR's CMOS (complementary metal oxide semiconductor) cell libraries on Mentor's workstations.

Although standard cell is one of the more promising design technologies—it can be highly automated, provides a good compromise between design times and performance, and costs less than gate arrays—it is not yet in wide use. Standard cell design systems are not as well developed as gate array design systems, but they are expected to catch up shortly. Some industry insiders feel that within the next 18 months standard cell prototyping times will fall to as little as 8–10 weeks, or to the point where gate arrays are today.

The next level of sophistication beyond the standard cell approach is the cell compiler, or macrocell design method, which provides a significant improvement in cost and performance over both the gate array and the standard cell. A macrocell design is assembled from large, optimized circuits—such as counters, random-access memories, and multiplexers—which are then placed and interconnected manually by the designer using a layout editor on a workstation. (In some newer systems, this process is performed automatically.) The optimized circuit block may be generated automatically from libraries of cell compilers or designed interactively with conventional layout tools. The design method is hierarchical—larger blocks may be built from smaller ones—so very large designs can be handled (in contrast to gate arrays) and the designer need interconnect only a few large blocks.

This approach has been followed by VLSI Technology, Inc. (VTI), a silicon foundry that offers a comprehensive set of CAE tools both for purchase by customers and for use at VTI's design centers. The company's cell compiler makes use of "megacells," large func-

Engineering workstation makers, such as Daisy Systems, are expanding their lines, particularly at the low end, to meet the expected needs of system engineers for designing application-specific integrated circuits.

diagram, completing a series of menulike specification forms for the circuit elements of registers, multiplexers, buses, etc. These elements need not be designed from scratch—they are provided as a function set within Genesil. The system will flag errors in logic and timing as the specifications are entered, but the designer can also view a compiler-generated logic diagram to check the design himself.

When the designer is satisfied with the logic, the compiler generates three models: a functional description for simulating the design to make sure it will operate correctly, a timing model to check the design's performance for timing errors, and a layout model for placing circuit blocks and routing the connections. If the design performance is unsatisfactory, it's a relatively simple matter to revise the specifications or even use different functions. The models are then recompiled, and the design is simulated again.

Once the design is complete, the design engineer can generate the tooling tape for a particular silicon technology and a specific foundry for manufacturing the chip.

The current Genesil system is restricted to NMOS technology, but CMOS will be available shortly. Similarly, only a few foundries—notably American Microsystems, International Microelectronics Products, NCR Microelectronics, and VLSI Technology—have been certified by SCI.

While a silicon compiler radically shortens the time needed to design VLSI chips and particularly the time needed to consider alternative designs, the overall design and implementation of a chip can still be a relatively lengthy process. For example, the Digital Equiment Corp. MicroVAX datapath chip, designed with SCI's compiler, took a three-person team seven months to go from specification to silicon. The simulation and testing of the complex 37,000-transistor IC required considerable computer time, even on a computer as powerful as the VAX-11/750.

SST's cell compiler, called Concorde, offers much the same capabilities as Genesil but without the ability to automatically route the interconnections of modules. However, it is based on CMOS, a rapidly growing technology, and even has an analog cell option (unlike most of SST's competitors). Concorde has been integrated with Valid Logic Systems' SCALDstar workstation, a potentially powerful combination. And SST continues to add capabilities—for example, simulation—to its compiler, giving it more of the functions of a complete silicon compiler.

Yet SCI and SST will not have the silicon compilation field to themselves for long. Among the up-and-coming competition are at least a couple of custom foundries, notably LSI Logic and VLSI Technology. The latter has recently arranged to license a highly automated standard cell and gate array compiler from a British company, Lattice Logic.

A group of former Bell Laboratories researchers have started Silicon Design Laboratories (Basking Ridge, N.J.), which will shortly offer a silicon compiler for Unix-based workstations. According to vice-president Peter Rip, Silicon Design's compiler is based on a new language that supports both circuit attributes and computing. The compiler was developed for the Plex malleable computer project at Bell Laboratories.

A totally different tack is being taken by MetaLogic (Cambridge, Mass.) with the MetaSyn hardware synthesis language. MetaSyn, which grew out of the MacPitts IC design technology project at MIT's Lincoln Laboratory, allows the system designer to specify a design in terms of its behavior. It's claimed to be the only silicon compiler that can transform a behavioral description into a mask set for a full custom integrated circuit. MetaSyn is expected to be available within a few months.

How integrated circuits are designed

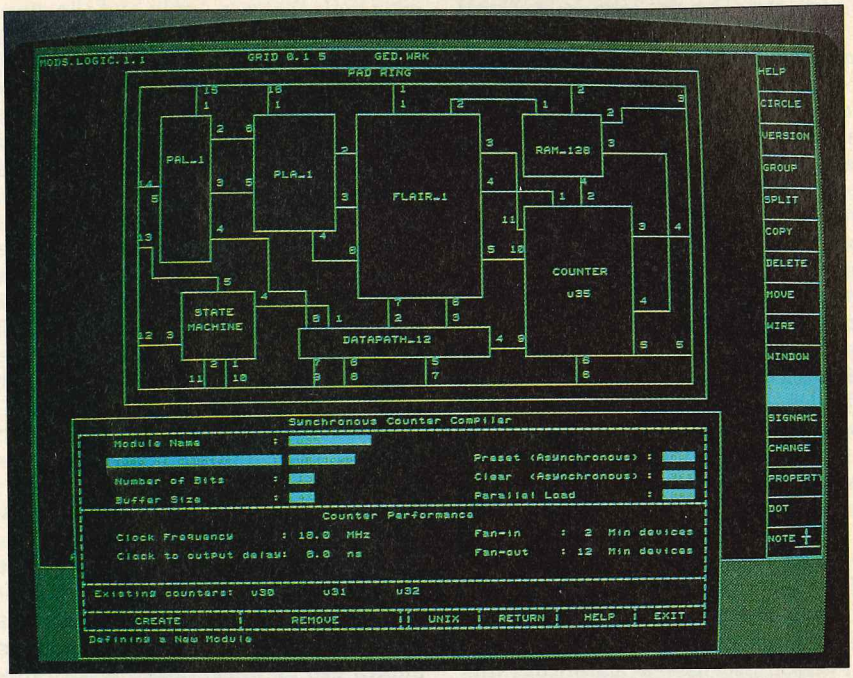
The design of an integrated circuit can be broken down into three major activities: the functional design of the circuit, the verification of the design, and the physical layout of the elements.

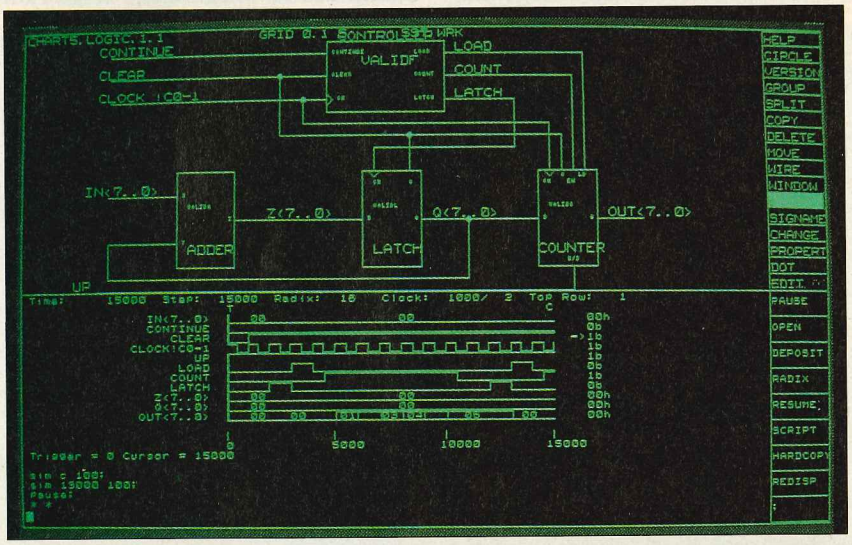
Seattle Silicon Technology's silicon compiler approach is based on this conventional design methodology. The process begins with the generation of a schematic diagram using a graphics editor (top photo), shown here on a Valid Logic SCALDstar workstation. The circuit elements are drawn and connected (upper half of screen) by the designer. Instead of selecting from a library of standard parts, the designer compiles modules for the specific application—in this case a synchronous counter—using an on-line menu (bottom half of screen). As decisions are made on the menus, the approximate performance of the module is immediately displayed on the screen (just below the specifications).

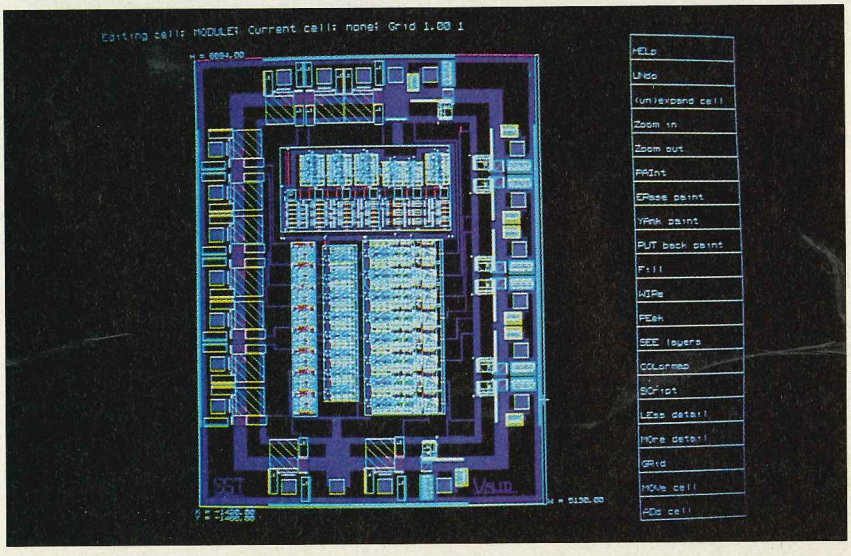
The next stage (middle photo) is the simulation of the design to verify that it is logically correct and has no timing problems. The display provides a window on the schematic (upper half of the screen) and the simulation waveforms in that part of the circuit (lower half of screen). The design will often be revised as the simulation results are analyzed; this may involve recompilation of several modules until the design performs satisfactorily.

When the user tells the compiler to construct a module, three representations are produced: symbols for schematic capture (diagram entry), a simulation model for design validation, and the actual module geometry for the final chip layout. When the engineer has verified the design, a layout is generated (bottom photo). At this point, depending on the type of circuit, the designer can finish the job either by laying out the modules manually and using a layout editor to make the interconnections or by employing the silicon compiler to do the placement and routing automatically.

Further simulation after layout is needed to verify that the design is ready for manufacturing. Current silicon compilers do not have this capability, so designers usually have to rely on simulation tools provided by the silicon foundry that will manufacture the circuit.







SEATTLE SILICON TECHNOLOGY

tional blocks that are designed for silicon area efficiency and that can be intermixed with user-compiled cells. VTI has generally been acknowledged as a leader in adopting CAE tools for ASIC design and in providing customer support, and other silicon foundries are now following its lead.

A cell compiler called Concorde is now available from Seattle Silicon Technology (Bellevue, Wash.), a company started by a group of designers from Boeing. The Concorde compiler has been adapted to Valid Logic Systems' SCALDstar VLSI design system for the creation of CMOS integrated circuits. Other cell compilers are expected to be available shortly from other companies—notably Lattice Logic (Edinburgh, Scotland), a spinoff from the IC design group at the University of Edinburgh, and Solomon Design Automation (Santa Clara, Cal.), a recent start-up headed by Jim Solomon, formerly manager of MOS analog R&D at National Semiconductor.

True silicon compilers, in which designers start with a high-level functional description of their system, are just beginning to appear as commercial products. The first is the Genesil System developed by Silicon Compilers, Inc. (SCI—San Jose, Cal.). SCI offers its own VAX-based design system, which supports four users, for a price of over $500,000. However, the company has recently received an infusion of capital from Daisy Systems, which is expected to offer a silicon compiler on its own single-user workstations for a price rumored to be around $200,000 and thus bring silicon compilation to a wider potential market.

SCI's silicon compiler requires that the user specify the chip's design structurally, as a set of components. This is a natural extension of a mode of design that is familiar to the conventional logic designer and the user of gate arrays and standard cells. An alternative design methodology is to specify the design in terms of its behavior, a potentially powerful technique. For example, MetaLogic (Cambridge, Mass.) is developing MetaSyn, a behavioral hardware-description language for design synthesis, simulation, and performance prediction. But although such a behavioral approach may eventually come closest to the way system designers will want to use computer-aided engineering for IC design—most of them do not now design or lay out chips, nor do they really want to—engineering-workstation makers are currently a long way from achieving this ideal.

MetaLogic is a spinoff from a small group of system designers at MIT's Lincoln Laboratories that developed the MacPitts silicon compiler on which the MetaSyn compiler is based. The principals—Frank Garofalo (president), Jeffrey Siskind (chief technical officer), and Jay Southard (director of technical marketing)—are all electrical engineers with strong programming backgrounds, not unlike their intended customers. Says Southard: "Our customers will be system designers with programming experience, which means anyone who has graduated or done significant design work in the last ten years."

Each of the "Big Three" workstation makers—Daisy, Mentor, and Valid—provides tools that are specific to its own products. But many believe that IC designers of the future will require a hierarchy of computing capabilities for complete design and layout. Robert Sumbs, executive vice-president of Valid Logic Systems, envisages a three-level set-up: personal computers (one per engineer) for entering schematic diagrams and for logic design; several powerful workstations for simulations, physical layout, and test generation; and a large mainframe computer that links all the units.

Such an arrangement seems inevitable, largely because of the spread of personal computers with increasing computational power and greater storage capabilities. In general, dedicated workstations can be used only for design activities, which are a relatively small part of the average design engineer's workload. A recent study by Hewlett-Packard estimated that design engineers typically spend only 30% of their time on design engineering (and only half of that time on actual design creation and modification) and the remainder on planning, management, and documentation—activities that can be greatly assisted by a personal computer. Thus the provision of inexpensive software for schematic capture (diagram entry), logic design, simulation, result analysis, and documentation could make better sense than the use of an expensive workstation.

Andrew Rappaport, president of the Technology Research Group (Boston), says that of the roughly 4500 single-user CAE workstations installed by the end of 1984, fewer than half were PC-based. By the end of this year, he says, that proportion should have grown substantially. Supermicro-based workstations from Valid and Mentor might be less expensive than their predecessors, but "when engineers buy PCs for design automation," says Rappaport, "they get a personal computer thrown in for free." Recognizing the trend toward personal computers, Daisy now offers an IBM PC-AT–based system, the Personal Logician, for around $25,000. While not exactly free, it performs at least as well as the original, and very successful, $75,000 supermicro-based Logician.

If the IBM PC is to be used for much more than schematic capture, high-resolution graphics and 32-bit processing are essential. Opus Systems, a Los Altos, Cal., start-up, will shortly introduce an IBM PC 32-bit processor board that will provide almost VAX-level computing power. Because such a processor will run a full System V UNIX operating system, the PC can be used with complex CAE progams.

Probably the best-selling PC-based design system is the Dash series offered by FutureNet (Canoga Park, Cal.) for the IBM PC, PC-XT, and PC-AT. The company claims to have sold over 2500 Dash systems. Not only does FutureNet cover schematic capture, but the com-

Plug-in special-purpose processors, such as this system developed by FutureNet, turn the IBM PC into an engineering workstation that can handle many aspects of integrated circuit design.

pany has recently begun to offer the Opus plug-in National Semiconductor 32032 coprocessor, which allows the PC to run the industry-standard CADAT logic and fault simulator produced by HHB Softron (Mahwah, N.J.). FutureNet offers the coprocessor with CADAT for approximately $25,000—about half the price of a supermicro workstation with similar capabilities.

Meanwhile, the workstation manufacturers are not standing idly by. Apollo has reduced its hardware prices to the point where Mentor Graphics can now offer an Apollo DN300–based schematic capture workstation that is comparable to Daisy's Personal Logician. The Logician-AT offers a simulation package, but Mentor counters with a diskless system that runs a remote simulator. And while higher-cost versions of the Personal Logician offer networking with Ethernet, the Apollo-based workstations use Apollo's own network, often reckoned the industry's best. Another plus: Apollo workstations can now run both the full Berkeley UNIX and AT&T's System V.

Workstation manufacturers are also extending the capabilities of their systems at the high-performance end. Valid Logic has attacked the problem of simulating complex VLSI devices in two ways—with a modeling system based on the use of actual devices and with a hardware-based simulation accelerator that runs hundreds of times faster than its software equivalent.

Almost any integrated circuit can be used as a model for this system—microprocessors, programmable logic arrays, floating-point processors, etc. The actual device is plugged into the Realchip system, and its inputs are stimulated to provide real outputs for the simulation. Thus the actual IC replaces a software model. Not only can Realchip be used with complex devices for which software models may be inadequate or unavailable, but it can also be used for simulating prototype devices or custom VLSI chips.

Not to be outdone, Mentor Graphics recently announced a similar method of incorporating actual devices into simulation models. The company claims that the new system, called the Hardware Modeling Library, can accommodate component clock speeds of up to 16 MHz, an important factor since current-

BUSINESS OUTLOOK

IC design tool market: changing as it grows

By simplifying integrated circuit design, the new methodologies of gate arrays, standard cells, and silicon compilation are expanding the number of professionals worldwide who can function, when the need arises, as IC designers. Consequently, the market for IC design tools, including software packages and workstations dedicated to running them, is also growing. The Technology Research Group (Boston) predicts that sales of automated tools for IC layout will rise from roughly $110 million in 1984 to $340 million in 1988, representing compound annual growth of 33%. And growth will continue to be strong into the 1990s.

But these figures don't tell the whole story; along with high growth comes fundamental change. Last year, nearly 80% of revenues from the IC design tool industry came from the sale of conventional geometric layout systems. These systems automate the drafting of chip layouts, but they require a one-to-one correspondence between what operators enter and see on the computer screens and what is ultimately etched into silicon. They are useful only to the few thousand engineers trained to design integrated circuits. By 1988, however, the Technology Research Group expects that conventional geometric layout systems will contribute only 15% of design tool industry revenues.

The real growth will be in design tools aimed at system designers—gate array and standard-cell placement and routing packages, silicon compilers, and symbolic layout editors. These systems automate the generation of geometric patterns and are therefore suited to system engineers not versed in the fine points of semiconductor physics and geometric chip layout. Sales of such advanced layout systems will grow 85% a year, from $25 million in 1984 to $290 million in 1988. Total installations will grow from 375 in 1984 to more than 6000 in 1988.

The biggest question now facing the design tool industry concerns who will sell these tools. Until recently, the industry was dominated by large computer-aided design (CAD) vendors—most notably General Electric's Calma subsidiary (Sunnyvale, Cal.), which was responsible for nearly two-thirds of all geometric layout systems in place in 1984. These older, minicomputer-based systems typically support three to four users and cost several hundred thousand dollars.

But as the emphasis in IC design tools shifts to automated layout software sold with new, microprocessor-based single-user workstations, old-line CAD vendors like Calma will face stiff competition. Daisy Systems (Mountain View, Cal.), Mentor Graphics (Beaverton, Ore.), and Valid Logic Systems (San Jose, Cal.)—the leading suppliers of computer-aided engineering systems—are enhancing their logic design systems with IC design tools. All three either offer or will shortly offer gate array and standard-cell layout systems and silicon compilers.

More important, these CAE vendors are now selling logic design workstations to the same system engineers who will seek layout systems as advanced IC design methodologies mature. Thus they have established an early toehold among the buyers who will ultimately contribute most to the expansion of the IC design market.

A raft of specialized start-ups is also addressing the market for advanced layout tools. Silicon Compilers, Inc. (San Jose, Cal.), and Seattle Silicon Technology were among the first in the silicon compilation market. Both companies are selling their software tools directly to end users but are hedging their bets through relationships with CAE vendors. Seattle Silicon sells its Concorde compiler through Valid Logic, while Silicon Compilers has sold a minority equity interest to Daisy Systems.

By year's end the market will be crowded with start-up vendors of silicon compilers and other advanced layout tools. Because system designers view IC design as only one small part of a much larger overall design task, the most successful vendors will likely be those that link up with mainstream CAE vendors or silicon foundries—suppliers of the custom chips themselves.

Indeed, next to users, silicon foundries have the greatest vested interest in IC design tools. As the design tool market grows to $340 million in 1988, the total market for semicustom chips will grow to $4 billion from $580 million in 1984. To CAE and CAD vendors, tools are an end product, but to foundries they are a means to a much larger market.

by Andrew S. Rappaport

ly available microprocessors have clock rates of 8 MHz or more.

The problem of simulation speeds is also addressed with Valid's Realfast simulation accelerator, an add-on unit with two processors that boost simulation speeds up to 500 times, according to Valid. One processor, termed an event engine, maintains simulation timing and schedules simulation events for evaluation. The other processor, the evaluation engine, resolves the logic states of the gates scheduled for changes by the event engine. With a simulation memory of up to 64 megabytes, Realfast can handle designs of up to 2.5 million gates, claims Thomas M. McWilliams, corporate vice-president of Valid.

Daisy's MegaLogician workstation also uses multiple processors to speed up the simulation process; Daisy offers a hardware simulator, called PMX (Physical Modeling Extension), that is comparable to Valid's Realchip. The savings in simulation time with these modeling workstations are dramatic. For example, the 1000-clock-cycle simulation of a 100,000-gate circuit might take 15 hours on a general-purpose mainframe computer. Such simulations are typically done overnight and the results analyzed later. But because the same simulation on a MegaLogician would, according to Daisy, take only three minutes, the design engineer could run simulations in a relatively interactive mode.

These advances, however, have not solved all the remaining problems in using CAE for VLSI design. The Technology Research Group's Rappaport still sees major problems in simulation, verification, and test, as well as in cooperation between workstation vendors and the silicon foundries that will be responsible for producing custom chips. "The principal factor separating winners from losers," he says, "will be how well vendors help system designers. Incomplete solutions to CAE support have nearly reached the end of their productive lives."

For example, Rappaport notes that simulation models on workstations often differ from those used by silicon foundries. Typically, the foundries use simulators developed for mainframe computers, such as HHB Softron's CADAT or GenRad's HILO, while vendors use their own proprietary simulators. Errors between the two types may be as simple as circuit timing, but this may be enough to cause inaccurate functional analyses. Chip designers are thus forced to run two sets of simulations—one on a workstation and another on the chip vendor's mainframe.

This is part of the general problem of standards that continues to bedevil CAE. System designers are unlikely to accept the technology unless they can be assured that the multiplicity of tools and databases can adequately communicate. CAE standards are "slow in coming and not widely adopted," says Bruce Gladstone, president of FutureNet. "We seem to have evolved into a spirit of noncooperation. And as long as everyone jealously guards their data, there is much less incentive for the customer to buy."

The only standard that is receiving much attention is the Electronic Design Interchange Format, which is adequate for transferring net lists and test patterns between systems. But CAE observers believe that it will not promote close integration between all CAE tools. For example, it does not remedy the lack of standards for simulation data.

In any case, the fast pace of development in CAE means that no viable standard would last very long; no workstation vendor would restrict system development merely to comply. However, the widespread adoption of PC-based workstations may produce some de facto standards, just as the IBM PC effectively made Microsoft's MS-DOS a standard operating system for personal computers.

From the design engineer's viewpoint, two key goals remain to be achieved before CAE can be widely accepted—integration of both software and hardware for the entire design and implementation process, and thorough training programs. Bob Graybill, an engineering fellow with the Westinghouse Defense and Electronics Center (Baltimore), echoes a familiar complaint: "There are too many workstation vendors and too many proprietary packages. For successful circuit design, we need the interactive capability of workstations but with access to shared databases and links to other users. Engineering is a team process."

The lack of adequate education and training is also a major stumbling block. A one- or two-week course is hardly enough to turn an engineer into a competent IC designer. All the workstation suppliers, some of the software tool developers, and several silicon foundries have thus been offering quite extensive training programs to fill the breach. Gerry Langeler, executive vice-president of Mentor Graphics, jokingly suggests that his firm is being transformed from a workstation company "with a small university attached" to "a large university with a small workstation company attached." Of course, if computer-aided engineering tools were genuinely easy to use, less support would be required and the tools would be accepted faster.

Langeler believes that as many as 30,000–50,000 engineers could be designing silicon chips by the end of 1986. While some might consider this an optimistic estimate from a vendor with a vested interest, the pressure for improvements in engineering productivity could in fact make the diffusion of CAE technology exceed even the wildest estimates. □

Jeffrey N. Bairstow is a senior editor of HIGH TECHNOLOGY.

For further information see **RESOURCES** *on page 74.*

Recognizing that the market for semicustom chips can expand only as fast as designers get effective tools, several foundries have aggressively pursued tool development. For example, VLSI Technology (San Jose, Cal.), a five-year-old vendor of custom chips, has pioneered work in cell compilation and symbolic chip assembly and sells design tools in addition to foundry services. Others, such as LSI Logic of Milpitas, Cal. (the leading CMOS gate array supplier), and Gould AMI Semiconductors of Santa Clara, Cal. (the most active U.S. custom chip foundry), fund large internal development groups to investigate and develop next-generation IC design tools. These tools not only help to ensure that foundries are well fed but also constitute a large part of the firms' competitive strategies.

And there's the rub for design tool vendors: When it comes to selling layout tools to system designers, foundries hold most of the cards. System designers used to purchasing only off-the-shelf components are concerned about their own ability to develop deliverable custom parts. Tool vendors can make bold claims about the quality and reliability of their software, but foundries are the ultimate sources of guarantees. Until system designers gain confidence in the layout process, they will prefer to purchase the tools recommended by foundries.

Andrew S. Rappaport is president of the Technology Research Group, a Boston-based market research and consulting company specializing in the computer-aided engineering and integrated circuit industries.

RESOURCES

Following are sources for further information about topics covered in the feature articles in this issue.

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