

Low Loss Multi-wafer Vertical Interconnects for Three Dimensional Integrated Circuits

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Abstract — A low loss multi-wafer vertical interconnect appropriate for a microstrip-based circuit architecture is proposed. This transition has been designed, fabricated and measured on 100 μm thick GaAs substrates. The measurements demonstrate insertion loss of better than 0.2dB and reflection of better than 13.6dB up to 20GHz. Using such a high performance transition allows for a more power efficient interconnect, while it enables denser packaging by stacking the substrates on top of each other, as today's technologies demand.

Index Terms- Vertical interconnects, Microstrip line, Integrated Circuit packaging.

I. INTRODUCTION

In today's technology, integrating a system is a major challenge in terms of having the most compact and efficient packaging. Microstrip lines are one of the best-suited architectures for Monolithic Microwave Integrated Circuits (MMICs), and hence are widely used due to their large bandwidth, high power handling, excellent miniaturization, and small volume. At the same time the microstrip architecture has been the most difficult one to utilize in multi-layer arrangements due to the extending ground planes and the parasitic inductances and capacitances associated with changes in the ground metallization.

High density circuit architectures require multi-layer transitions that can be used to tightly integrate circuit components on multiple wafers, integrated using wafer-to-wafer bonding methods. Developing a multi-layer circuit using a low-loss vertical interconnect architecture results in less dissipated power per unit area, and so increased power handling capability and reduced volume and cost. To design an optimal transition, not only the line impedances should be matched (to maximize the coupling and minimize the reflection), but also the fields on the two interconnecting lines should transition in a way that reduces unwanted junction parasitics. Even at frequencies as low as L-band, matching the impedances alone is not adequate and the fields along the transition have to maintain their continuity as well. In high density circuits high performance requires low loss combined with reduced parasitic radiation and proximity coupling between the various sections of the electromagnetic structure.

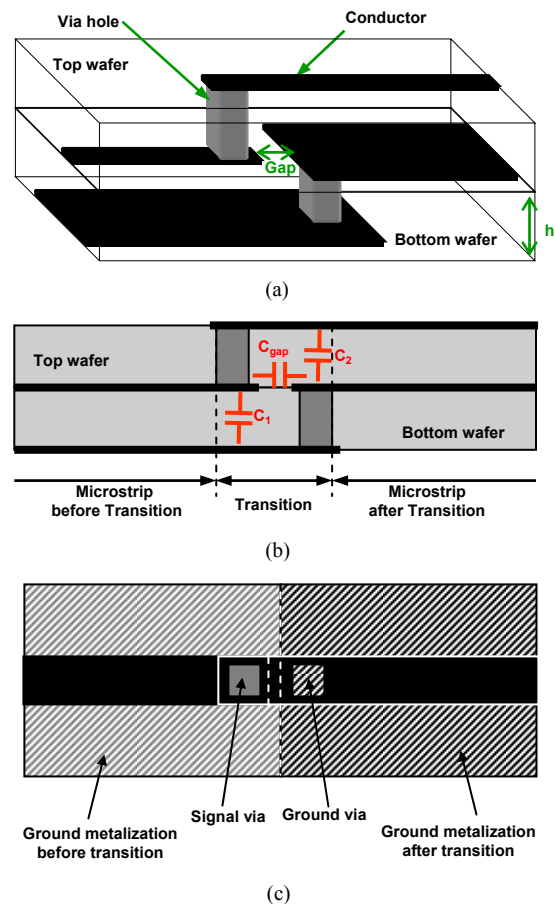


Fig. 1 Preliminary idea of vertical interconnects between two wafers (a) 3D view, (b) side view, (c) top view.

Multi-wafer microstrip transitions that exhibit the above frequencies are not available. Prior research work has focused on the development of uniplanar transitions [4] or vertical transitions that transfer the wave (signal) from the backside of a wafer to the front side of the same wafer [1]-[3]. Some examples include a coplanar waveguide (CPW) to microstrip transition on a single wafer [1], a CPW to CPW transition [2], a microstrip to coplanar stripline (CPS) transition, a slotline transition [3], and a CPS to CPW transition [4]. Different multi-layer transitions have so far been designed and demonstrated in a finite ground CPW circuit environment. Previous work from our group has successfully demonstrated a CPW-to-CPW vertical transition on silicon wafers operated at frequencies as high as W band

[5]. The study presented herein describes for the first time the development and successful demonstration of a new three-dimensional microstrip transition that can transition RF signals vertically through many wafers. These transitions have been demonstrated using two 100 μm GaAs wafers. Fig.1 illustrates the primary idea of the proposed transition. In the 3D view the wire-framed boxes represent the substrates while in the side view the substrates are recognized as solid boxes. Also for the clarity of the figure only the metal layers are depicted in the top view.

II. DESIGN AND MODELING

As shown in Fig.1 in addition to the signal lines the ground lines are finite in size and their width has been designed to provide the appropriate characteristic impedance (50 Ω). Both signal and ground lines are transitioned from a bottom wafer to the top wafer through vias. The presence of vias increases the inductance of the line locally, which has to be compensated by introducing the proper capacitance at the transition point, for the desired frequency range. To demonstrate the idea, a simple model has been derived that describes the response of such a transition very well (Fig.2). The parameters of this simplified model is derived within ADS 2003, while the physical structure is simulated and optimized using Ansoft HFSS V.9.1, for the best impedance and field match in the desired frequency range (1 GHz -20 GHz). The extension of the lines before and after the via transitions have been modeled as simple transmission lines, while the lumped circuit shown in Fig.2 represents the transition section itself.

The inductance values are governed by the shape of the via and the via pads, while the capacitance has two components, the typical parasitic capacitance seen between the signal and ground conductors of the microstrip line (C_1, C_2 in Fig.1 (b)), and the proximity capacitance of the signal and ground conductors at the midsection of the transition (C_{gap}), hence the total capacitance of $C = C_{\text{gap}} + C_1 + C_2$ should be considered. In order to derive the value of the parameters shown in Fig.2 (L_1 through L_4 and the capacitance C) as function of the given geometry, a detailed study is performed using both HFSS and ADS software. First by keeping the architecture and all the dimensions the same, the Gap size, which is the distance between the metal traces as shown in Fig.1 (a) has been varied and at each step the structure has been simulated within HFSS. Next step the wafer thickness, labeled as “h” in Fig.1 (a), is changed within steps and the new structure is simulated within HFSS. The simulated s-parameters of each of the above mentioned steps have been exported from HFSS and then imported in ADS. By utilizing the gradient optimization the best-fit value of circuit elements shown in Fig.2, are derived for each set of data. These values for the capacitance and inductances are collected and plotted

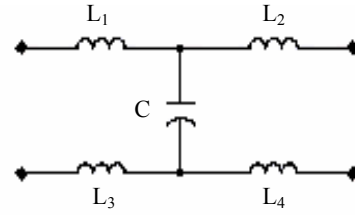


Fig. 2 Simplified model of the transition.

in Fig.3 (a) and (b), respectively. As observed from the graph in Fig.3 (a), the gap size was changed for three different wafer thicknesses ($h= 50\mu\text{m}$, $100\mu\text{m}$ and $200\mu\text{m}$). As the gap size decreases the value of the capacitance increases. Also as the wafer thickness increases the value of the capacitance decreases accordingly. By keeping the Gap size at the nominal value, $75\mu\text{m}$, and increasing the thickness of wafers the inductance value would increase relatively since the signal is forced to go through a deeper via. For a given thickness of the wafer, the L_i 's and C values can be derived from the graphs in Fig.3 (a) and (b) and the proper dimensions for the transition can be selected to optimize the performance for the desired frequency range. For a $100\mu\text{m}$ thick GaAs wafer, and gap size of $75\mu\text{m}$ the inductance and capacitance values can be read off the graphs as: $L_1 = L_2 = 0.166nH$, $L_3 = L_4 = 0.081nH$, $C = 0.0445 pf$.

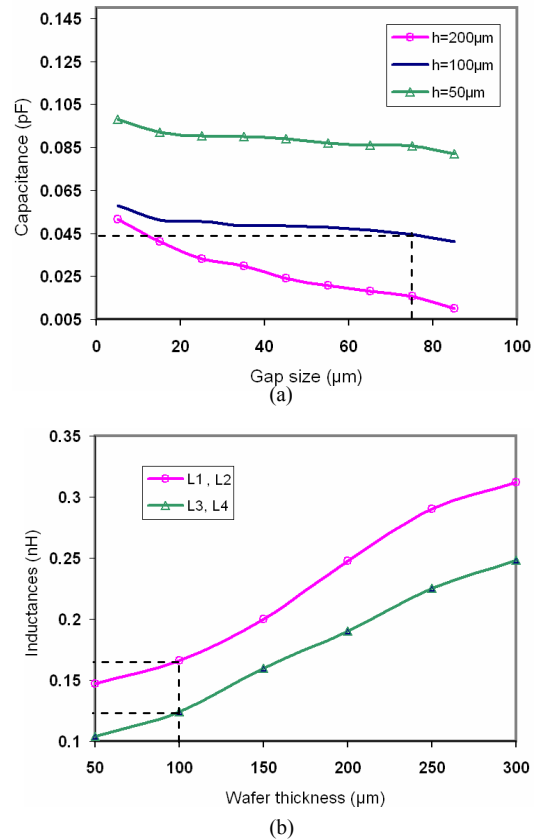


Fig. 3 Change of modeled parameter values with respect to geometry variations (a) capacitance, (b) inductances.

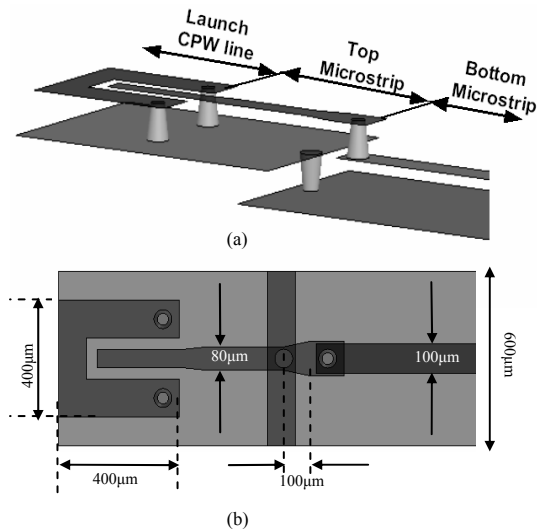


Fig. 4 Architecture of the optimized microstrip-to-microstrip vertical interconnect, (a) 3D view (b) top view.

In order to measure the s-parameters of the designed structure, a number of back-to-back transitions with different lengths in between, were fabricated. Moreover to be able to make on-wafer measurements with the CPW mode probes of a network analyzer, a CPW section of line with a signal-gap-ground size of $60\mu\text{m}-40\mu\text{m}-150\mu\text{m}$ (50Ω) was utilized and appropriate CPW-to-microstrip transitions were designed and added at both ends. In this design the vias are cylindrical with a $60\mu\text{m}$ diameter and with a pad size of $85\mu\text{m} \times 85\mu\text{m}$. As illustrated in Fig.4 (a) the signal is fed through the CPW section to the top microstrip and transits to the bottom microstrip through the vias. During the transition the ground conductor of the top microstrip and the signal conductor of the bottom microstrip are sandwiched between the two GaAs wafers (substrates are not shown in Fig.4) and this causes a change in the characteristic impedance of the line. Specifically, the characteristic impedance deviates from 50Ω to a higher value. To correct for this change, the width of the signal line is widened from $80\mu\text{m}$ on the top microstrip to $100\mu\text{m}$ wide line on the bottom microstrip, as Fig.4 (b) demonstrates.

III. FABRICATION

Fabrication of the multi-wafer transition utilizes industry standard GaAs processing and is compatible with active FET (Field Effect Transistor) fabrication and integration. Full thickness GaAs wafers are processed fully on one side and then flipped and mounted on carriers for backside processing. Backside processing includes thinning the GaAs wafer to $100\mu\text{m}$, dry etching the $60\mu\text{m}$ diameter vias, metallization, patterning and scribing. Each of the top and bottom wafers are processed separately. After completion of the fabrication steps on each of the two wafers, the top and bottom transition substrates are bonded together by a thermo-compression gold to-gold bond to form the stacked multi-wafer

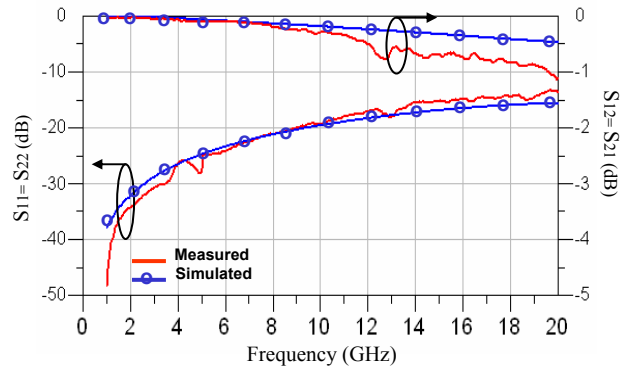


Fig. 5 Measured and simulated response of the whole structure consisting of two back-to-back microstrip-to-microstrip vertical interconnects along with the CPW-to-microstrip feed lines at both ends.

structure. Alignment is achieved by simply aligning the edges of the two wafer pieces [6]-[7].

IV. MEASUREMENTS AND SIMULATION RESULTS

The designed transitions have been fabricated and measured using the 8722 network analyzer, calibrated from 1-20GHz. As mentioned in the design section, the two-port CPW measurement is possible by fabricating a back-to-back microstrip transition with additional microstrip-to-CPW transition at both ends. Fig.5 demonstrates the measured and the simulated results of this design. As seen from the figures, the measured s-parameters agree very well with the simulated results from HFSS.

For this design, a reflection of better than 13.6dB for the whole frequency band has been achieved. The measured insertion loss is slightly higher than the simulated results due to the fact that the simulations include perfect conductors and the ohmic losses were omitted. The non-de-embedded insertion loss of better than 1.1dB up to 20GHz, has been measured. The measured insertion loss of this structure includes the insertion loss of two vertical transitions in a back-to-back configuration, along with the ohmic loss of the 1mm long microstrip line, which connects these two transitions. There are also two $600\mu\text{m}$ long sections of microstrip line, right after the CPW pads, which have to be considered when de-embedding the excess loss terms. To get a more accurate characterization of the transition response, the loss of the line sections included in the designs (approximately a total of 2.2mm long microstrip line) are de-embedded. Fig.6 demonstrates the insertion loss of the measured structure before and after de-embedding. The response of the back-to-back transition has been extracted from the measurements and plotted in this figure. Consequently the insertion loss per vertical transition has been found to be less than 0.2dB for the frequencies up to 20GHz.

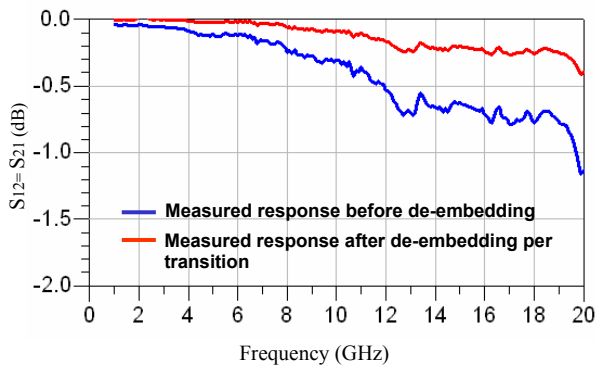


Fig. 6 Measured response of the whole structure consisting of two back-to-back microstrip-to-microstrip vertical interconnects along with the CPW-to-microstrip feed lines at both ends and the de-embedded response per transition.

V. Conclusion

Novel microstrip architecture for multi-wafer vertical interconnects compatible with industry standard GaAs active wafer technology has been demonstrated. The transition shows very low insertion loss and good return loss for frequencies up to 20GHz while maintaining a microstrip mode throughout the transition. This design opens new opportunities for further integration of multi wafer architectures in a new class of three-dimensional circuits. Since these transitions are based on microstrip architecture, the presented designs are very flexible and will result in significant reduction of chip size along with cost and power consumption.

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