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Monolithic broadband transimpedance amplifiers and their high frequency small and large signal characteristics using CBE-based GaInP/GaAs HBT technology

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Abstract

Monolithic broadband transimpedance amplifiers were developed using chemical beam epitaxy (CBE) based GaInP/GaAs HBT technology. The developed HBTs showed a cut-off frequency (f_T) of 60 GHz and a maximum oscillation frequency (f_{max}) of 100 GHz using laterally etched undercut (LEU) technology. The fabricated amplifiers had a maximum bandwidth of 19 GHz and an associated transimpedance gain of 47 dBΩ. The small and large signal characteristics of two transimpedance amplifier designs with similar gain were investigated. The cascode design when compared to the common-emitter design, provided a higher bandwidth and a more open eye diagram, as well as less sensitive to input power gain and eye diagram pattern. © 2000 Published by Elsevier Science Ltd. All rights reserved.

1. Introduction

High speed and high capacity optical transmission systems require high-speed sensitive current input preamplifiers to condition the input signal received in the form of current pulses from PIN diodes or avalanche photodiode detectors (APDs). Transimpedance feedback amplifiers are commonly used as preamplifiers with low-input impedance and flat-gain characteristics. Considerations made in the development of the transimpedance amplifiers include process yield which is related to cost reduction, bandwidth, gain flatness, sensitivity to input power, performance stability and device lifetime under actual circumstances [1].

Future optical transmission systems will operate at bit rates up to 40 $\mathrm{Gb\,s^{-1}}$ and higher and silicon devices that are traditionally used in these designs are no longer suitable for such speeds. Compound semiconductor devices have been studied extensively for such applications and provide not only a higher bandwidth of operation, but they also offer possibility of integration with photodiode. FETs were the first compound semiconductor devices used for photoreceiver applications [2,3]. State of the art photoreceivers with 27 GHz bandwidth have been demonstrated using InAlAs/InGaAs HFETs [4]. Transimpedance amplifiers have also been demonstrated using heterojunction bipolar transistors (HBTs) [5–7].

Monolithic integration, higher reliability and simple processing technology of GaAs based HBTs in addition to their improved linearity and noise performance are some of the advantages for the application of these devices in high-speed optical communication systems. AlGaAs/GaAs HBT preamplifiers based on advanced p^+ regrown extrinsic technology have demonstrated excellent performance (34.6 GHz) with a transimpedance gain of 41.6 dBΩ [8]. GaInP/GaAs HBT monolithic integrated circuits have also been used for optical communication systems at bit rates up to 10 $\mathrm{Gb\,s^{-1}}$ [9]. GaInP/GaAs HBTs are well known alternatives over AlGaAs/GaAs HBTs due to their attractive features

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such as excellent etching selectivity which contributes to process yield, device reliability [10] and improved carrier injection efficiency [11,12] due to their large valence band discontinuity. GaInP/GaAs HBT monolithic transimpedance amplifiers can be used for short distance communication (0.8 μm) such as board-to-board or chip-to-chip data links but also as an alternative solution to InP-based technology for long distance communication (1.3–1.5 μm) by means of flip chip hybrid mounted InP photodiodes.

A first report on GaInP/GaAs HBT technology and its use for high-speed transimpedance amplifiers with bandwidth exceeding 19 GHz was recently presented by the authors [13]. This paper provides further details on the design, fabrication and high frequency characteristics of transimpedance amplifier OEICs using the GaInP/GaAs HBT approach. Both small and large signal characteristics are reported. The large-signal characteristics of these amplifiers become an important issue when the front-end preamplifier receives large power signals from a photodiode as often as it occurs in optical receiver systems [14]. Advanced systems of this type, use a variable gain preamplifier to establish a linear regime of operation [1]. Another alternative is the use of a simple high gain preamplifier as a limiting amplifier. In this case, the amplifier operates in large-signal regime which can affect its speed and output signal waveform and consequently the bit-error-rate performance of the optical receiver system. Section 2 of the paper presents HBT design consideration and the process technology applied to device and circuit fabrication. Section 3 presents the design and experimental characteristics of transimpedance amplifiers using this technology. The large-signal properties of the amplifiers are reported in Sections 4 and 5.

2. HBT design and process technology

In this work, the single GaInP/GaAs HBTs were optimized in terms of microwave performance by evaluating an appropriate layer structure and process. A GaInP tunneling emitter barrier design was chosen, since the tunneling barrier acts as a “mass filter” and provides a much higher ratio of tunneling probabilities, a higher emitter injection efficiency, and high transconductance compared with traditional designs leading therefore to an improved microwave performance. The thin tunneling barrier was sandwiched between the n-type emitter and p-type base of an otherwise homojunction bipolar transistor design. Details of this tunneling HBT design were reported earlier by the authors [15].

The GaInP/GaAs HBTs were fabricated on layers which were grown by a specially developed hydride and hydrogen-free chemical beam epitaxy (CBE) process which guaranteed a very high degree of reproducibility of growth parameters with small defect content and high output capability [16]. The process starts with Ti/Pt/Au non-alloyed metal deposition for emitter contacts followed by an etch of InGaAs, GaAs emitter caps, and GaInP emitter. A short separation of 0.1 μm between the self-aligned base and the emitter assures small base resistance and hence improved maximum oscillation frequency. The base metal consists of Pt/Ti/Pt/Au and was deposited on a 600 Å thick GaAs base. The process was followed by etching the GaAs base and collector regions and then deposition of Ti/Pt/Au for collector contact. Laterally etched undercut (LEU) was developed and applied to the collector region to further reduce base–collector capacitance (C_{BC}) while avoiding base resistance degradation. The collector layer under the base contact was removed for this purpose. Fig. 1 shows the SEM cross-section pictures of the fabricated HBT (a) without and (b) with LEU technology. The 2×30 μm^2 single emitter HBTs were measured using a network analyzer from 0.5 to 25.5 GHz. A reduction of C_{BC} from 46.7 to 36.5 fF by lateral etching of about 6000 Å leads to 10% gain improvement at 10 GHz as shown in Fig. 2 and a higher maximum oscillation frequency. The most commonly used approach for minimizing C_{BC} is based on ion-implantation through the active base layer. The

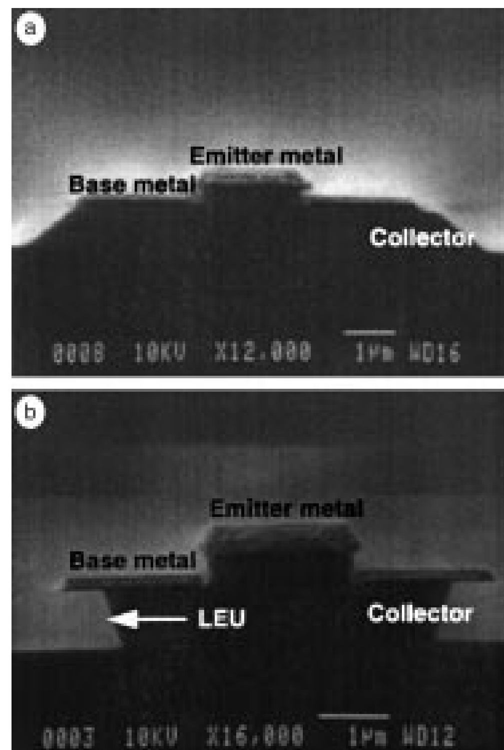


Fig. 1. Cross section of the device with laterally etched undercut technique.

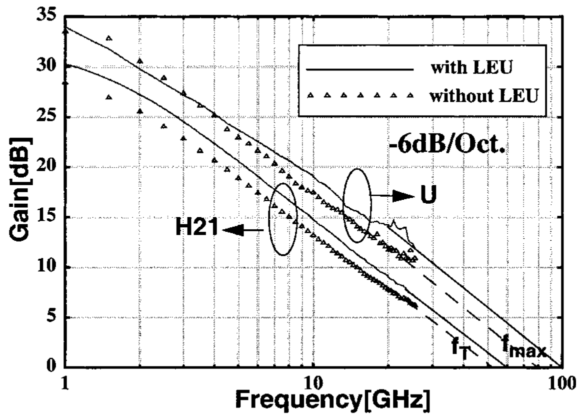


Fig. 2. Microwave performance of 2×30 μm^2 single emitter HBT with and without LEU technology at $V_{CE} = 2.5$ V, $I_C = 20$ mA.

process analyzed here is based on LEU of the collector layer and offers therefore simplicity and a very effective way of reducing C_{BC}.

The key in this technology step is the incorporation of a thin (1×10^{19} cm^{-3} doped) GaInP layer between the n^+ and n^- GaAs collector which provides selectivity in etching and determines the etching profile below the base. The 2×30 μm^2 single emitter HBTs fabricated using LEU technology demonstrated an f_T of 58 GHz and f_{max} of 100 GHz at $I_C = 20$ mA, $V_{CE} = 2.5$ V. This corresponds to an f_T increase of 11% and f_{max} increase of 25% as a result of using LEU technology as shown in Fig. 2. The microwave performance of the investigated GaInP/GaAs HBTs shows only a slight change with bias and therefore permits robust circuit design. The HBTs showed a thermal resistance of 1430 K W^{-1} as explained in Section 3.

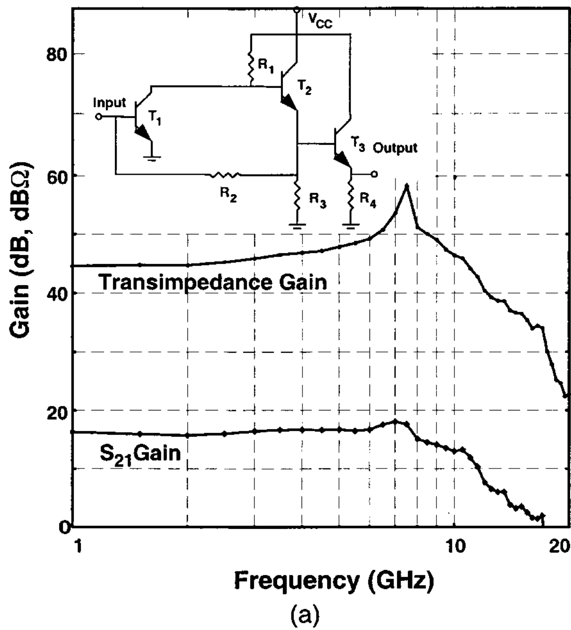
The technology used to fabricate the monolithic integrated circuits employs additional steps of Ni–Cr thin metal film deposition for monolithic resistors and Al_2O_3 film deposition as the insulator for high-Q MIM monolithic capacitors. A SiO_2 PECVD deposited layer was used as the final step for HBT passivation and was found to induce very little degradation to the HBT characteristics.

3. Design and experimental performance of the transimpedance amplifiers

The 2×30 μm^2 single emitter HBT was modeled using small and large-signal equivalent circuit models developed by the authors which were introduced in HP EESOF LIBRA and HSPICE [17,18]. The small-signal high-frequency model is based on physical parameters and is extracted directly from cold and hot S-parameter measurement [17]. The large-signal model is based on Gummel–Poon equivalent circuit and includes a thermal resistance that accounts for device heating [18]. The temperature effect is observed under high dissipated power conditions when the junction temperature rise manifests itself with a negative slope in I_C–V_{CE} characteristics. The large-signal model combines the small-signal equivalent circuit with data obtained from DC parameters extracted from Gummel-plots and I_C–V_{CE} characteristics. This model also accounts for parasitic reactances due to device interconnects. Both small and large-signal HBT equivalent circuits were developed within HP-EESOF LIBRA environment for compatibility with high-frequency circuit simulation needs. Circuit design was carried-out using models for HBTs, resistors and capacitors in different LIBRA environments such as linear, DC, large signal S-parameters and harmonic-balanced test benches.

The inset of Fig. 3(a) shows the schematic of the common-emitter based transimpedance amplifier (design A) employed in this work. The input signal current is amplified by the common emitter stage of transistor T_1 and resistor R_1. The feedback network which consists of resistors R_2 and R_3 stabilizes the transimpedance gain. Transistor T_2 serves as a buffer to isolate the feedback network from the gain stage. T_3 and R_4 behave as another buffer to isolate the feedback network and output. The inset of Fig. 3(b) shows the schematic of another transimpedance amplifier (design B) which was also explored and fabricated in the same lot. The schematic is identical to that of the simple transimpedance amplifier of Fig. 3(a) except that in this case, a cascode topology is used as the gain stage. As shown in the following, the cascode design not only improves the bandwidth, but also contributes to better large signal performance.

Fig. 3(a) also shows the measured small-signal transmission coefficient (S_{21}) and transimpedance gain of the common-emitter based transimpedance amplifier measured with an HP 8722D network analyzer. A S_{21} gain of 17 dB with a bandwidth of 10 GHz has been measured using on-wafer probe measurement. Fig. 3(b) shows S_{21} and transimpedance gain of the cascode based transimpedance amplifier. A similar S_{21} gain of 17 dB with a bandwidth of 15 GHz has been achieved for bias condition A ($V_{CC} = 5$ V). The transimpedance gain was 47 dB Ω and 50 dB Ω for designs A and B, respectively. By increasing the collector voltage of the cascode stage (bias condition B, $V_{CC} = 7$ V), the bandwidth could be increased to 19 GHz while the associated S_{21} and transimpedance gain were 12 dB and 47 dB Ω, respectively. Fig. 4 shows a photograph of the fabricated transimpedance circuit (design A). Coplanar waveguide transmission lines were employed to connect the amplifier to 50 Ω terminations. The chip size for the circuits was 1125×800 μm^2.



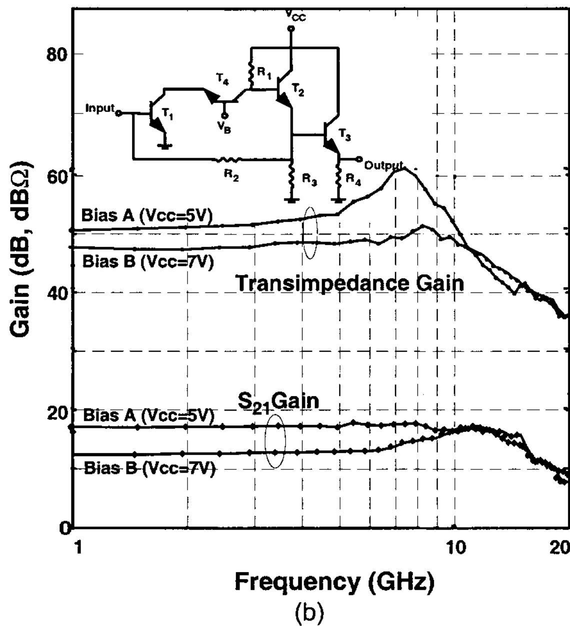


Fig. 3. Transmission coefficient S_{21} and transimpedance gain of (a) design A and (b) design B vs. frequency. The schematics are also shown in the insets.

4. Large signal analysis

To show the effect of input signal on DC biasing of amplifiers, we have first performed a comparison of transimpedance amplifier characteristics based on analytical expressions and a simple T-equivalent circuit for HBTs. This analysis was done at small frequencies (DC to 1 GHz) for which the junction reactances are negligible so that an estimate of circuit performance can be made on a DC basis without significant impact from reactive elements. Fig. 5(a) shows the circuit schematics of the cascode transimpedance amplifier (design B) using the HBT T-equivalent circuit. The emitter current of the input transistor (T_1) can be written as

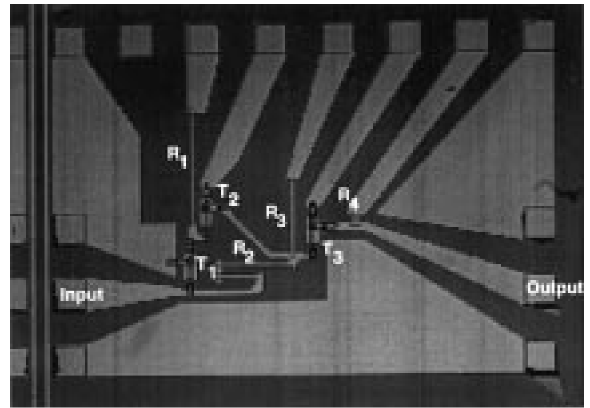


Fig. 4. Photograph of the fabricated transimpedance amplifier. (Design A).

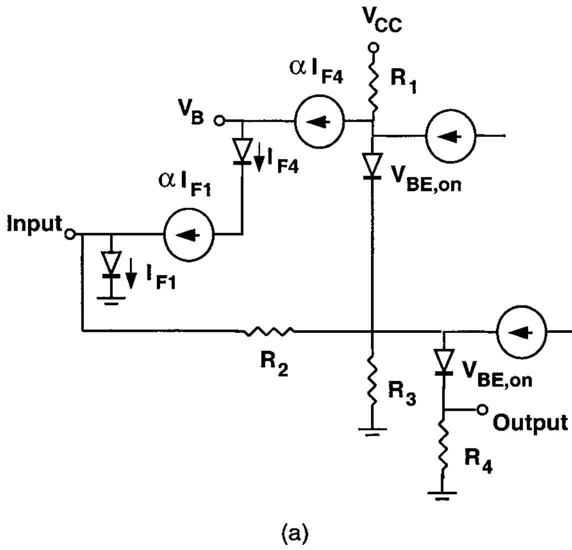
$$I_{F1} = I_0 e^{(V_{BE}+V_{in})/V_T} = I_{F1Q} e^{V_{in}/V_T}, \tag{1}$$

where I_{F1} is the emitter current of T_1, I_{F1Q} is the quiescent component of the emitter current, I_0 is the emitter–base dark current, α is the HBT emitter injection efficiency, V_{BE} is the quiescent component of the base–emitter voltage, V_{in} is a sinusoidal input voltage and V_T is the thermal voltage. For the purpose of the analysis, it is assumed that all HBTs in the circuit have the same current gain since they are all operating around the same bias condition. One can find the quiescent current component I_{F1Q} and the output voltage V_{out} for this circuit as

$$I_{F1Q} = \frac{V_{CC} - 2V_{BE,on}}{(1-\alpha)R_2 + \alpha^2 R_1 e^{V_{in}/V_T}}, \tag{2}$$

$$V_{out,cascode} = V_{CC} - 2V_{BE,on} - \alpha^2 R_1 I_{F1Q} e^{V_{in}/V_T}. \tag{3}$$

Therefore, the DC component of the output voltage can be approximated by the average of minimum and maximum voltage of the output signal with 90° and 270° phase shift, respectively with respect to the input. By employing the same approach, one can also establish a DC large-signal model for the common-emitter transimpedance amplifier (design A). The output voltage, in this case, is given by the following equation.



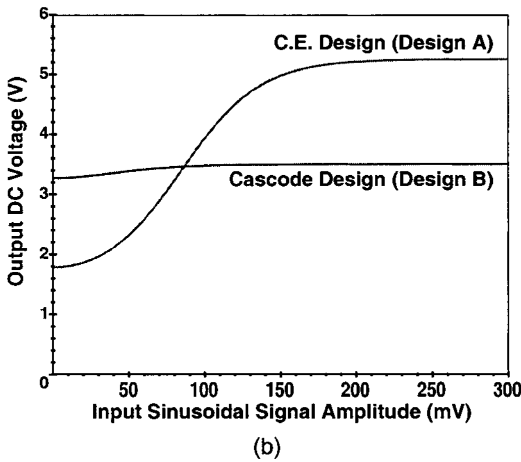


Fig. 5. (a) T-equivalent circuit of cascode transimpedance amplifier. (b) DC component of the output voltage as a function of input voltage, simulated using T-equivalent large-signal model of the HBT.

$$V_{\text{out,common-emitter}} = (V_{\text{CC}} - 2V_{\text{BE,on}}) \times \frac{(1-\alpha)R_2}{(1-\alpha)R_2 + \alpha R_1 \mathrm{e}^{V_{\text{in}}/V_{\text{T}}}}. \quad (4)$$

Based on the previously described theory, one can estimate the change of the output voltage DC component as the input voltage swing increases for the two different designs. Such a comparison is shown in Fig. 5(b), where the DC component of the output voltage is plotted vs. the amplitude of the sinusoidal input voltage. Design A which is based on the common-emitter approach shows a larger variation of the DC bias for the output stage transistor T_3 due to self-biasing. Self-biasing occurs when the non-linear operation of the transistor generates by rectification an additional DC component which effectively changes the operating bias of the transistor. Transistor HBT T_2 of the previous stage of design A also shows significant self-biasing while transistor HBT T_2 of design B is not subjected to significant self-biasing.

To explain the difference in the output voltage DC component, one should notice that the two amplifiers compared in this study were designed to provide similar gain. In common-emitter design (design A), HBT T_1 has a large voltage gain and therefore a large effective Miller capacitance is in parallel to resistor R_1. In order to keep the gain high, the value of R_1 must be higher than that of design B (cascode configuration) in which the Miller effect is minimal ($R_1 = 400\ \Omega$ in design A vs. $R_1 = 75\ \Omega$ in design B). Since optimal bias needs to be employed for large bandwidth of operation, the bias voltage of the circuit (V_{CC}) has to increase to provide the same current in resistor R_1 ($V_{\text{CC}} = 12$ V in design A vs. $V_{\text{CC}} = 5$ V in design B to provide 20 mA current in R_1). The optimum collector–emitter voltage for the HBTs employed in the circuits is 3 V and transistor T_1 of design A is biased at 3 V, while its maximum collector voltage can reach 12 V. On the other hand, the minimum attainable collector voltage of this transistor, neglecting the offset voltage, is close to 0 V. Therefore, at high input power, transistor T_1 operates between 0 and 12 V resulting in a shift of collector voltage DC component to about 6 V. Design B, however, shows a smaller shift in DC components in presence of high input power due to smaller V_{CC}, and thus the self-biasing is not pronounced in this design; under high power input signal conditions, the cascode design corresponds to signal swings between 0 and 5 V.

Self-biasing effects can deteriorate the gain of the amplifier by driving the HBT out of its optimum bias setting. It manifests by a reduction of the forward transmission coefficient S_{21}, but may also result in pronounced input and output mismatching (higher S_{11} and S_{22}). Full large-signal S-parameter simulation was performed for this purpose in a second step of the analysis. The transimpedance circuits were analyzed for this purpose using the large-signal model developed by the authors for GaInP/GaAs HBTs [18]. Fig. 6(a) shows the change in S_{11}, S_{21} and S_{22} parameters for the amplifier of design A as the input incident power increases. The simulation is performed at three different frequencies to view the effect of HBT reactances on large signal S-parameters. The large signal forward transmission coefficient S_{21} reduces as the input power increases. This reduction is pronounced at smaller frequencies (2 and 5 GHz) where the HBT reactive elements such as C_{BC} and C_{BE} are negligible. The input signal passes, in this case, primarily through nonlinear elements of the HBT such as base–emitter diode and the gain varies in a non-linear fashion with the input power level. At higher frequencies

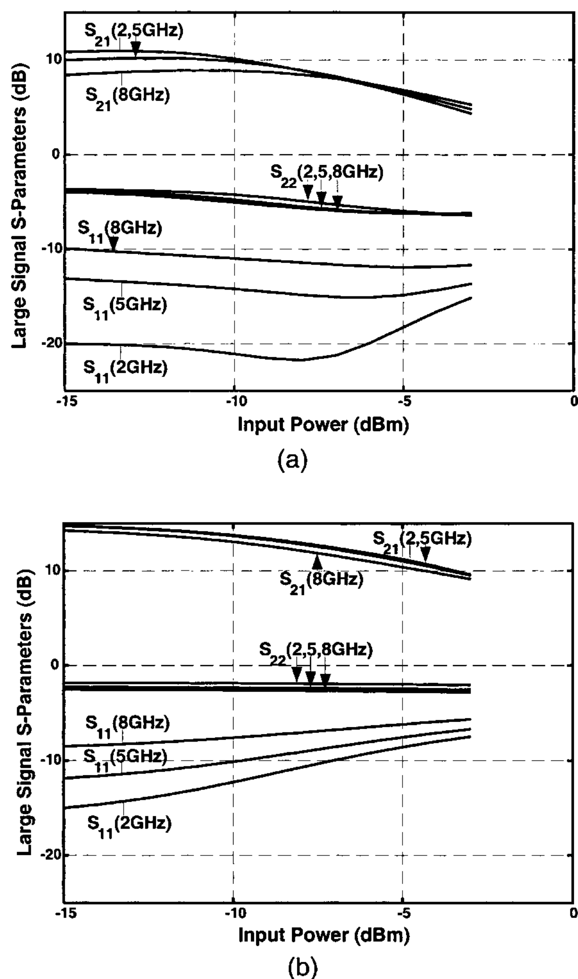


Fig. 6. Simulated Large-signal S-Parameters of (a) design A transimpedance amplifier, (b) design B transimpedance amplifier vs. input power at 2, 5 and 8 GHz frequency using HP-EESOF LIBRA.

(8 GHz), a significant part of the signal passes through reactive elements (C_{BC} and C_{BE}) which are linear by a first degree approximation. Therefore, the amplifier itself behaves more linearly resulting in less variation of the large-signal S_{21} parameter. The large-signal input and output reflection coefficients S_{11} and S_{22} also depend upon input power as shown in Fig. 6(a). Large-signal S_{22} improves slightly as the input power increases. Large-signal S_{11} also improves at higher frequencies (5 and 8 GHz) as the input power increases. At low frequencies (2 GHz), however, S_{11} increases significantly and leads to rapid power gain compression.

Fig. 6(b) shows the large-signal transmission and reflection coefficients of the amplifier based on cascode design (design B). The large-signal forward transmission coefficient S_{21} is found in this design to have a much smaller dependence on input power. As the frequency increases, S_{21} decreases slightly for all shown input power levels. The large-signal output reflection coefficient S_{22} is almost independent on input power for design B at different frequencies as is depicted in Fig. 6(b). The large-signal input reflection coefficient S_{11}, however, increases as the input power increases. This results in power gain compression of the amplifier at large input signal.

As mentioned earlier, in the case of the cascode transimpedance amplifier of design B, the large signal S_{21} diminishes slightly as the input power is increased despite the fact that self-biasing is not important (Fig. 6(b)). This is due to less efficient amplification in the frequency of interest under non-linear operation conditions where part of the injected carriers from the base to the collector lead to higher harmonic frequency components. The latter is verified by examining the output power spectrum as the input signal is increased. This was done by performing harmonic-balanced simulation based on the developed HBT large-signal model. As expected, the higher harmonic components of the output power of the amplifier of designs A and B increase as the input incident power increases. Fig. 7 shows these features by assuming that the fundamental frequency for amplification is 5 GHz and examining multiples of this frequency. One may observe that the output power lost in harmonics is much higher in the case of design A at power levels beyond -12 dBm where the device behaves in strongly non-linear fashion. As a result, the gain degradation with input power level is expected to be smaller in design B.

The impact of input incident power on the power gain of the transimpedance amplifiers of designs A and B was also investigated using the harmonic-balanced approach. Fig. 8(a) shows the power gain of design A

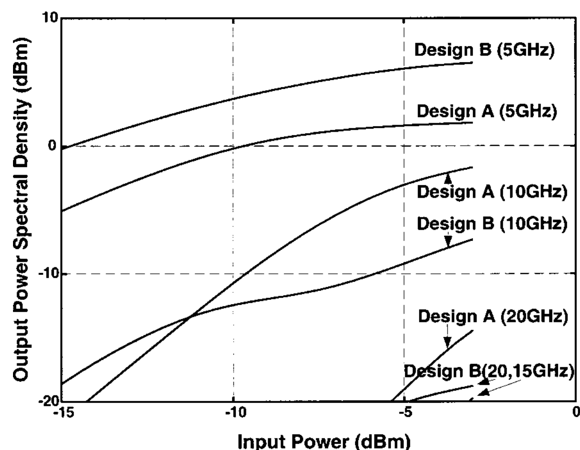


Fig. 7. Simulated fundamental and higher harmonic components of output power as a function of input power for design A and B at 5 GHz fundamental frequency.

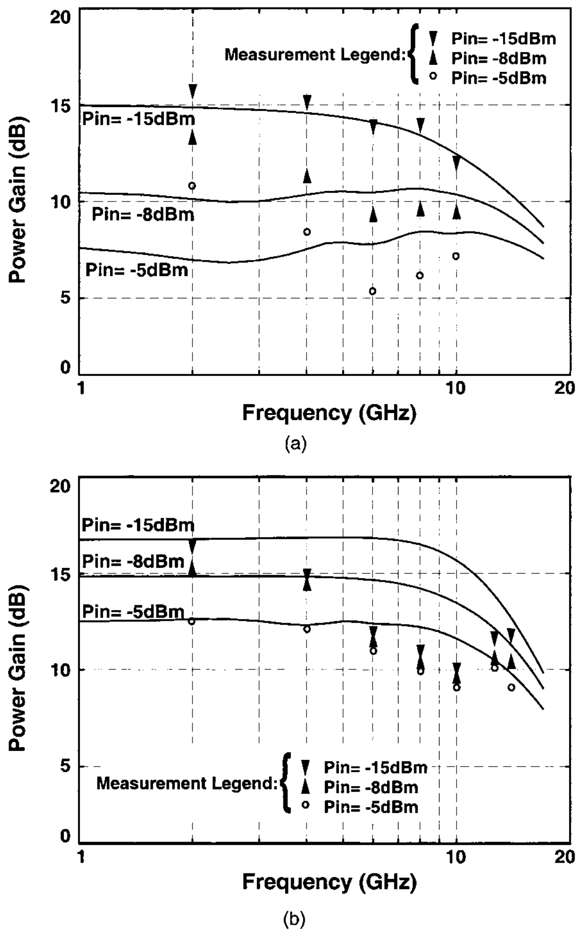


Fig. 8. Measured and harmonic-balanced simulation of power gain vs. frequency as a function of input power for (a) design A transimpedance amplifier, (b) design B transimpedance amplifier.

amplifier as a function of frequency for different input power. Notice that the power gain reduces dramatically as the input power increases due to both self-biasing and reduction of large-signal gain under non-linear operation conditions. Fig. 8(b) shows the power gain of design B transimpedance amplifier as a function of frequency for different input power levels. The reduction in gain is less significant due to the suppression of self-biasing. The pronounced input mismatch as well as non-linear operation of the amplifier are, however, found to reduce the gain slightly at higher input power.

5. Experimental characteristics of the transimpedance amplifiers

The large signal performance of the two transimpedance designs was evaluated using an HP 8722D network analyzer and the output power was monitored with a power meter for higher accuracy. Fig. 9(a) and (b) shows the P_{out}–P_{in} characteristics for different frequencies for common-emitter based (design A) and cascode based (design B) transimpedance amplifiers, respectively. The chips compared showed similar gain-frequency characteristics under small-signal conditions. The common-emitter transimpedance amplifier (design A) shows a more pronounced gain compression especially at lower frequencies. The cascode transimpedance circuit, however, shows very small gain compression at high input power. This is mainly due to the fact that self-biasing effects resulting from the presence of large signal input conditions are reduced in this design as explained theoretically in Section 4.

Frequency dependence tests of the large-signal gain proved again the superiority of the cascode design in terms of immunity to increased input power level conditions. Fig. 8(a) and (b) shows a comparison of the

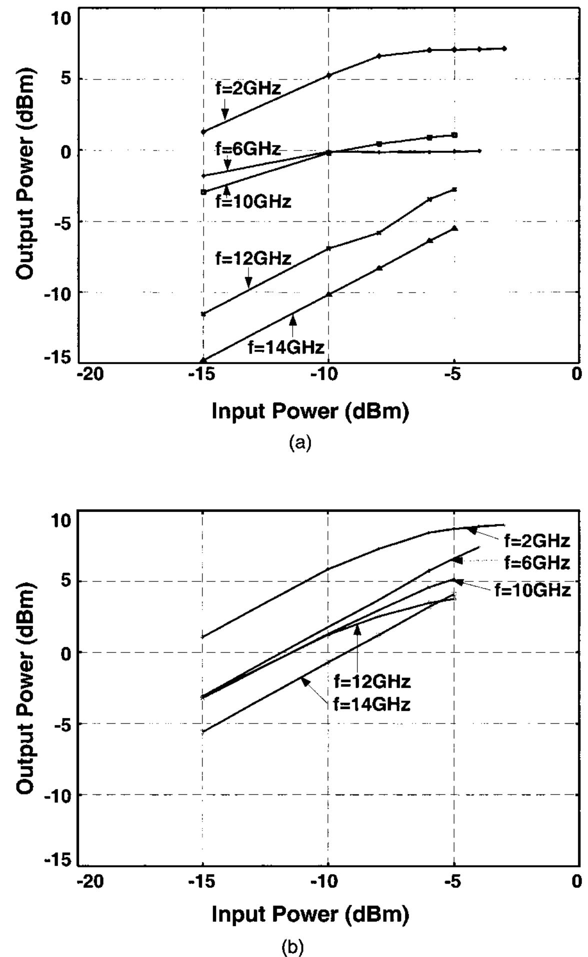


Fig. 9. Measured P_{out}–P_{in} characteristics of (a) design A and (b) design B transimpedance amplifiers.

measured and simulated power gain vs. frequency characteristics for design A and B amplifiers when the input power is varied. The power gain of the cascode based design (design B) shows a much smaller dependence on input power as the input power is varied over the entire measured frequency range.

A comparison between the collector currents of transistor T_3 (output stage) of these two designs revealed that in the case of design A, the collector current increases from the nominal value of 18–48 mA as the input power increases from −15 to −3 dBm. The cascode design however shows a negligible current increase. Overall, the cascode design appears to be less sensitive to increased input power levels. This feature, in addition to a higher bandwidth, make the cascode design a better choice for optoelectronic applications.

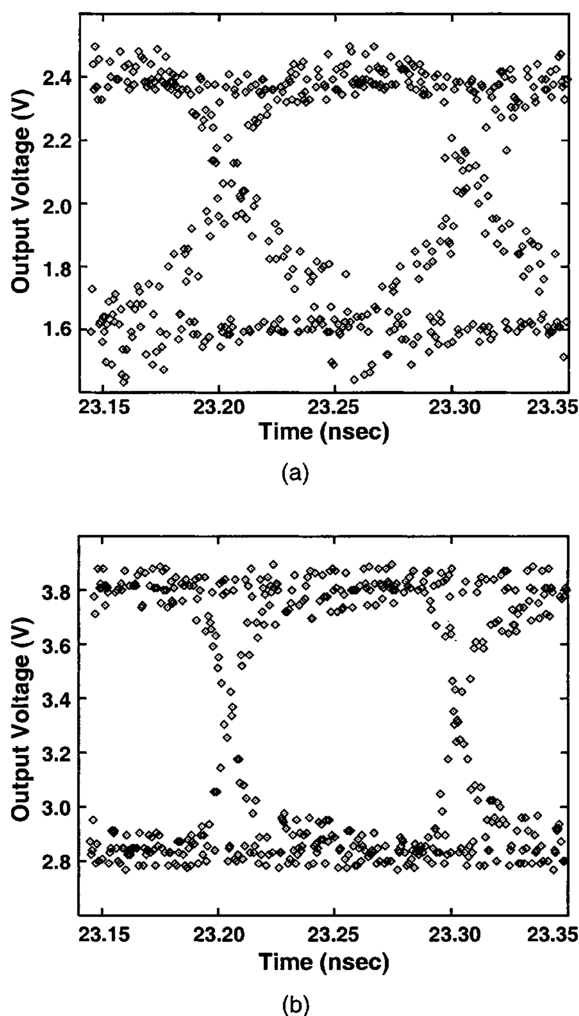


Fig. 10. Output waveform eye diagram for 10 Gbs^{-1} 2^{15}-1 NRZ input signal for (a) design A and (b) design B transimpedance amplifiers.

The eye diagrams of the two transimpedance amplifiers were obtained using an Anritsu MP1701B 10 GHz random pattern generator and a Tektronix 11801B 50 GHz sampling oscilloscope. Both transimpedance amplifiers were subjected to a 2^{15}-1 NRZ PRBS signal at 10 GHz input data for eye diagram measurement. The resultant eye diagrams of designs A and B are shown in Fig. 10(a) and (b), respectively. The cascode based design (design B) shows a much more open and clear eye pattern even at smaller input excitation (Fig. 10(b)). The common-emitter based design (design A) showed an acceptable response at large input excitations (Fig. 10(a)). For smaller input signal, however, the eye pattern showed not only a more noisy amplitude of the output signal, but also non-consistent rise and fall times resulting in a more closed and noisier eye pattern. This is an indication of higher bit error rate at lower input excitation for transimpedance amplifier of design A.

6. Conclusions

Broadband transimpedance amplifiers were designed, fabricated and tested using an CBE-based GaInP/GaAs HBT technology which is promising due to the combination of good electrical performance with process simplicity as necessary for production of high-speed and high capacity transmission systems. A maximum bandwidth of 19 GHz and associated transimpedance gain of 47 dB Ω were achieved using a cascode design approach. Two transimpedance designs were compared and the design based on the cascode approach showed larger bandwidth and a much smaller input power dependence. For the same gain characteristics, cascode configuration requires a smaller collector resistance comparing to the common-emitter configuration due to reduced Miller effect in cascode design. This will translate into a smaller power supply requirement in cascode design for the same optimum collector current. Therefore, the self-biasing effect can be significantly reduced in the cascode configuration resulting in a smaller sensitivity to input power. Eye diagrams of these two amplifiers were measured at 10 GHz and a much more open and clear eye pattern was achieved for the cascode configuration.

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References

[1] Meyer RG, Mack WD. A wideband low-noise variable-gain BiCMOS transimpedance amplifier. IEEE J Solid-State Circ 1994;29(6):701–6.

[2] Gutierrez-Aitken AL, Bhattacharya P, Chen YC, Pavlidis D, Brock T. High-performance monolithic PIN-MODFET transimpedance photoreceiver. IEEE Photonics Technol Lett 1993;5(8):913–5.

[3] Scheinberg N, Bayruns RJ, Laverick TM. Monolithic GaAs transimpedance amplifiers for fiber-optic receivers. IEEE J Solid-State Circ 1991;26(12):1834–9.

[4] van Waasen S, et al. 27-GHz bandwidth high-speed monolithic integrated optoelectronic photoreceiver consisting of a waveguide fed photodiode and an InAlAs/InGaAs-HFET traveling wave amplifier. IEEE J Solid-State Circ 1997;32(9):1394–401.

[5] Lunardi LM, Chandersekhar S, Gnauck AH, Burrus CA, Hamm RA, Sulhoff JW, Zyskind JL. A 12 Gb/s high-performance, high-sensitivity monolithic pin/HBT photoreceiver module for long-wavelength transmission systems. IEEE Photonics Tech Lett 1995;7(2):182–4.

[6] Gutierrez-Aitken AL, Yang K, Zhang X, Haddad GI, Bhattacharya P, Lunardi LM. 16-GHz bandwidth InAlAs–InGaAs monolithically integrated pin/HBT photoreceiver. IEEE Photonics Tech Lett 1995;7(11):1339–41.

[7] Chandrasekhar S, Glance B, Dentai AG, Joyner CH, Qua GJ, Sulhoff JW. Monolithic balanced pin/HBT photoreceiver for coherent optical heterodyne communications. IEEE Photonic Tech Lett 1991;3(6):537–9.

[8] Suzuki Y, Shimawaki H, Amamiya Y, Fukuchi K. An HBT preamplifier for 40 Gb/s optical systems. IEEE GaAs IC Symp Dig 1996;203–6.

[9] Ihara T, Oikawa Y, Yamamoto T, Tomoguji H, Hamano H, Ohnishi H, Watanabe Y. InGaP/GaAs HBT IC chipset for 10 Gb/s optical receiver. IEEE GaAs IC Symp Dig 1996;262–5.

[10] Takahashi T, Sasa S, Kawano A, Iwai T, Fujii T. High-reliability InGaP/GaAs HBTs fabricated by self-aligned process. 1994 IEDM Tech Dig 1994;191.

[11] Razeghi M, Omnes F, Defour M, Maurel Ph, Hu J, Pavlidis D. High performance GaAs/GaInP HBTs grown by MOCVD. Sem Sci Tech 1990;5:278–80.

[12] Fresina MT, Ahmari DA, Mares PJ, Hartmann QJ, Feng M, Stillman GE. High-speed, low-noise InGaP/GaAs HBTs. IEEE Electron Dev Lett 1995;16(12):540–1.

[13] Park JW, Mohammadi S, Pavlidis D, Dua C, Garcia J-C. GaInP/GaAs HBT Broadband Monolithic Transimpedance Amplifiers and their High-Frequency small and large signal characteristics. IEEE MTTS International Microwave Symposium Technical Digest, (IEEE Radio Frequency Integrated Circuits, RFIC '98). Baltimore MD, 1998;1: 39–42.

[14] Nagano N, Suzaki T, Kasahara K, Takeuchi T, Honjo K. Monolithic ultra-broadband transimpedance amplifiers using AlGaAs/GaAs HBTs. IEEE Trans Microwave Theory Tech 1994;42(1):2–9.

[15] Park JW, Pavlidis D, Mohammadi S, Guyaux J-L, Garcia J-C. High speed tunneling emitter GaInP/GaAs HBTs. IEEE Trans Electron Dev 2000, submitted for publication.

[16] Garcia JC, Dua C, Mohammadi S, Park JW, Pavlidis D. Growth characterization of Hydride-free CBE and application of GaInP/GaAs HBTs. J Electron Mater 1998; 27(5):442–5.

[17] Pehlke D, Pavlidis D. Evaluation of the factors determining HBT high-frequency performance by direct analysis of *S*-parameter data. IEEE Trans Microwave Theory Tech 1992;40:2367–73.

[18] Samelis A, Pavlidis D. Analysis of the large-signal characteristics of power HBTs exhibiting self-heating effects. IEEE Trans Microwave Theory Tech 1997;45:534–42.