

# Exam 2

*ECE 559: MOS VLSI Design (Fall 2009)*

*ECE Department, Purdue University*

*November 5, 2009*

Name: \_\_\_\_\_

PUID: \_\_\_\_\_

**Instructions:** It is important that you clearly show your work and mark the final answer clearly, closed book, closed notes, no calculator.

**Time:** 1 hour 15 minutes

## Scoring

**Problem 1 (Total 30 points)**

Part a) 10 points \_\_\_\_\_

Part b) 10 points \_\_\_\_\_

Part c) 10 points \_\_\_\_\_

**Problem 2 (Total 40 points)**

Part a) 10 points \_\_\_\_\_

Part b) 10 points \_\_\_\_\_

Part c) 10 points \_\_\_\_\_

Part d) 10 points \_\_\_\_\_

**Problem 3 (30 points)** \_\_\_\_\_

**Total:** 100 points \_\_\_\_\_

**Problem 1:****[30 points]****Part a)** Draw *positive* and *negative*  $C^2$ MOS latches. Clearly show the applied clock signals.**[10 points]**

**Part b)** Implement NOR operation **using static logic** as a pipelined datapath using C<sup>2</sup>MOS latches that *avoids any race-condition due to clock overlaps*. Clearly draw all the transistors and the applied clock signals in your diagram. Write your assumptions, if any.

**[10 points]**

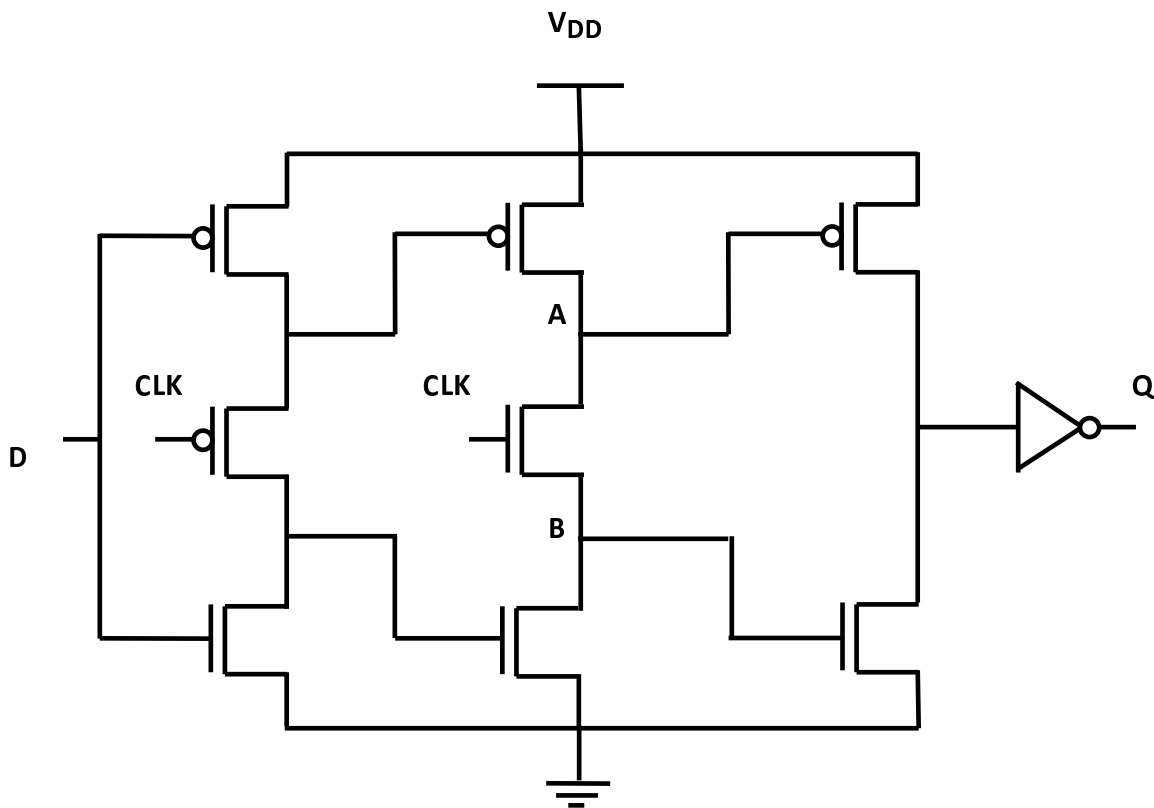
**Part c)** Implement NOR operation **using dynamic logic** as a pipelined datapath using C<sup>2</sup>MOS latches that *avoids any race-condition due to clock overlaps*. Clearly draw all the transistors and the applied clock signals in your diagram. Write your assumptions, if any.

**[10 points]**

**Problem 2:** Consider the edge-triggered register shown below. Clearly and concisely answer the following questions with explanation. Write your assumptions, if any.

[40 points]

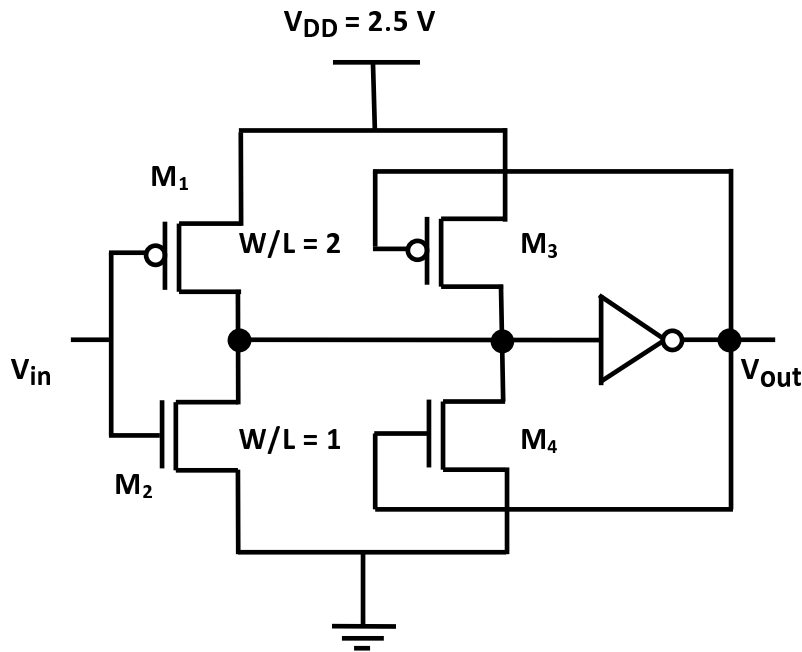
- a) What are the minimum and maximum voltages possible at the nodes A and B? [10 points]
- b) Determine the set-up time. [10 points]
- c) Determine the propagation delay. [10 points]
- d) Determine the hold time. [10 points]





**Problem 3:** Consider the Schmitt trigger circuit shown below. Find the widths of the transistors  $M_3$  and  $M_4$  to have  $V_{M^-} = 1\text{ V}$  and  $V_{M^+} = 2\text{ V}$ . Clearly write the *regions of operation* of the transistors during your calculation and write your assumptions, if any.

[30 points]



$$K_p' = \mu_p C_{ox} = 50e-6 \text{ A/V}^2$$

$$K_n' = \mu_n C_{ox} = 100e-6 \text{ A/V}^2$$

$$V_{tp} = -0.5 \text{ V}, V_{tn} = 0.5 \text{ V}$$

$$L = 300 \text{ nm}$$





**Scratch Paper 1**

**Scratch Paper 2**