Exam 3

ECE 559: MOS VLSI Design (Fall 2009)

ECE Department, Purdue University

December 3, 2009

Name: SOLUTION

PUID: _____

Instructions: It is important that you clearly show your work and mark the final answer clearly, closed book, closed notes, no calculator.

Time: 1 hour 15 minutes

Scoring

Problem 1 (Total 30 points)

Part a) 20 points _____

Part b) 10 points _____

Problem 2 (Total 30 points)

Part a) 15 points _____

Part b) 15 points _____

Problem 3 (Total 40 points)

Part a) 20 points _____

Part b) 20 points _____

Total: 100 points _____

Problem 1: Consider an inverter of minimum size (input capacitance of C_i) driving a load C_L, which is x times large as C_i ($C_L = x.C_i$) . The width of the PMOS transistor is a times larger than the NMOS transistor. You decide to introduce another inverter (transistor widths are u times larger than the first for both PMOS and NMOS) between the minimum sized inverter and the load C_L.

Answer the following questions. Clearly state your assumptions, if any.

[30 points]

a) What should u be to minimize the delay? Show your calculations. **[20 points]**

b) If $x = 5$, does it make sense to introduce the second inverter? Explain your answer. (Without explanation, you will not get any points.) **[10 points]**

Solution:

a) Let the propagation delay of a minimum sized inverter driving another minimum sized inverter is t_{p0}.

Then, the propagation delay of a minimum sized inverter driving a load C_L (where, $C_L = x.C_i$),

$$t_{p1} = x.t_{p0}.$$

Note that the proportionality factor between the internal capacitance and the input capacitance has been assumed as 1.

If the second inverter is added, the total propagation delay would be,

$$t_{p2} = u.t_{p0} + (x.C_i / u.C_i).t_{p0} = (u + x/u).t_{p0}.$$

To get the value of u that minimizes the delay t_{p2}, we need to differentiate t_{p2} with respect to u. Accordingly,

$$1 - x/u^2 = 0$$

i.e., $u = \sqrt{x}$.

Accordingly,

$$t_{p2,\,opt} = (\sqrt{x} + x/\sqrt{x}).t_{p0} = 2\sqrt{x}\ t_{p0}.$$

b) It makes sense to introduce an inverter when

$$t_{p2,\,opt} < t_{p1}$$

i.e., $2\sqrt{x} < x$

i.e., $x > 4.$

So, if x = 5, it makes sense to introduce the second inverter as we will have lower propagation delay in that case.

Note: we are comparing two different configurations of two different areas. With the introduction of the second inverter, the overall area required for the second configuration is increased. We could have argued for an *iso-area* comparison.

Problem 2: Consider a standard 6-T SRAM cell as shown in the below diagram. Due to *Random Dopant Fluctuation (RDF)*, transistors in a single cell may have different *threshold voltages* than that of what was designed for. Assume that the cell is designed for

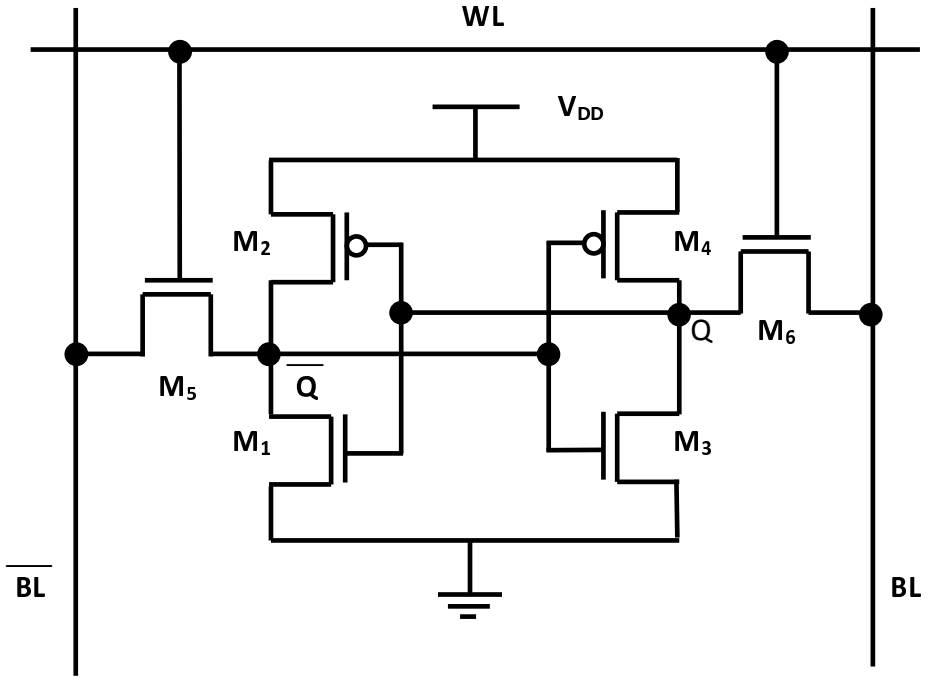
$$V_{DD} = 1\ V,\ V_{tn} = 0.3\ V,\ V_{tp} = -0.3\ V.$$

Consider that due to *RDF*, a variation of **± 30 mV** in threshold voltage can happen.

Clearly and concisely answer the following questions with explanation. Write your assumptions, if any. **[30 points]**

a) Determine the threshold voltages of *all the transistors* for *worst case read* operation. **[15 points]**

b) Determine the threshold voltages of *all the transistors* for *worst case write* operation. **[15 points]**



Solution: There will be two ways of providing the answer; both will get full-credit.

First Way:

a) Assume Q = 1 ($\overline{Q}$ = 0) is stored in the cell. We know that for successful read operation, M_1 has to be strong enough compared to M_5 so that the voltage at the node $\overline{Q}$ does not rise high enough to flip the bit in the SRAM cell.

Accordingly, for worst case read operation to happen, the threshold voltages of the MOSs M_1 and M_5 require to change in such a way that **M_1 gets weaker** and **M_5 gets stronger**.

Also, if **M_4 gets weaker** and **M_3 gets stronger**, it will reduce the trip-point voltage of the M_3-M_4 inverter and hence will facilitate the worst case read operation to happen.

If **M_2 gets stronger**, it will try to pull-up the voltage at $\overline{Q}$ that will facilitate the worst case read operation.

Finally, if **M_6 gets weaker**, it will fight less to keep the voltage at node Q to logic 1 which in turn will facilitate flipping of the bit in the cell.

Accordingly,

VT_{M1} = (300 + 30) mv = 330 mv,
VT_{M2} = - (300 - 30) mv = - 270 mv,
VT_{M3} = (300 - 30) mv = 270 mv,
VT_{M4} = - (300 + 30) mv = - 330 mv,
VT_{M5} = (300 - 30) mv = 270 mv,
VT_{M6} = (300 + 30) mv = 330 mv.

Similarly if we assume Q = 0 ($\overline{Q}$ = 1) is stored in the cell, we can determine the threshold voltages of all the transistors for worst case read operation to happen.

b) Assume Q = 1 ($\overline{Q}$ = 0) is stored in the cell. We know that for successful write operation (Q = 0), M_6 has to be strong enough compared to M_4 so that the voltage at the node Q does fall low enough to facilitate the writing Q = 0 in the SRAM cell.

Accordingly, for worst case write operation to happen, the threshold voltages of the MOSs M_4 and M_6 require to change in such a way that **M_4 gets stronger** and **M_6 gets weaker**.

Also, if **M_1 gets stronger** and **M_2 gets weaker** it will reduce the trip-point voltage of the M_1-M_2 inverter and hence will facilitate the worst case write operation to happen.

If **M_3 gets weaker**, it will fight less to bring down the voltage at node Q that would facilitate the worst case write operation to happen.

Finally, if **M_5 gets weaker**, it will fight less to bring up the voltage at node $\overline{Q}$ to logic 1 which in turn will facilitate the worst case write operation to happen.

Accordingly,

VT_{M1} = (300 - 30) mv = 270 mv,
VT_{M2} = - (300 + 30) mv = - 330 mv,
VT_{M3} = (300 + 30) mv = 330 mv,
VT_{M4} = - (300 - 30) mv = - 270 mv,
VT_{M5} = (300 + 30) mv = 330 mv,
VT_{M6} = (300 + 30) mv = 330 mv.

Similarly if we assume Q = 0 ($\overline{Q}$ = 1) is stored in the cell, we can determine the threshold voltages of all the transistors for worst case write operation to happen.

Second Way:

Assumption: For both the cases we have assumed symmetric operation of SRAM cell considering the possibility of reading (or writing) *0* or *1* is same.

a) We know that for successful read operation, M_1 (M_3) has to be strong enough compared to M_5 (M_6) so that the voltage at the node $\overline{Q}$ (Q) does not rise high enough to flip the bit in the SRAM cell.

Accordingly, for worst case read operation to happen, the threshold voltages require to change in such a way that **M_1 (M_3) gets weaker** and **M_5 (M_6) gets stronger**.

Also, if **M_4 (M_2) gets weaker**, it will reduce the trip-point voltage of the M_3-M_4 (M_1-M_2) inverter and hence will facilitate the worst case read operation to happen.

Accordingly,

$VT_{M1} = VT_{M3} = (300 + 30)\ mv = 330\ mv,$
$VT_{M2} = VT_{M4} = -(300 + 30)\ mv = -330\ mv,$
$VT_{M5} = VT_{M6} = (300 - 30)\ mv = 270\ mv.$

b) We know that for successful write operation, M_5 (M_6) has to be strong enough compared to M_2 (M_4) so that the voltage at the node $\overline{Q}$ (Q) does fall sufficiently enough to facilitate the writing of the bit in the SRAM cell.

Accordingly, for worst case write operation to happen, the threshold voltages require to change in such a way that **M_2 (M_4) gets stronger** and **M_5 (M_6) gets weaker**.

Also, if **M_3 (M_1) gets stronger**, it will reduce the trip-point voltage of the M_3-M_4 (M_1-M_2) inverter and hence will facilitate the worst case write operation to happen.

Accordingly,

$VT_{M1} = VT_{M3} = (300 - 30)\ mv = 270\ mv,$
$VT_{M2} = VT_{M4} = -(300 - 30)\ mv = -270\ mv,$
$VT_{M5} = VT_{M6} = (300 + 30)\ mv = 330\ mv.$

Problem 3: Consider a *10-bit* NAND row address decoder with *2-bit pre-decoder* for a memory array. Answer the following questions. Write your assumptions, if any.

[40 points]

a) Design the decoder and draw the corresponding schematic diagram. (You don't need to draw the complete diagram, but draw *enough* so that it's clear.) **[20 points]**

b) Using the *Elmore delay model*, determine the approximate delay improvement compared to the case when the pre-decoder is not used. **[20 points]**

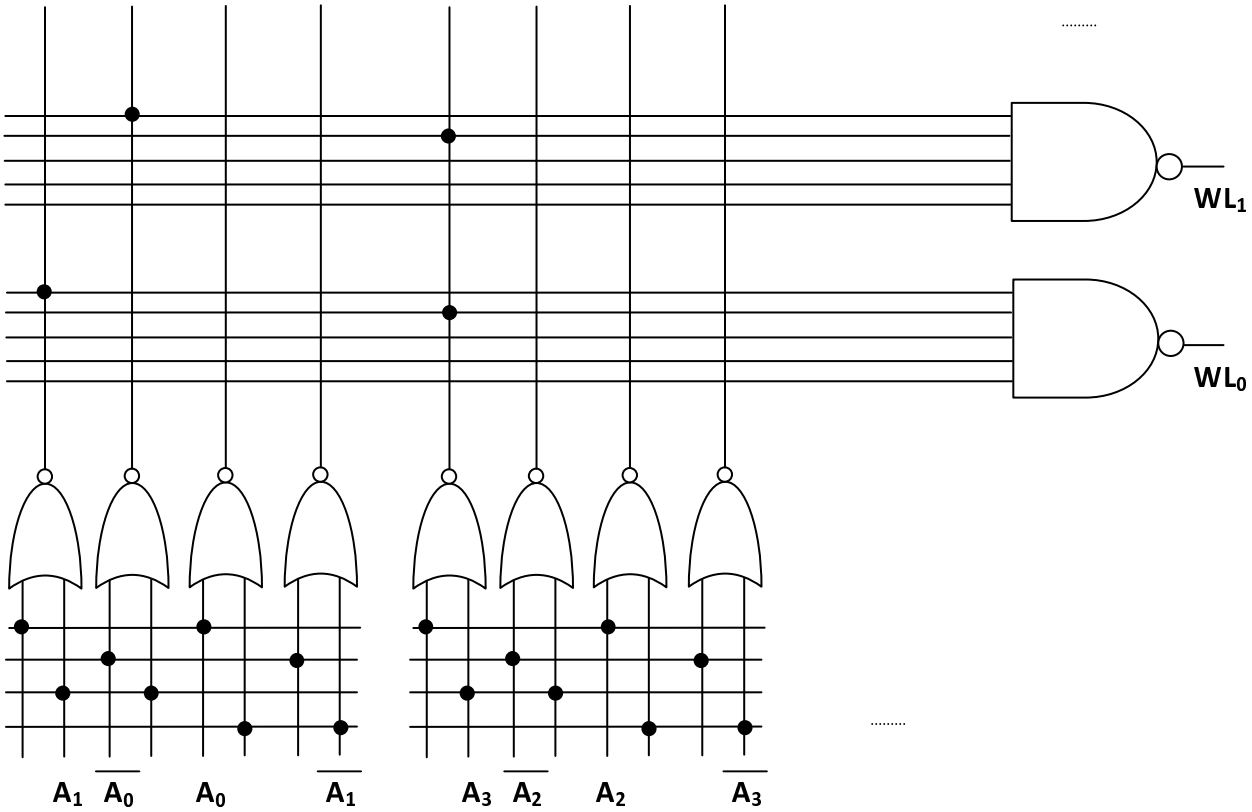
Solution:

a) For the case of an *10-bit* NAND row address decoder with *2-bit pre-decoder*, the expression for WL_0 can be grouped as

$$WL_0 = \overline{\overline{A_0}\ \overline{A_1}\ \overline{A_2}\ \overline{A_3}\ \overline{A_4}\ \overline{A_5}\ \overline{A_6}\ \overline{A_7}\ \overline{A_8}\ \overline{A_9}}$$

$$= \overline{\overline{(A_0 + A_1)}\ \overline{(A_2 + A_3)}\ \overline{(A_4 + A_5)}\ \overline{(A_6 + A_7)}\ \overline{(A_8 + A_9)}} \ .$$

Other terms (WL_1 to WL_{1023}) can be written similarly.



b) Without pre-decoder stage, there will be 10-input NAND gate for each word line. Using Elmore delay model (with NMOS resistance R_N and capacitance C), the approximate maximum propagation delay (output falling delay for NAND gate) would be

$$t_{10\text{-nand}} = R_NC + 2R_NC + \ldots + 10R_NC + (10R_N/n).(10C.p + C_L)$$

where, *n* and *p* are the sizing factor of the NMOS and PMOS transistors, respectively. The sizing factors we can assume as $n = 10$ (since we have a 10-input NAND gate) and $p = 3$ (width of PMOS is set as three times as the width of the NMOS for an invererter). C_L represents the load-capacitance at an word line or a buffer, if introduced.

$$t_{10\text{-nand}} = (10*11/2).R_NC + (10R_N/10).(10C.3 + C_L) = 55R_NC + 30R_NC + R_NC_L = 85R_NC + R_NC_L.$$

Notice the effect of considering the capacitances due to PMOS transistors in the 10-input NAND gate.

With a 2-bit pre-decoder, using Elmore delay model, the approximate maximum propagation delay would be

$$\begin{aligned} t_{\text{pre-decoder}} &= t_{2\text{-nor}} + t_{5\text{-nand}} \\ &= [R_PC + 2R_PC + (2R_P/6).(2C.1)] + [R_NC + 2R_NC + \ldots + 5R_NC + (5R_N.5).(5C.3 + C_L)\ ] \\ &= 3.66(3.R_N)C + (15R_NC + 15R_NC) + R_NC_L \qquad (R_P \approx 3R_N) \\ &= 41R_NC + R_NC_L. \end{aligned}$$

Note that in the 2-input NOR gates we have assumed the sizing of the PMOS transistors as 6 times the sizing of the NMOS transistors to accord to the similar assumption made previously. Also notice that we have not quite considered the load capacitance at the output of the each NOR gate at the pre-decoder stage represented by the input capacitances of the connected transistors in the NAND gates at the final decoder stage.

$$\begin{aligned} \text{So, the approximate delay improvement would be} \quad &= (85R_NC + RC_L) - (41R_NC + R_NC_L) \\ &= 44R_NC. \end{aligned}$$

Considering that the output of the NAND gates at the final decoder stage is buffered, we can ignore C_L. Hence, the approximate percentage delay improvement would be 44/85 = 51.76%.