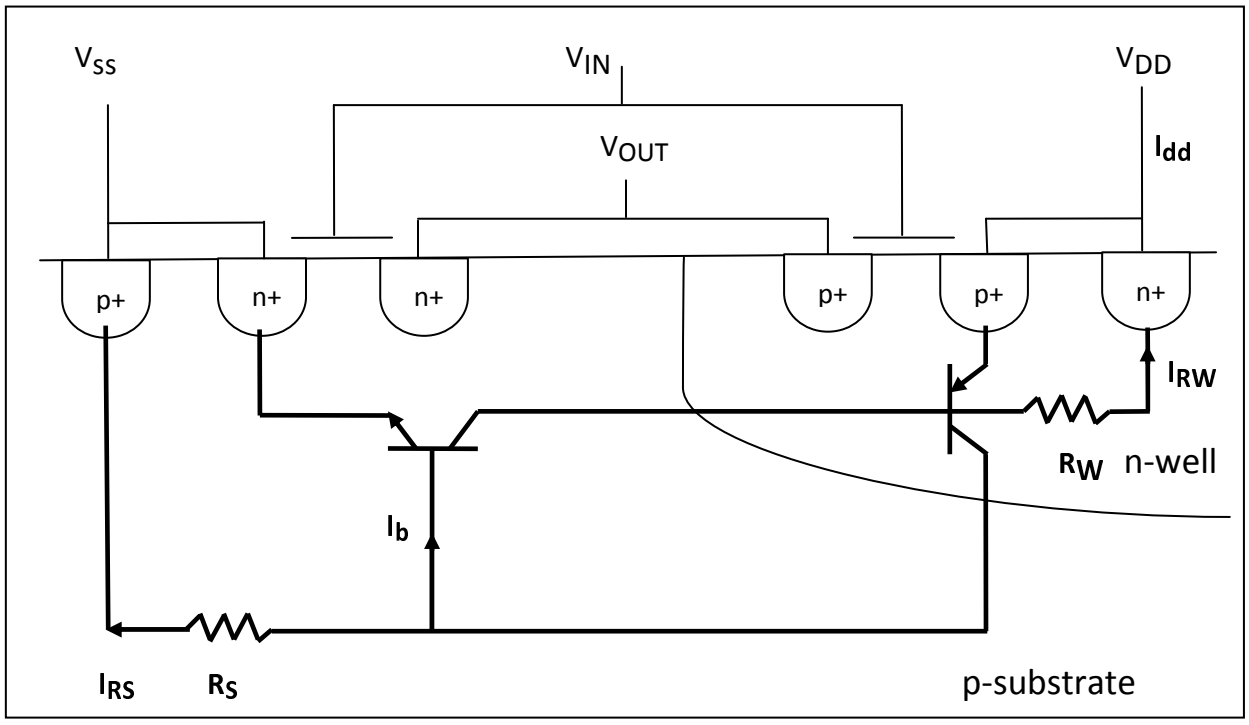
Homework 1

ECE 559: MOS VLSI Design (Fall 2009)

ECE Department, Purdue University

Assigned: 17-Sep-2009 Due: 24-Sep-2009

Problem 1 (Latchup): The schematic and equivalent circuit of parasitic resistors and bipolar transistors in a CMOS is shown below. Here, the latchup is triggered at the point when the *npn*-transistor is turned on, i.e., the voltage drop across the resistor R_s is larger than the turn-on voltage of *npn*-transistor.



From this condition, derive the following inequality for the triggering of the latchup

$$\beta_{npn}\beta_{pnp} > 1 + \frac{\left(\beta_{npn}+1\right)\left(I_{RS}+I_{RW}\beta_{pnp}\right)}{\left(I_{dd}-I_{RS}\right)}.$$

Where β_{pnp} and β_{npn} are the common-emitter current gains for the *pnp* and *npn* transistors, respectively.

Problem 2 (CMOS Limits): Prove that the minimum V_{DD} for CMOS circuit operation is

$$V_{DD}\,|_{\min} = 2\ln(2)\frac{KT}{q}.$$

Problem 3 (Pseduo-NMOS): Consider a pseudo-NMOS 2-input NAND gate as in the figure below. Use the following

$V_{DD} = 1$ V

$K_p' = \mu_p C_{ox} = 30\text{e-}6$ A/V^2 $K_n' = \mu_n C_{ox} = 60\text{e-}6$ A/V^2

$V_{tp} = -0.3$ V $V_{tn} = 0.3$ V.

Assume there is no sub threshold current, no body effect, and every transistor has ideal long-channel characteristics.

Determine the output voltage (V_{out}) when the input voltage is i) 0 V ii) 0.2 V iii) 0.3 V iv) 0.4 V v) 0.7 V vi) 1 V.