Homework 3

ECE 559: MOS VLSI Design (Fall 2009)

ECE Department, Purdue University

Assigned: 06-Oct-2009 Due: 15-Oct-2009

Important: Please turn-in all of your codes along with the waveforms (when necessary) during submission of your solution. You may be asked to provide the soft copy of your codes by email if such need arises.

Problem 1: For a gate if we increase the widths of the transistors, the corresponding propagation delays get decreased first but if you continue to increase the widths, you will find that the propagation delays get increased eventually.

Part a) Explain why does it happen.

Perform SPICE simulations for a simple CMOS inverter with the libraries that you have used in lab, i.e., *tsmc25N* and *tsmc25P* to confirm your answer. Use L = 300 nm, V_{DD} = 2.5 V.

Part b) A gate has *rising* and *falling* propagation delays. Also a gate with more than one input can have different rising and falling propagation delays depending on different input vector combinations applied to the inputs of the gate. Consider a 2-input NAND gate. Explain for which input combinations, the *maximum rising* and the *maximum falling* delays occur.

Perform SPICE simulation with the libraries that you have used in lab, i.e., *tsmc25N* and *tsmc25P* to confirm your answer. Use L = 300 nm, V_{DD} = 2.5 V.

Part c) Find out the *optimum widths of the transistors* so that the *maximum input-to-output propagation delay for a 2-input NAND gate* is *minimized*. Clearly explain the procedure you have followed. Submit the necessary plots showing the trade-off between propagation delays and transistor widths.

Problem 2: Draw a layout of a 2-input NAND gate with the optimized widths that you have got for the problem 1. You can round the widths of the transistors as allowed by the technology library that you have used in lab. Perform DRC, extract layout, do layout vs. schematic check, and at last simulate your extracted netlist to verify its functionality. Submit the plots of schematic and layout of your design.

Problem 3: In the circuit given below, the input voltage, V_{in} varies as shown. Determine the energy dissipation when 1) RC >> T and 2) T >> RC, respectively.