Homework 6

ECE 559: MOS VLSI Design (Fall 2009)

ECE Department, Purdue University

Assigned: 18-Nov-2009 Due: 24-Nov-2009

Important: Please turn-in all of your codes along with the waveforms (when necessary) during submission of your solution. You may be asked to provide the soft copy of your codes by email if such need arises.

Problem 1: Consider a standard 6-T SRAM cell. Use the following parameters.

L = 300 nm, V_{DD} = 2.5 V.

For all the NMOS transistors, allowed *minimum* and *maximum* widths are 450 nm and 1800 nm, respectively. Always size the pull-up PMOS transistors as three-times the widths of the pull-down NMOS transistors. You should consider widths in *50 nm* intervals.

Write your assumptions with clear and concise explanation for all the parts below.

Part a) Determine by hand calculation

i) *Cell ratio* (ratio of the widths of pull-down NMOS and access transistor) for read
ii) *Pull-up ratio* (ratio of the widths of pull-up PMOS and access transistor) for write

Write the regions of operation of all the transistors for both i) and ii).

Any extra parameter that you might need, you should *extract* from the SPICE library that you are using.

Part b) Size the transistors in the SRAM cell to have the *maximum read stability*. By SPICE simulation, determine the *static noise margin* (SNM) of the SRAM cell. (SNM is defined as the minimum noise voltage present at each of the cell storage nodes necessary to flip the state of the cell.) Explain the procedure you have followed.

Part c) What happens to the write operation for the cell? If write operation fails, size the transistors in such a way that it's at the verge of satisfying the write operation. By SPICE simulation, determine the *static noise margin* (SNM) of the SRAM cell. Explain the procedure you have followed.

Compare SNM for this part with that of part b). Explain if the result is according to your expectation or not.