Combinational Logic Gates in CMOS

References:

Adapted from: *Digital Integrated Circuits: A Design Perspective*, J. Rabaey, Prentice Hall © UCB

Principles of CMOS VLSI Design: A Systems Perspective, N. H. E. Weste, K. Eshraghian, Addison Wesley

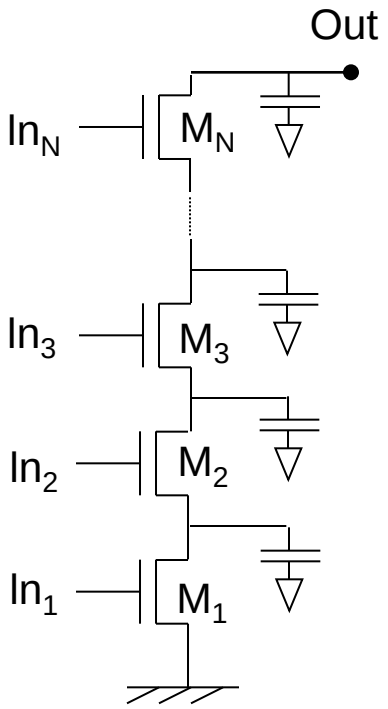
Adapted from: EE216A Lecture Notes by Prof. K. Bult © UCLA

Design Techniques for Large Fan-In

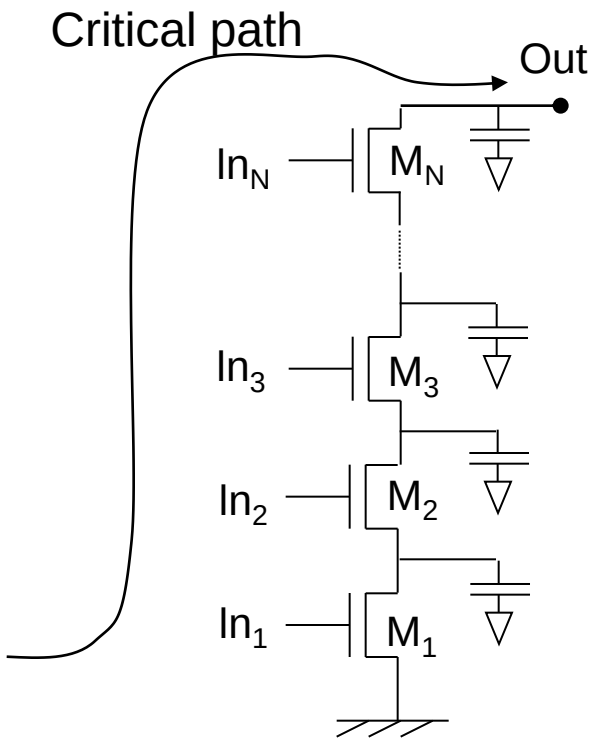
- Transistor Sizing
- Progressive Transistor Sizing
- Transistor Ordering
- Logic Design to reduce the gate fan-in

Progressive Sizing

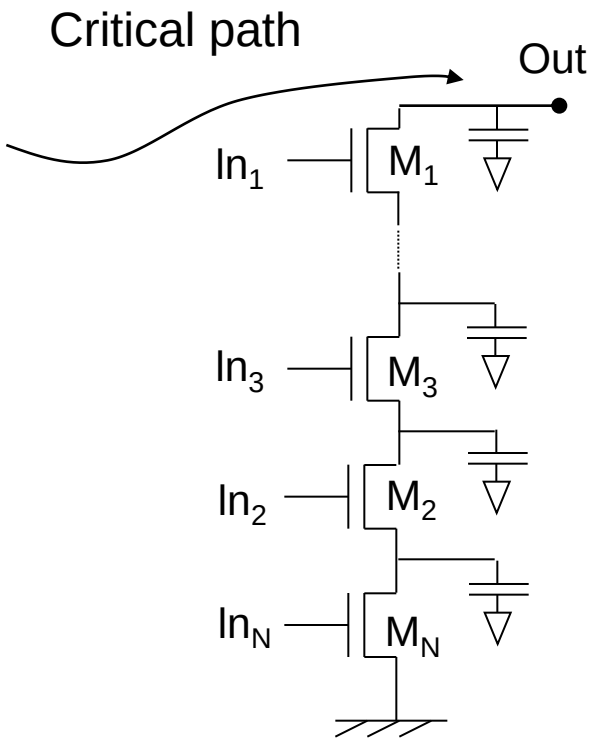
- When parasitic capacitance is significant (e.g., when fan-in is large), needs to consider distributed RC effect
- Increasing the size of M1 has the largest impact in terms of delay reduction
- $M_1 > M_2 > M_3 > \ldots > M_N$



Delay Optimization by Transistor Ordering

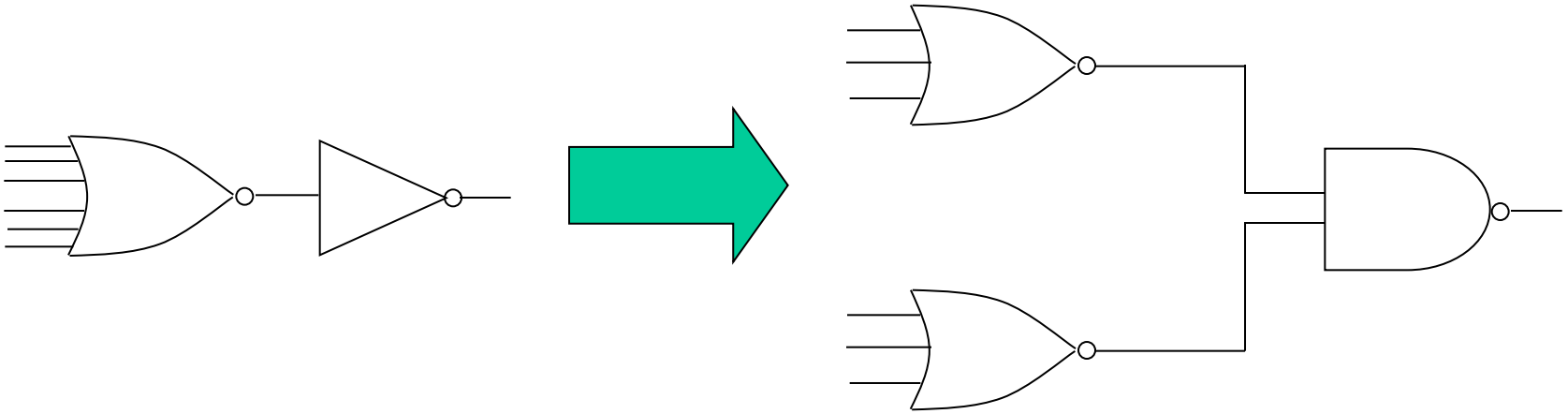


Critical signal next to supply



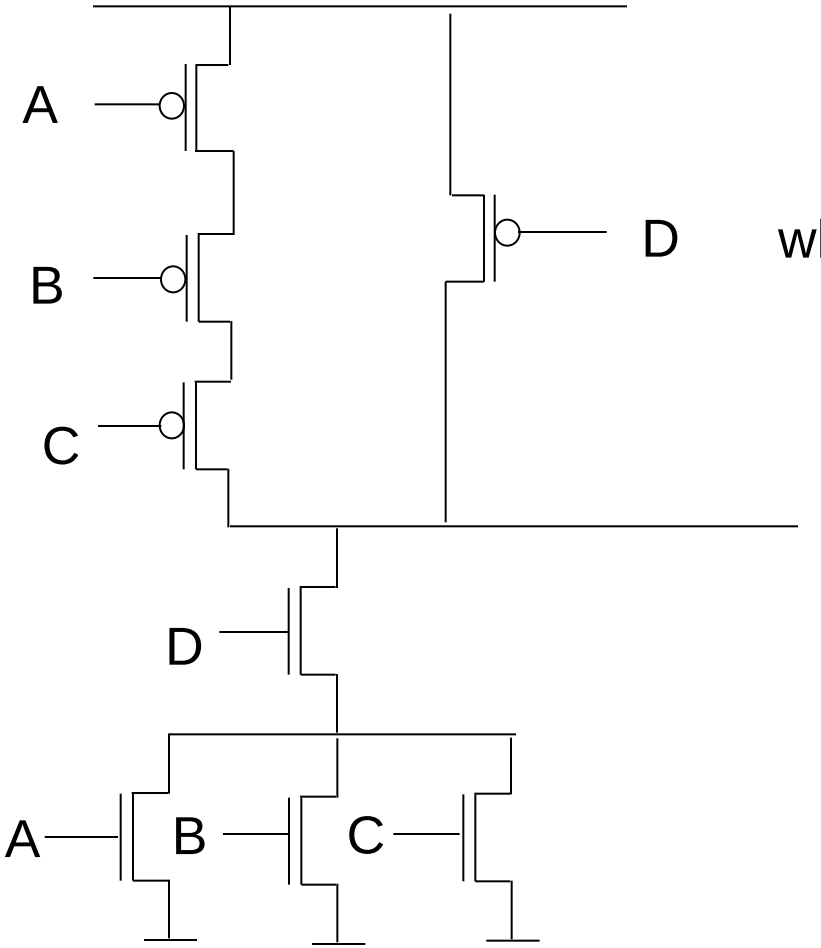
Critical signal next to output

Improved Logic Design



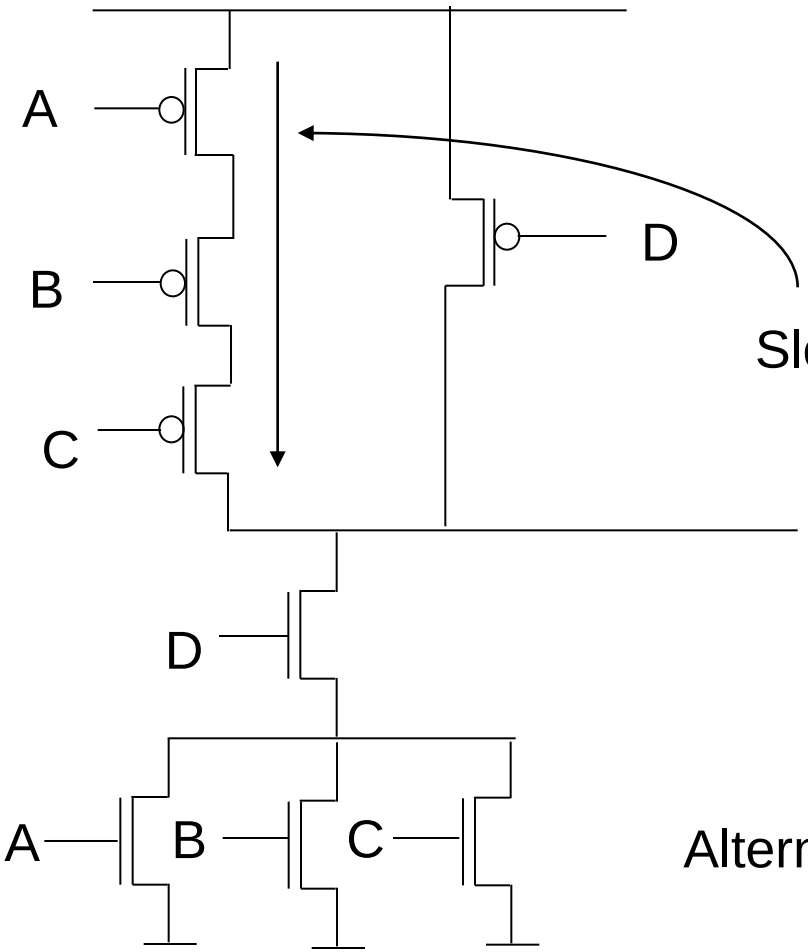
Reduce the fan-in to each gate

Example: $F = \overline{((A + B + C).D)}$



which path is the slowest ?

Example: $F = \overline{((A+B+C).D)}$



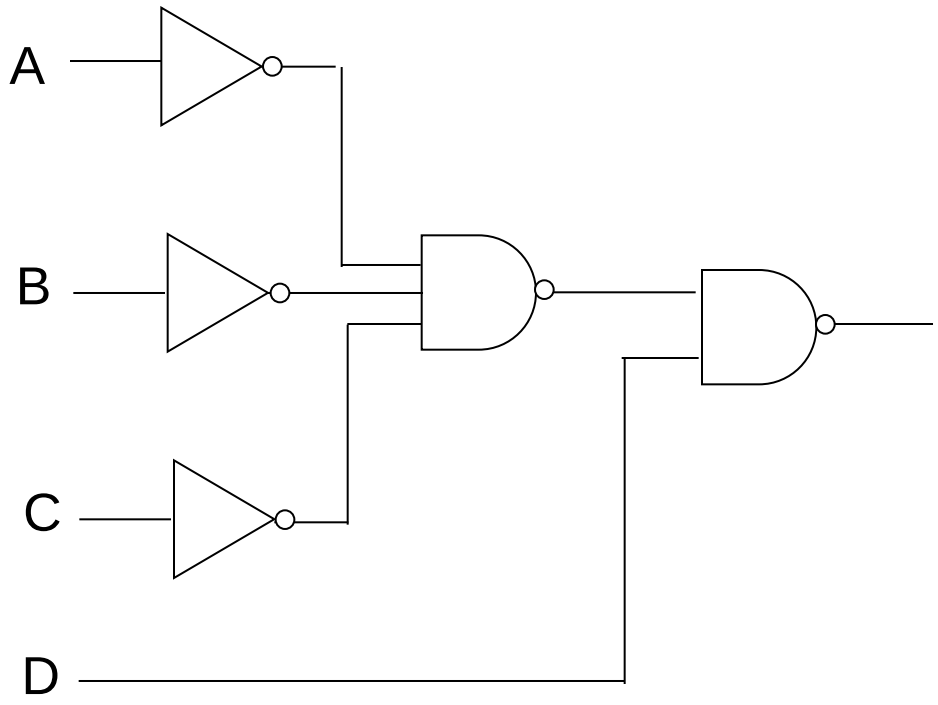
Slowest path

Alternatives ?

If minimum-size: $t_{dr} \approx 6 \times t_{df,inv}$

$t_{df,inv}$ = delay of a minimum inverter

Example: $F = \overline{((A+B+C).D)}$

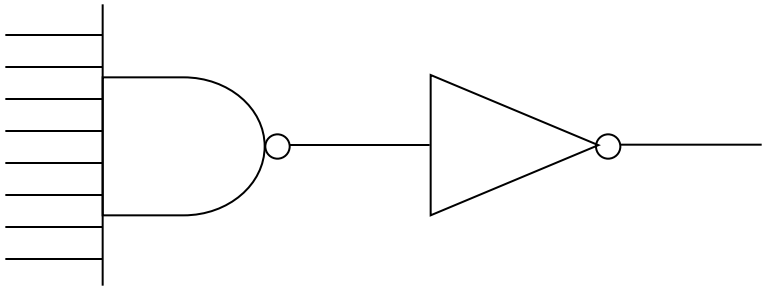


If minimum-size: $t_{dr} \approx 7 \times t_{df.inv}$

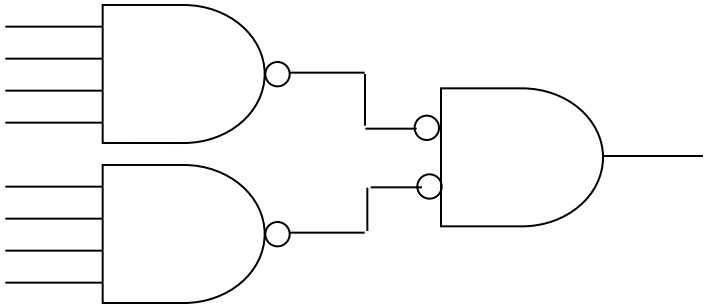
⟶ this approach is advantageous if driving larger load

Design of an 8-Input AND

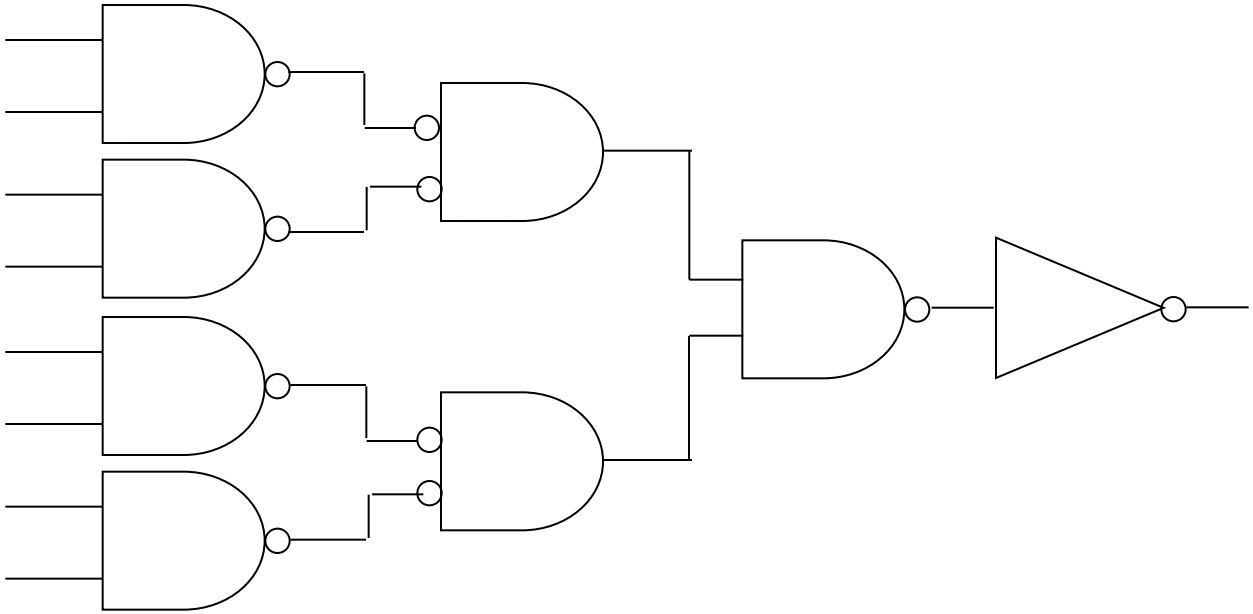
Approach 1



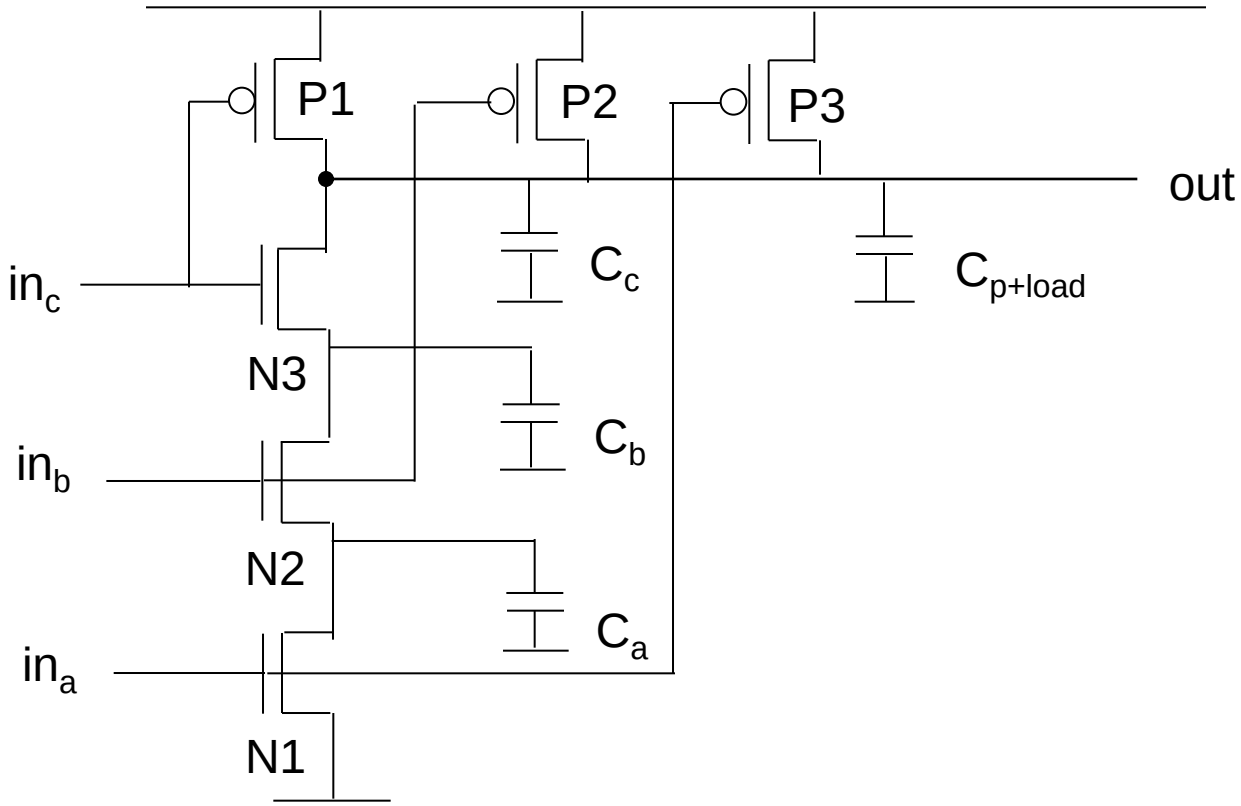
Approach 2



Approach 3



3-input NAND Gate with Parasitic Capacitors



Macro Modeling for Worst Case Analysis

$$t_{df} = [R_{N1}C_a] + [(R_{N1}+R_{N2})C_b] + [(R_{N1} + R_{N2} + R_{N3})C_c] + [(R_{N1} + R_{N2} + R_{N3})C_p] + [(R_{N1} + R_{N2} + R_{N3})C_{load}]$$

Internal delay

External load

$$t_d = T_{d,\ internal} + \lambda \times C_{load}$$

Macro Modeling

$$t_{df} = \frac{m^2 + m}{2} R_N C_j + \frac{mR_N}{n}(mpC_j + C_L)$$

m: fan-in
n: sizing factor of NMOS transistors
p: sizing factor of PMOS transistors

$C_{inv,min}$ = total gate capacitance of minimum size inverter
k = "fan-out" corresponding to C_L
$C_j = r\, C_{inv,min}$

$$t_{df} = R_N \left(\frac{(m^2 + m)C_j}{2} + \frac{m^2 pC_j}{n} + \frac{mkC_{inv,\min}}{n} \right)$$

Keep m^2 and m^2p/n and mk/n reasonable

Macro Modeling for NOR Gate

$$t_{dr,NOR} = R_P \left(\frac{(m^2 + m)C_j}{2} + \frac{m^2 nC_j}{p} + \frac{mkC_{inv,\min}}{p} \right)$$

Keep m^2 and m^2n/p and mk/p reasonable

$$t_{df,NOR} = R_N \left(mC_j + \frac{mpC_j}{n} + \frac{kC_{inv,\min}}{n} \right)$$

Keep n as small as possible to minimize the impact on rise-delay

Design Strategy

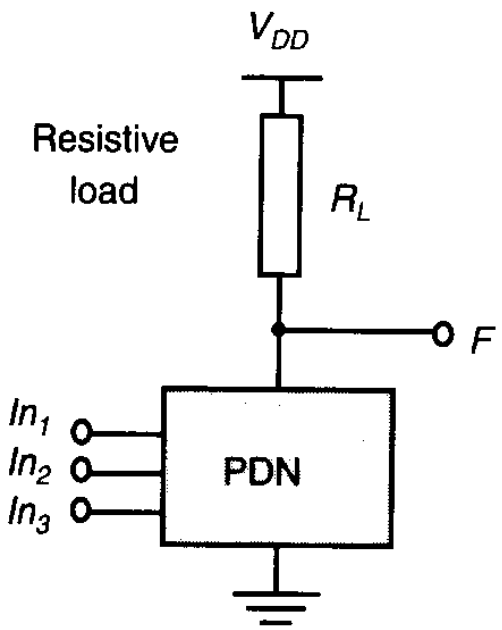
- Use minimum sized transistors
- Analyze critical path (slowest, maybe more than 1)
- Look at alternative implementations (substitute NOR’s ?)
- Compare and choose best
- Analyze critical path(s) and optimize transistor sizing

Complementary Logic

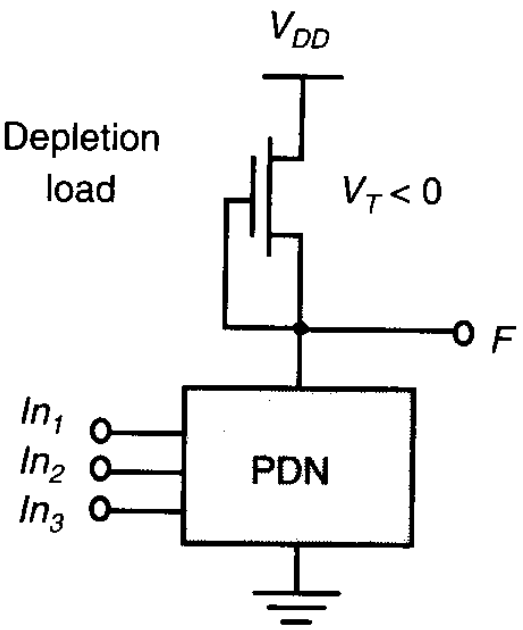
- 2n transistors
- Complicated wiring
- No functional sizing required

Ratioed Logic

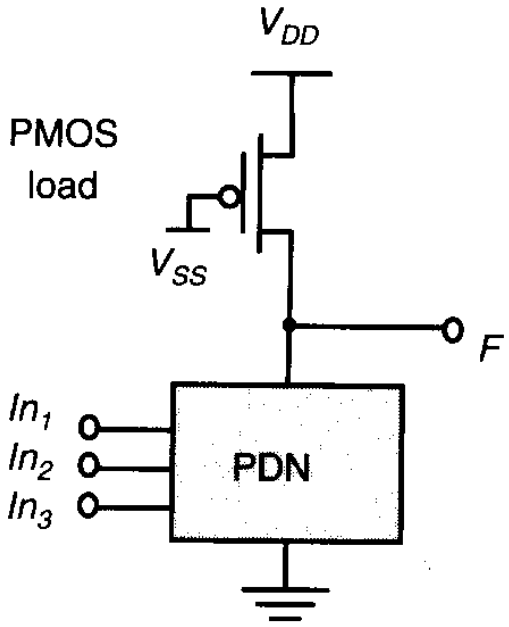
Ratioed Logic



(a) Resistive load



(b) Depletion load NMOS



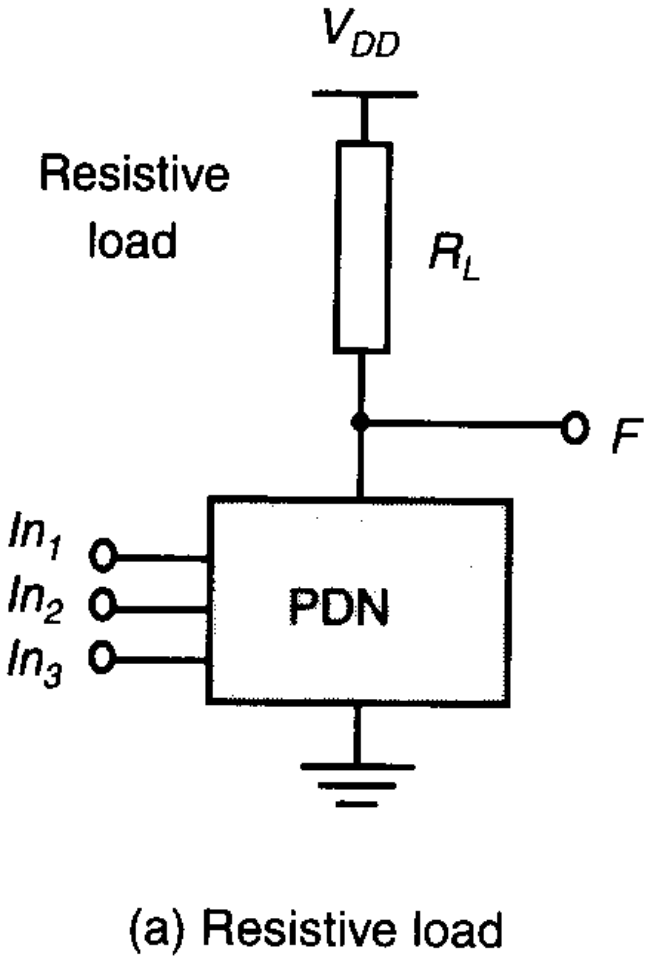
(c) Pseudo-NMOS

Reduce the number of devices over complementary logic

Ratioed Logic

- Use PDN to implement the function (which is the negation of the network)
- Total number of devices: n for the input, 1 for the static load
- Minimum load is 1 unit-gate load
- Functional sizing is required to optimize noise margin

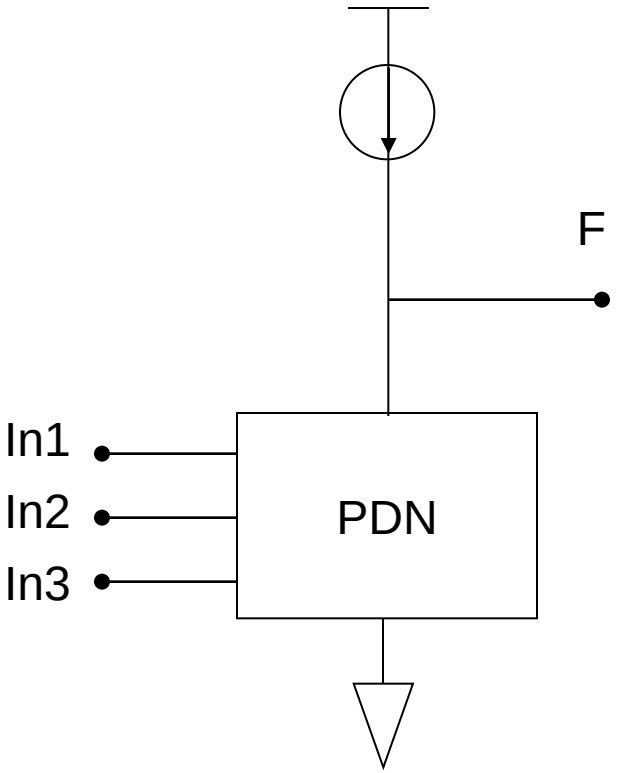
Functional Sizing in Ratioed Logic



(a) Resistive load

- N transistors
- $V_{OH} = V_{DD}$
- $$V_{OL} = \frac{R_{PDN}}{R_{PDN} + R_L} V_{DD}$$
- Asymmetrical response
- Static power consumption
- $t_{pLH} = 0.69\, R_L C_L$
- $t_{pHL} = 0.69\, (R_L \,||\, R_{PDN})\, C_L$

Current Source as the Static Load



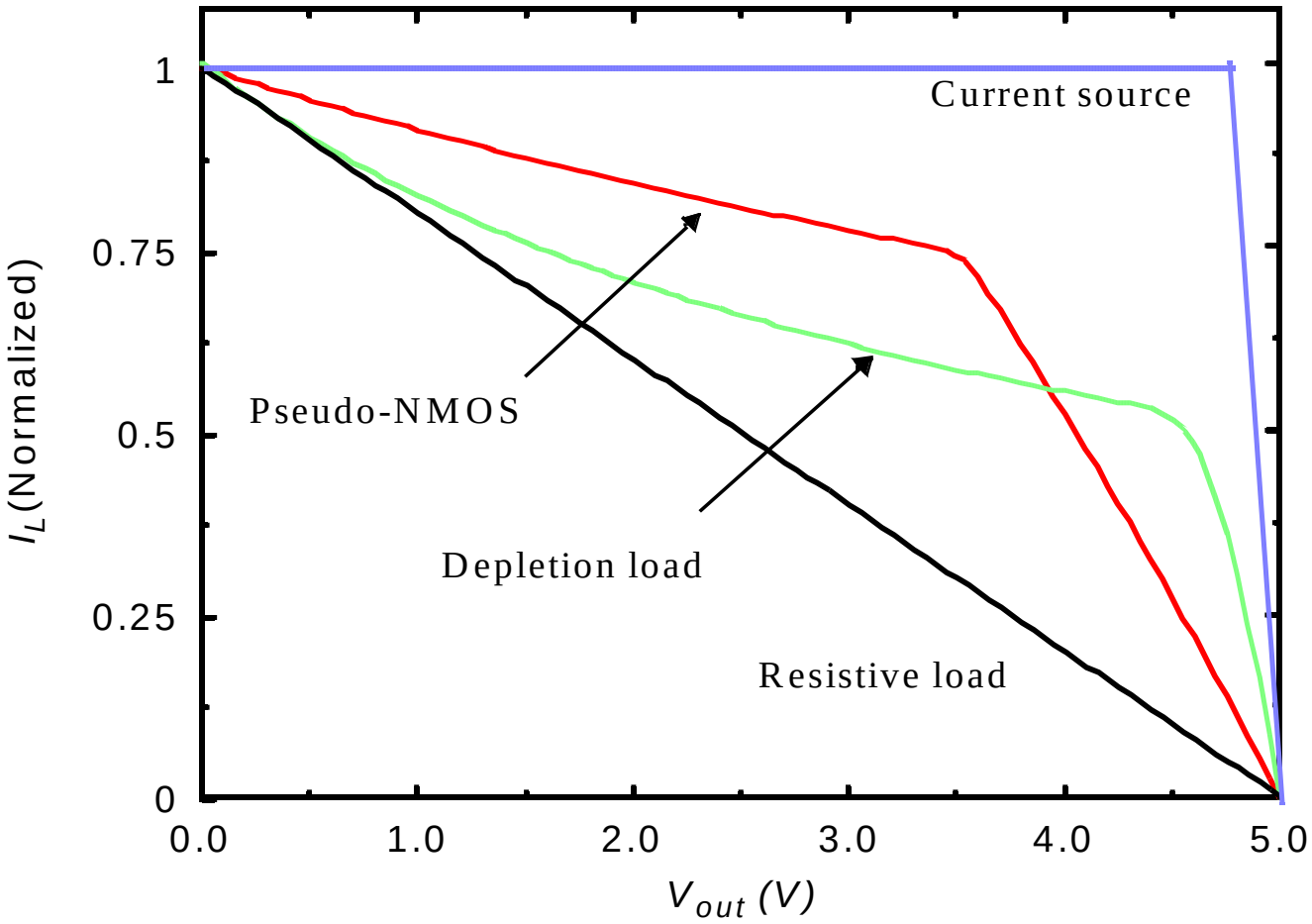
$$t_{pLH} = \frac{C_L V_{swing} / 2}{I_{ave}}$$

- If current source equals V_{DD}/R_L = initial charging current from the resistive load

$$t_{pLH} = \frac{C_L R_L}{2}$$

- More than 25% reduction compared to resistive load

Load Lines of Ratioed Gates



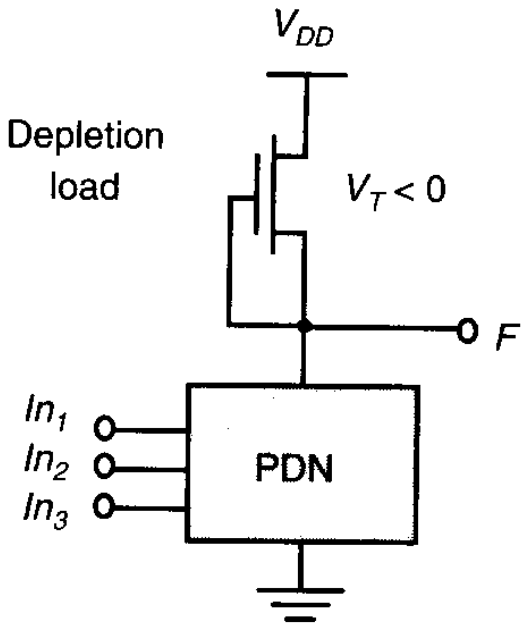
NMOS Depletion Load

Use depletion mode NMOS transistor as pull-up

V_{tdep} of depletion transistor is < 0 V

The depletion mode transistor is always ON:
gate and source connected $\Rightarrow V_{gs} = 0$

$V_{in} = 0 \Rightarrow$ transistor pull down is off $\Rightarrow V_{out}$ is high



(b) Depletion load NMOS

Voltage Output Low

Driver is in linear region with input high
Load is in saturation region

$$\beta_{driver}\left((V_{DD}-V_{tn})V_{OL}-\frac{V_{OL}^{2}}{2}\right)=\frac{\beta_{load}}{2}(-V_{tdep})^{2}$$

Assume: $V_{DD} = 5.0V$
$V_{tn} = 1.0V = - V_{tdep}$

Proper design: $V_{ol} < V_{tn}$

Let: $V_{ol} = 0.5V$

$$\frac{\beta_{driver}}{\beta_{load}} = 0.267$$

Gate Threshold Voltage

Gate threshold voltage = V_{inv}

= Input voltage at which $V_{in} = V_{out}$

Assume that both driver and load are in saturation with input V_{inv}

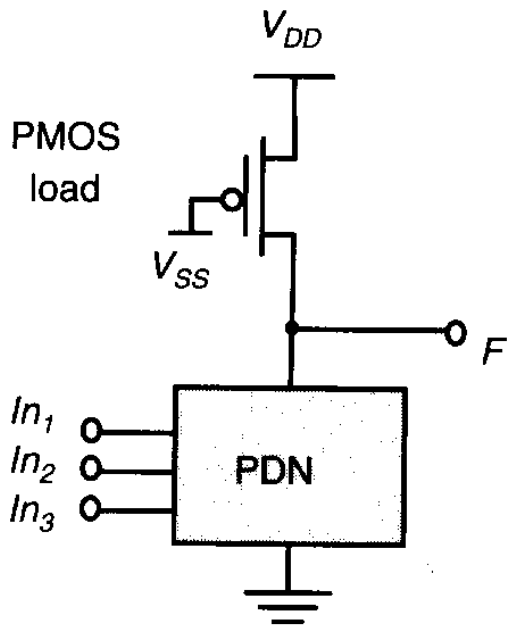
$$I_{DS\,(sat)} = \frac{\beta_{driver}}{2}(V_{gs} - V_t)^2$$

$$\therefore \frac{\beta_{driver}}{2}(V_{inv} - V_t)^2 = \frac{\beta_{load}}{2}(-V_{dep})^2$$

Hence, $$V_{inv} = V_t - V_{dep}\sqrt{\frac{\beta_{load}}{\beta_{driver}}}$$

If β_{driver} is increased relative to β_{load} then, V_{inv} decreases

PMOST Load with Constant V_{GS}



(c) Pseudo-NMOS

$V_{oh} = 5.0V$

$V_{ol} = ???$

$I = 0.5\beta_p.(V_{dd}-V_{tp})^2$

$I = \beta_n.((V_{dd}-V_{tn})V_{ol}-0.5V_{ol}^2)$

$$\frac{\beta_n}{\beta_p} = \frac{0.5(V_{dd} - V_{tp})^2}{((V_{dd} - V_{tn})V_{ol} - 0.5V_{ol}^2)}$$

Sizing for V_{OL}

$$\frac{\beta_n}{\beta_p} = \frac{0.5(V_{dd} - V_{tp})^2}{((V_{dd} - V_{tn})V_{ol} - 0.5V_{ol}^2)}$$

Assume: $V_{dd} = 5.0V$
$V_{tn} = V_{tp} = 1.0V$

Proper design: $V_{ol} < V_{th}$

Let: $V_{ol} = 0.5V$

$$\frac{\beta_n}{\beta_p} = 4.26$$

Sizing for Gate Threshold Voltage

N-device: saturated $(V_{out} > V_{in} - V_{tn})$

$$I_{dsn} = \frac{\beta_n}{2}(V_{in} - V_{tn})^2$$

P-device: non-saturated

$$V_{gsp} = -V_{DD}$$

$$I_{dsp} = \beta_p[(-V_{DD} - V_{tp})(V_{out} - V_{DD}) - \frac{(V_{out} - V_{DD})^2}{2}]$$

Equating the two currents we obtain,

$$\frac{\beta_n}{2}(V_{in} - V_{tn})^2 = -\beta_p[(-V_{DD} - V_{tp})(V_{out} - V_{DD}) - \frac{(V_{out} - V_{DD})^2}{2}]$$

Sizing for Gate Threshold Voltage

Solving for V_{out}

$$V_{out} = -V_{tp} + \sqrt{(V_{DD} + V_{tp})^2 - C}$$

Where $C = k (V_{in} - V_{tn})^2$

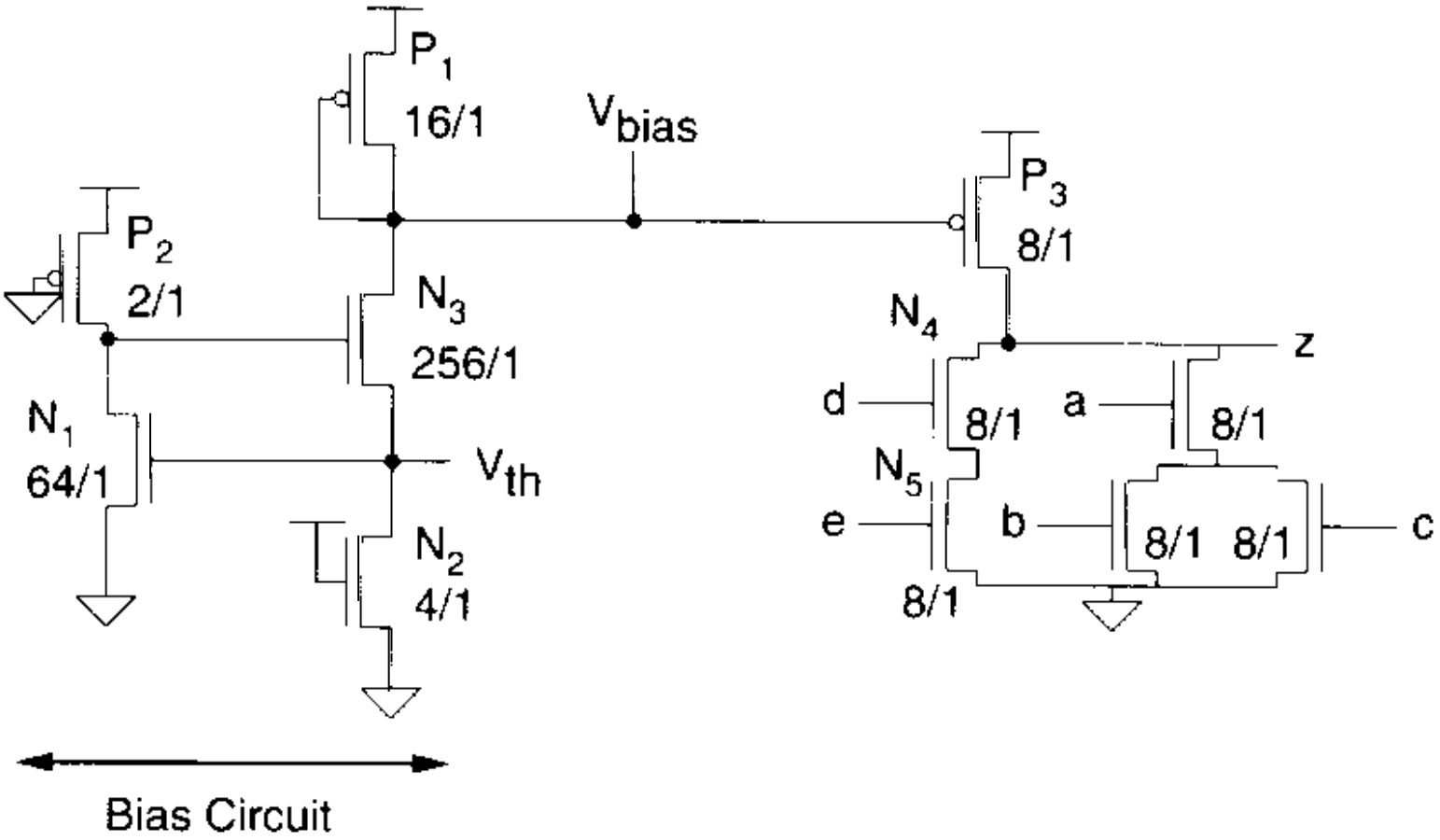
$$k = \frac{\beta_n}{\beta_p}$$

Also, $$\frac{\beta_n}{\beta_p} = \frac{(V_{DD} + V_{tp})^2 - (V_{out} + V_{tp})^2}{(V_{in} - V_{tn})^2}$$

To make gate threshold voltage = $0.5V_{DD}$

$$\frac{\beta_n}{\beta_p} = 6.11$$

Forcing the Voltage Output Low



Propagation Delay of Pseudo-NMOS Inverter

- Use average current

$$I_{av}(L \rightarrow H) = \frac{1}{2}\left[\frac{\beta_P}{2}(-V_{DD} - V_{tp})^2 + \beta_P(-V_{DD} - V_{tp})(\frac{-V_{DD}}{2}) - (\frac{V_{DD}^2}{8})\right]$$

$$I_{av}(H \rightarrow L) = \frac{1}{2}\left[\frac{\beta_N}{2}(V_{DD} - V_{tn})^2 + \beta_N(V_{DD} - V_{tn}) - \beta_P(V_{DD} + V_{tn})\frac{-V_{DD}}{2} + (\beta_N - \beta_P)\frac{V_{DD}^2}{8}\right]$$

- Propagation delay

$$t_p = \frac{C_L(V_{DD}/2)}{I_{av}}$$

Power Consumption

- Consume power when the output is low

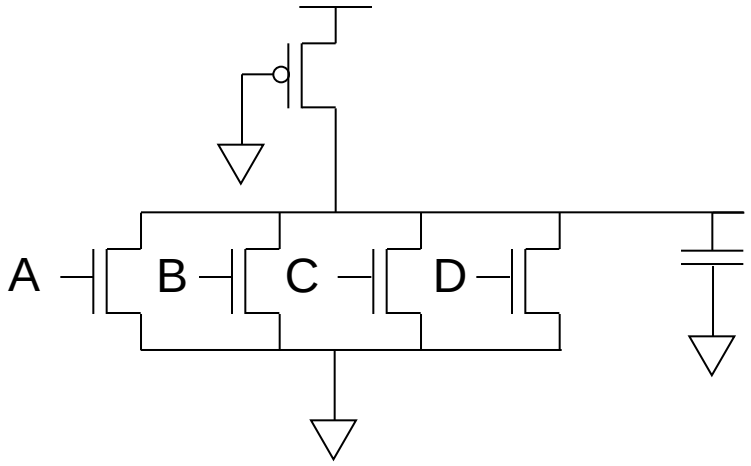
$$I_{av,low} = \frac{\beta_P}{2}(-V_{DD} - V_{tp})^2$$

$$P_{av,low} = V_{DD} I_{av,low} = \frac{\beta_P}{2} V_{DD} (V_{DD} + V_{tp})^2$$

Trade-offs to be Considered

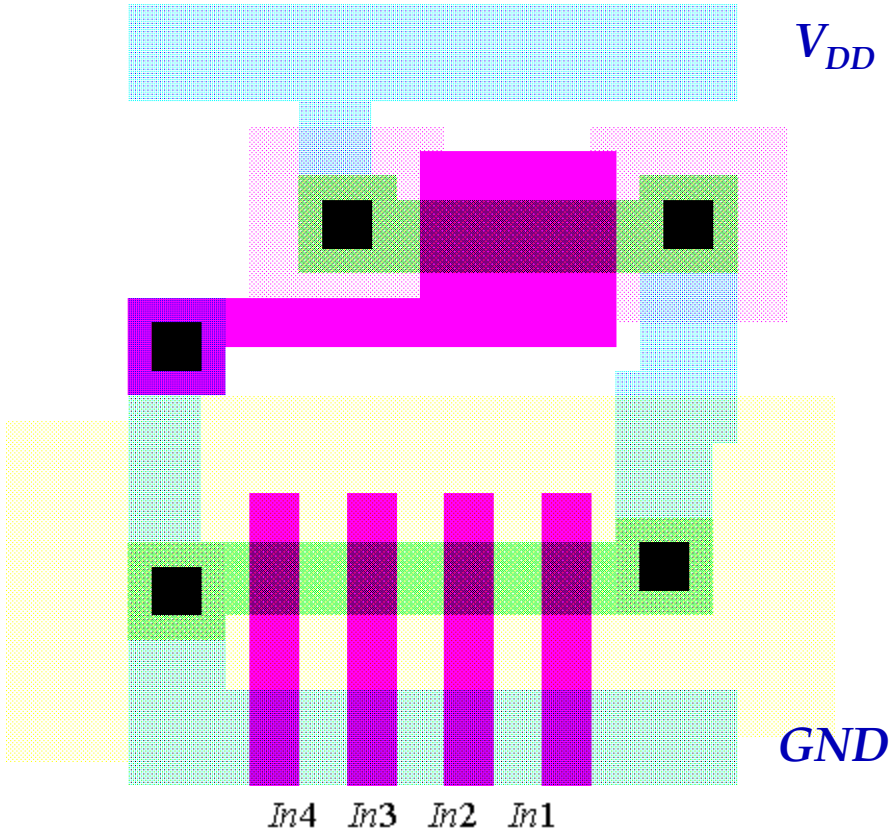
- To reduce static power, I_{Load} should be low
- To obtain a reasonable NM_L, $V_{OL} = I_{Load}R_{PDN}$ should be low
- To reduce $t_{pLH} \approx C_L V_{DD}/(2I_{Load})$, I_{Load} should be high
- To reduce $t_{pHL} \approx 0.69\ R_{PDN}C_L$, R_{PDN} should be kept small

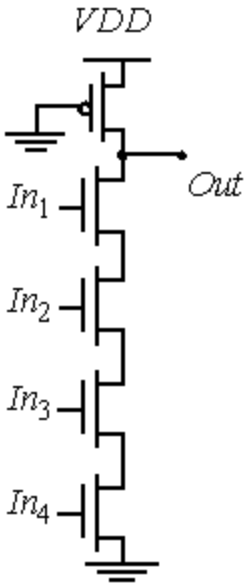
Pseudo-NMOS NOR Gate



- Fan-in of N inputs requires only N+1 transistors, smaller parasitic capacitance and area
- Smaller load to preceding gate
- Static power consumption at output low
- Pseudo-NMOS gates can be used effectively when speed is importance and majority of the output is high

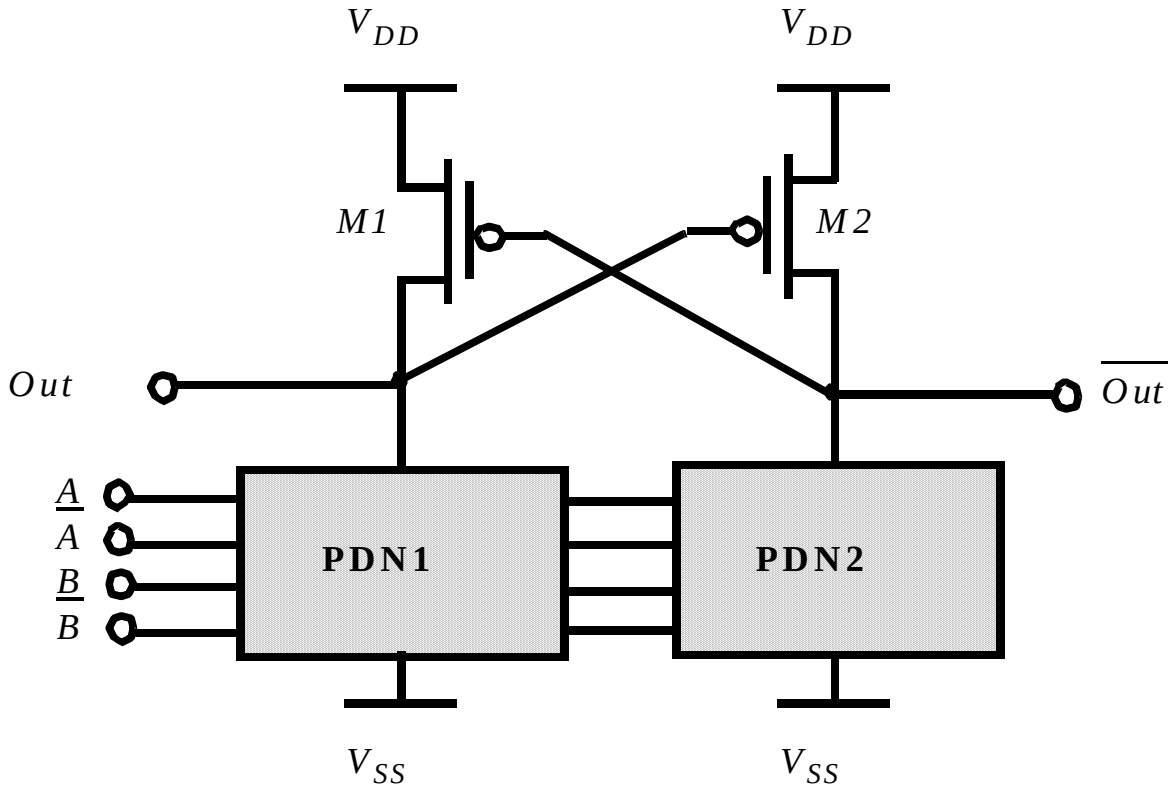
Pseudo-NMOS NAND Gate





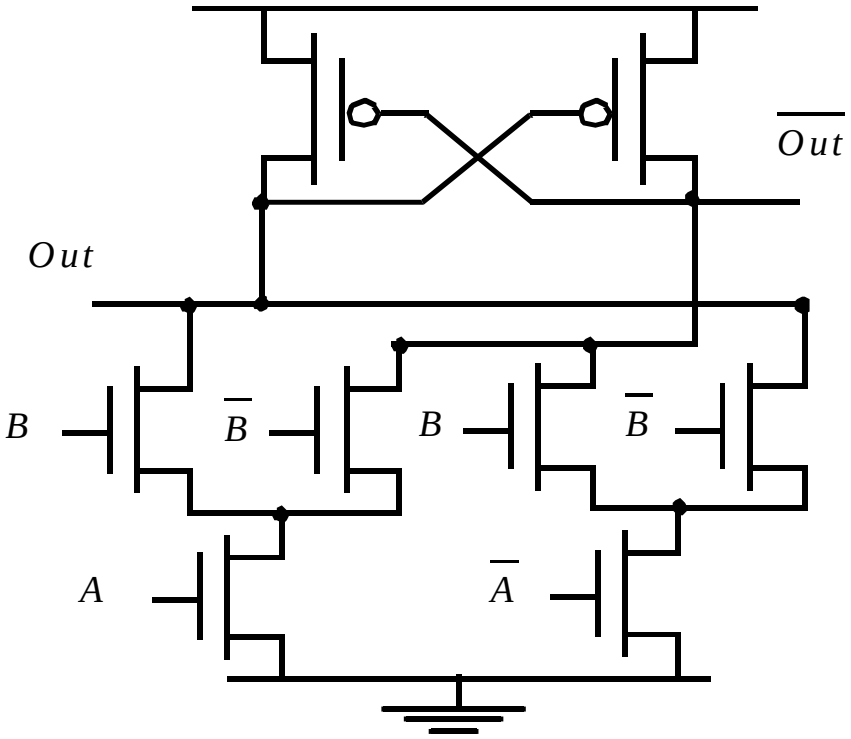
$$C_{L,pseudo} = 0.5\ C_{L,CMOS}\ \text{(Fan-out of 1)}$$

Improved Loads (2)



Dual Cascode Voltage Switch Logic (DCVSL)

Example



XOR-NXOR gate