Combinational Logic Gates in CMOS

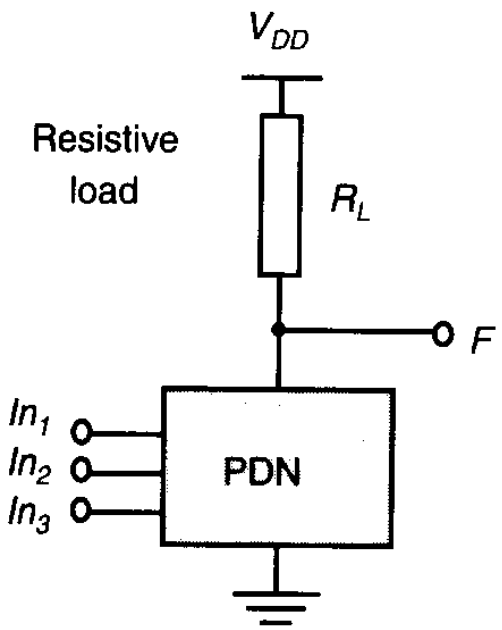
References:

Adapted from: *Digital Integrated Circuits: A Design Perspective*, J. Rabaey, Prentice Hall © UCB

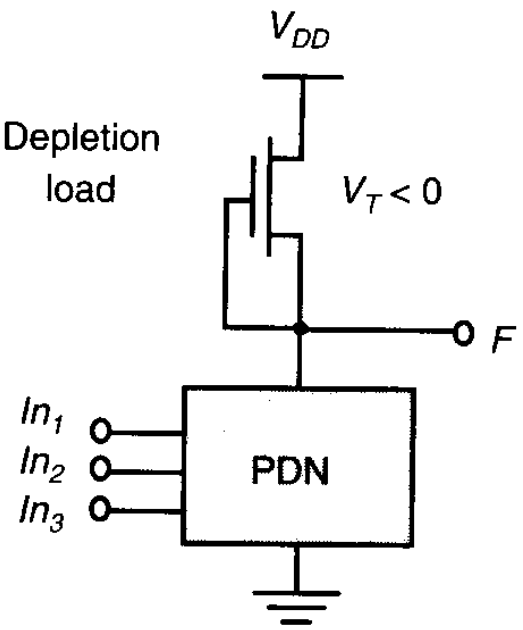
Principles of CMOS VLSI Design: A Systems Perspective, N. H. E. Weste, K. Eshraghian, Addison Wesley

Adapted from: EE216A Lecture Notes by Prof. K. Bult © UCLA

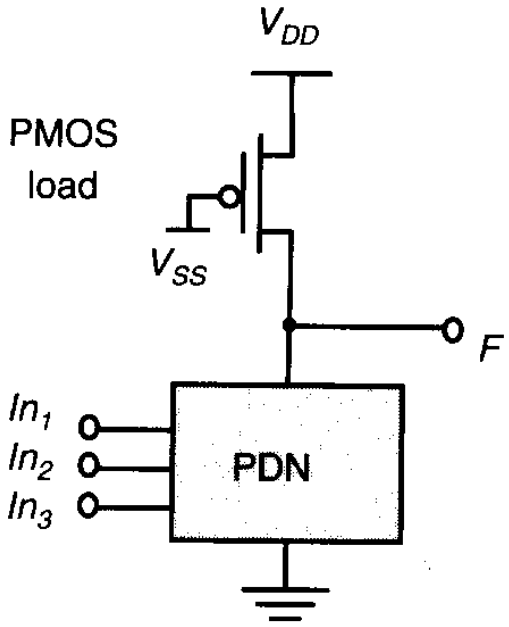
Ratioed Logic



(a) Resistive load



(b) Depletion load NMOS



(c) Pseudo-NMOS

Reduce the number of devices over complementary logic

Ratioed Logic

- Use PDN to implement the function (which is the negation of the network)
- Total number of devices: n for the input, 1 for the static load
- Minimum load is 1 unit-gate load
- Functional sizing is required to optimize noise margin

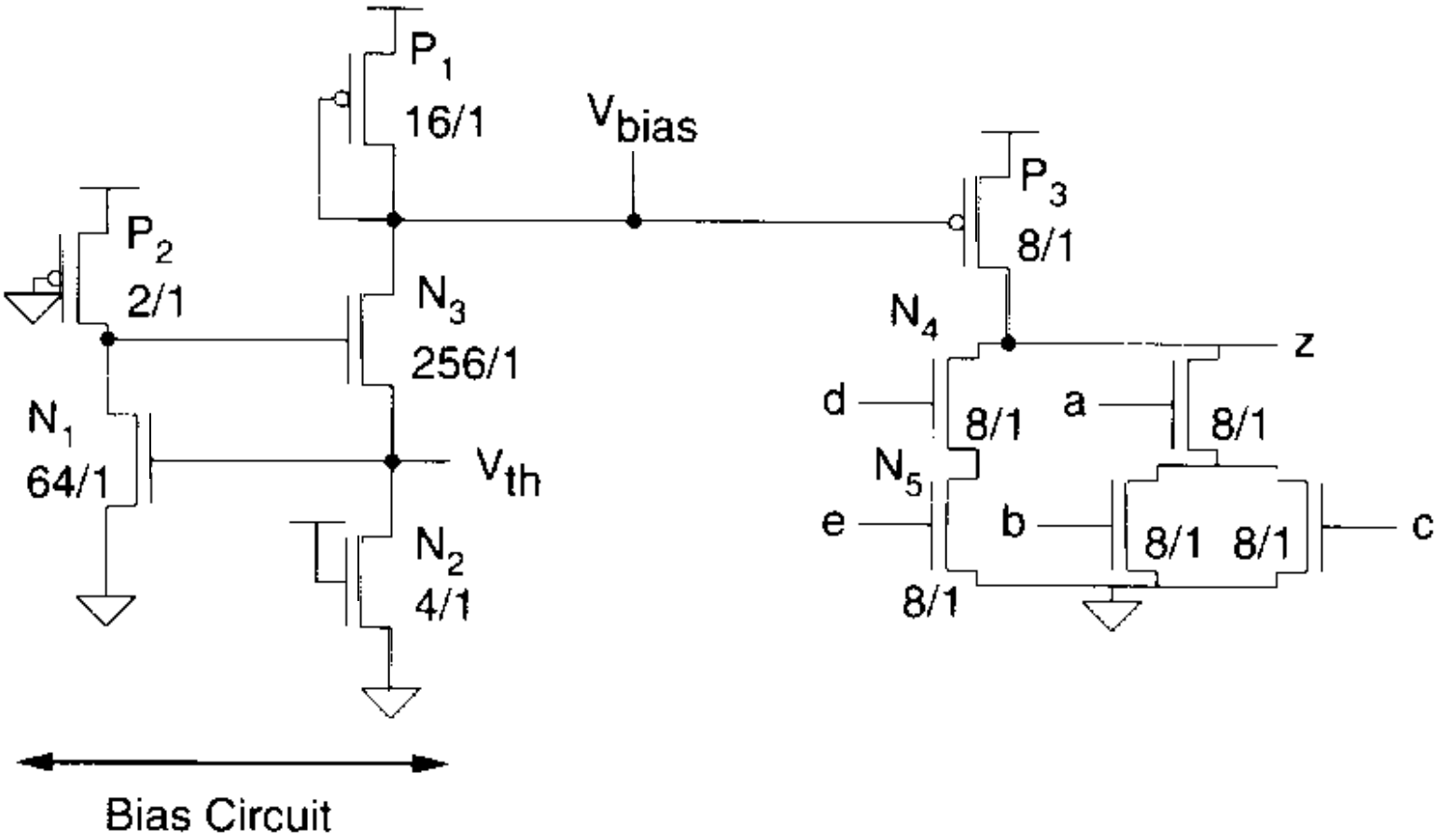
Trade-offs to be Considered

- To reduce static power, I_{Load} should be low
- To obtain a reasonable NM_L, $V_{OL} = I_{Load}R_{PDN}$ should be low
- To reduce $t_{pLH} \approx C_L V_{DD}/(2I_{Load})$, I_{Load} should be high
- To reduce $t_{pHL} \approx 0.69\ R_{PDN}C_L$, R_{PDN} should be kept small

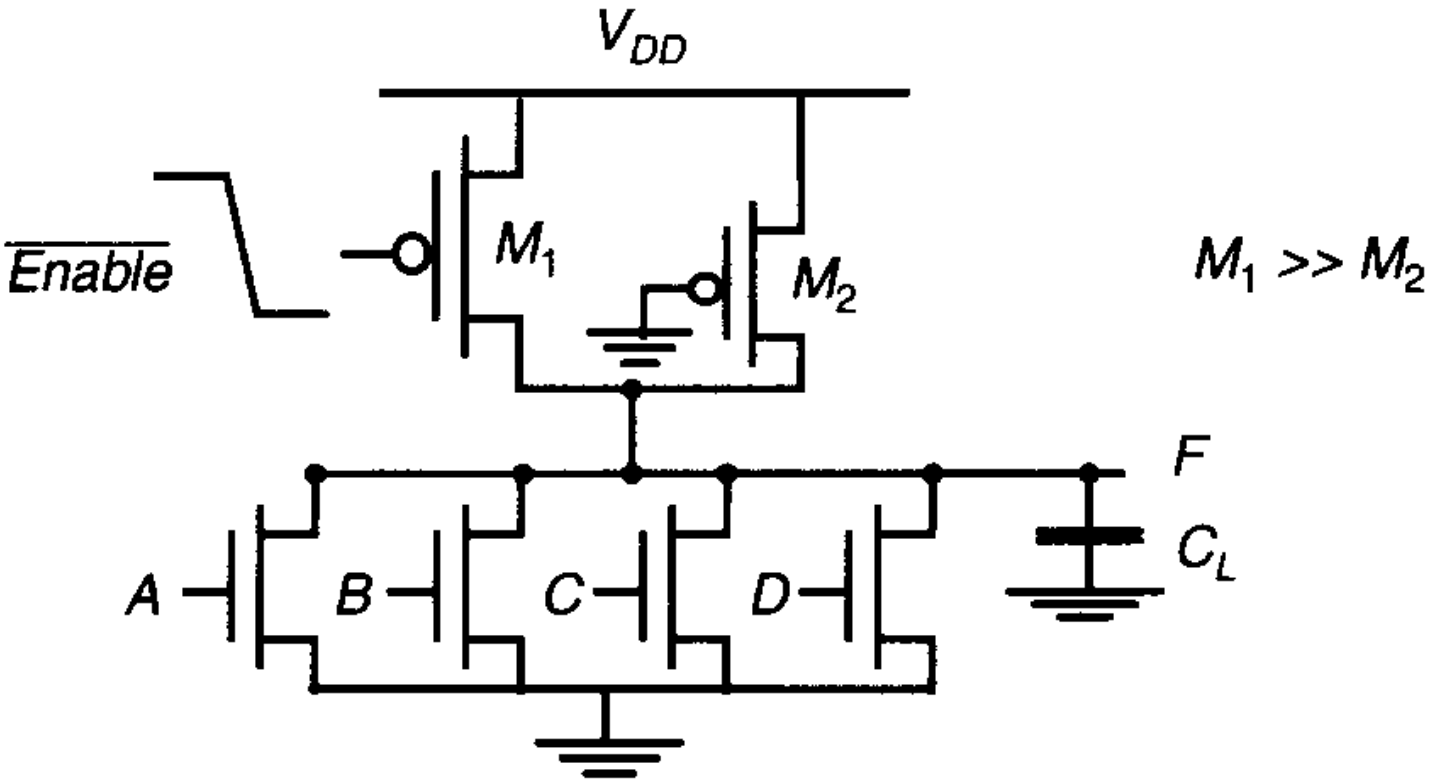
Improving DC and AC Characteristics

- Bias circuit to force VOL below threshold
- Build better load to improve VOL and switching time
- Use differential logic to eliminate static current

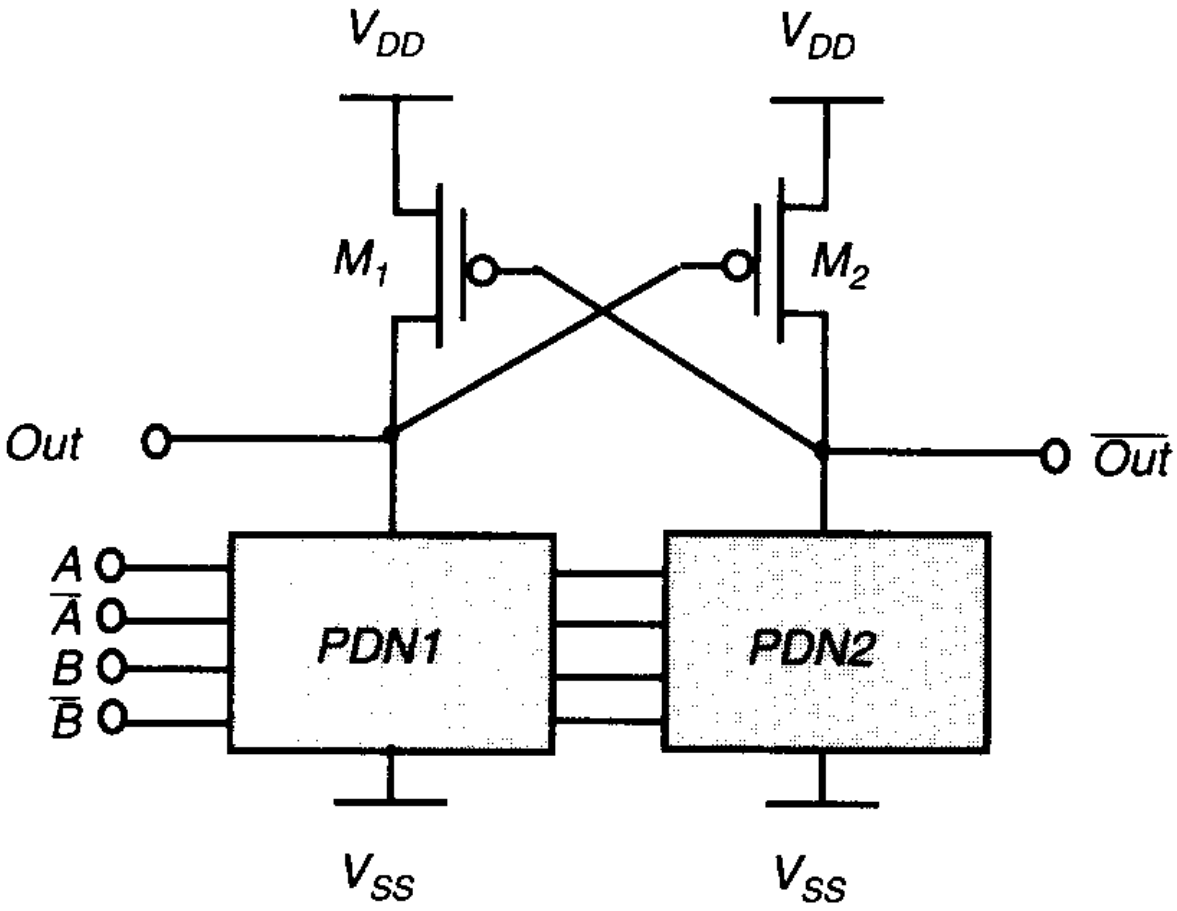
Forcing the Voltage Output Low



Adaptive Load



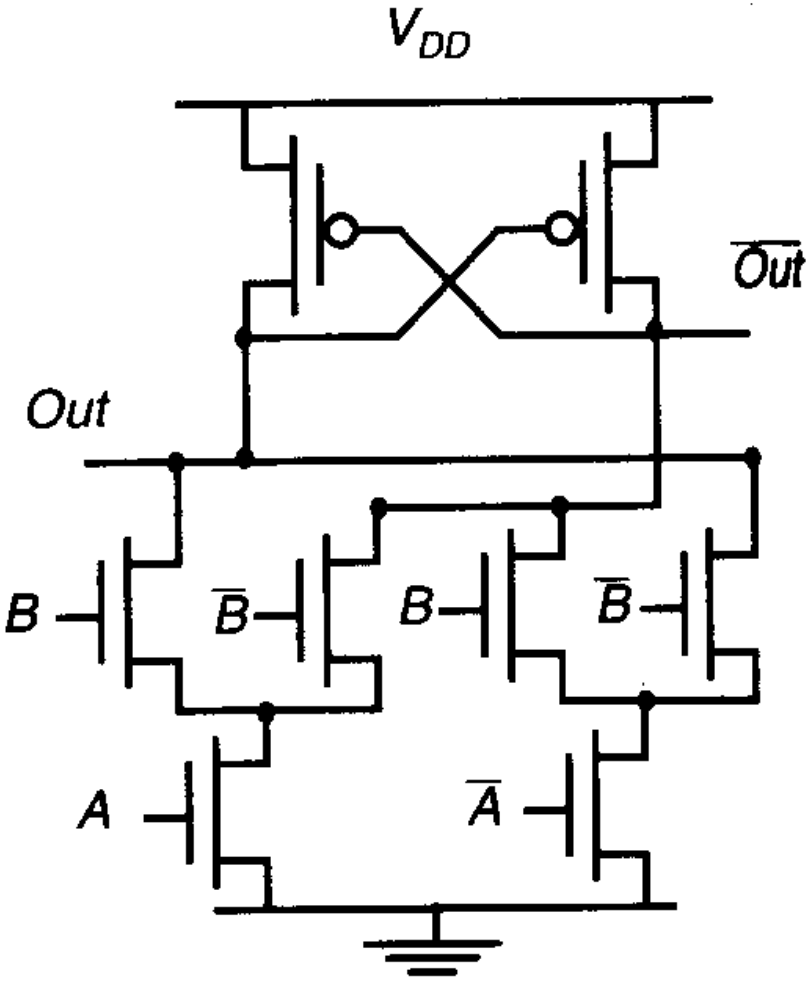
Improved Loads



(a) Basic principle

Differential Cascade Voltage Switch Logic (DCVSL)

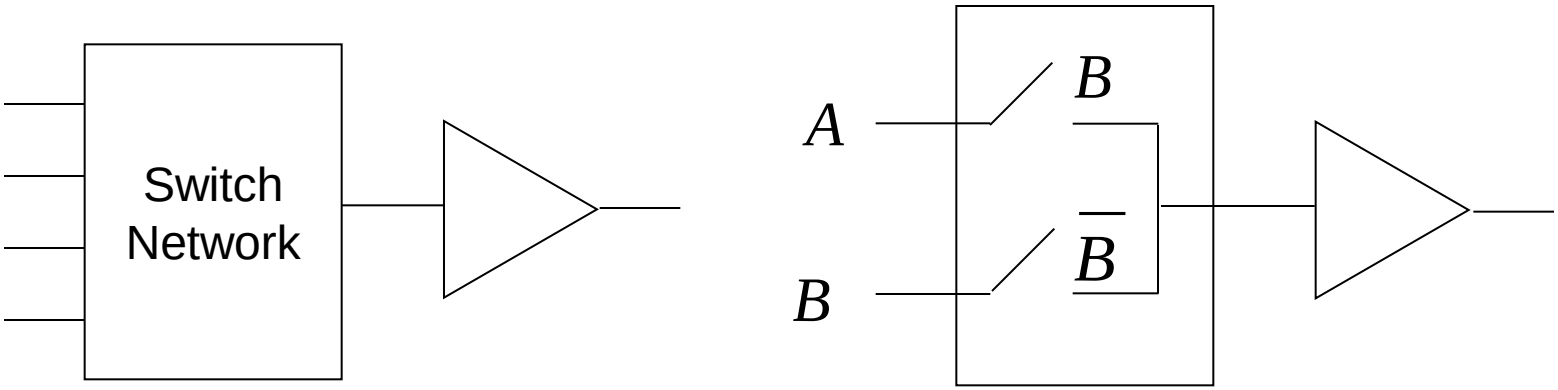
Example



(b) XOR-NXOR gate

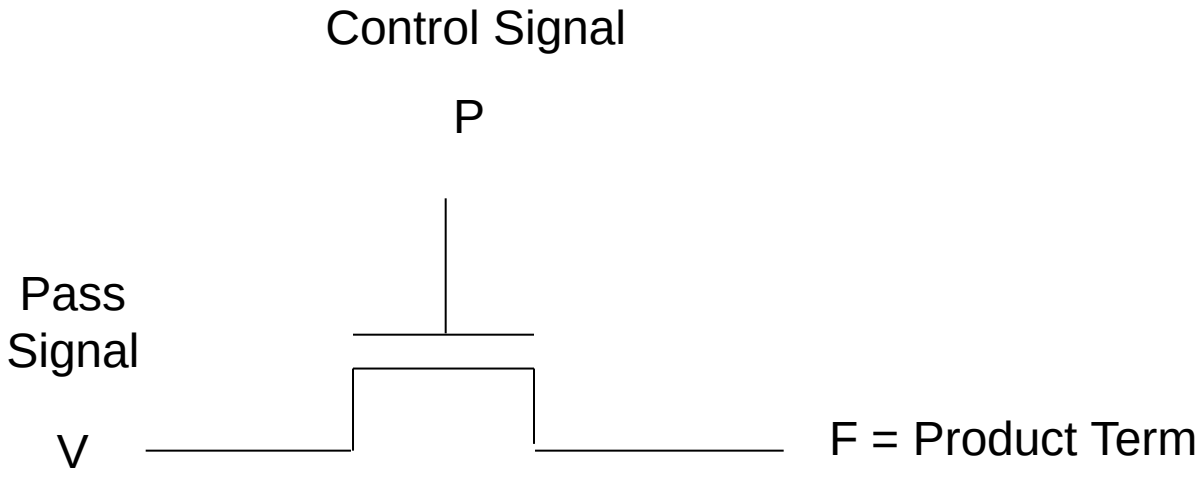
Pass Transistor Logic

Pass-Transistor Logic



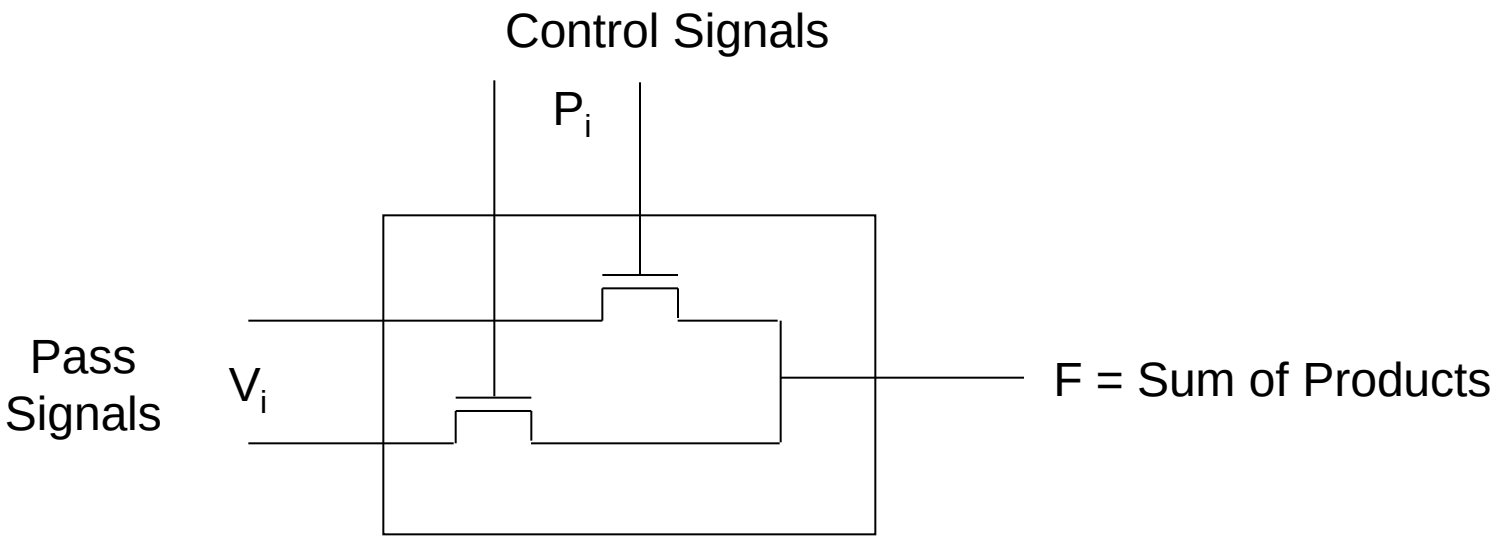
- Reduced number of transistors
- No static power consumption

Pass Transistor Logic



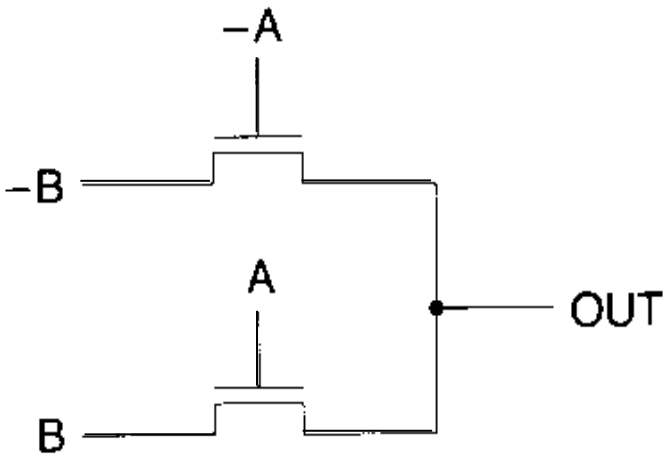
$$F = \begin{cases} Z & \text{if } P = 0 \\ V & \text{if } P = 1 \end{cases}$$

Basic Pass Transistor Logic Model



$$F = P_1(V_1) + P_2(V_2) + \ldots + P_n(V_n)$$

XNOR Gate



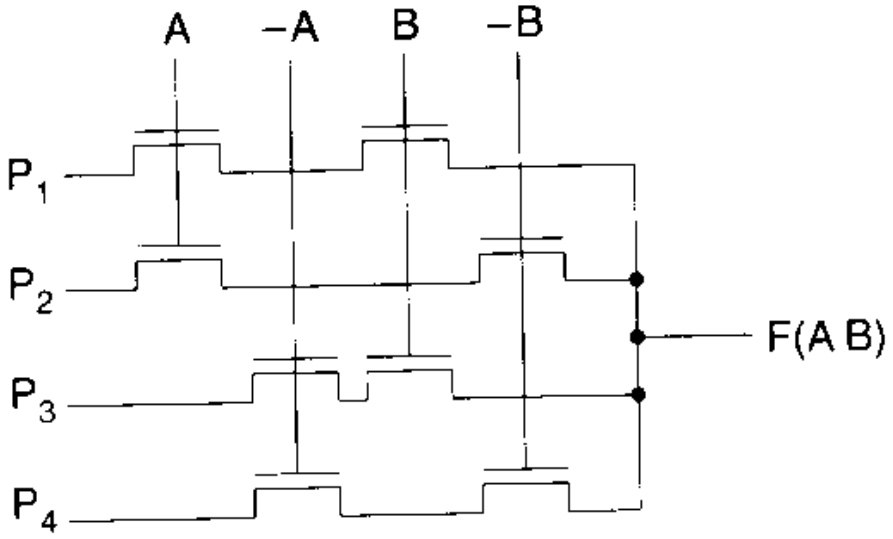
Truth Table

A	B	OUT	Pass Function
0	0	1	-A + -B
0	1	0	A + -B
1	0	0	-A + B
1	1	1	A + B

Modified Karnaugh Map

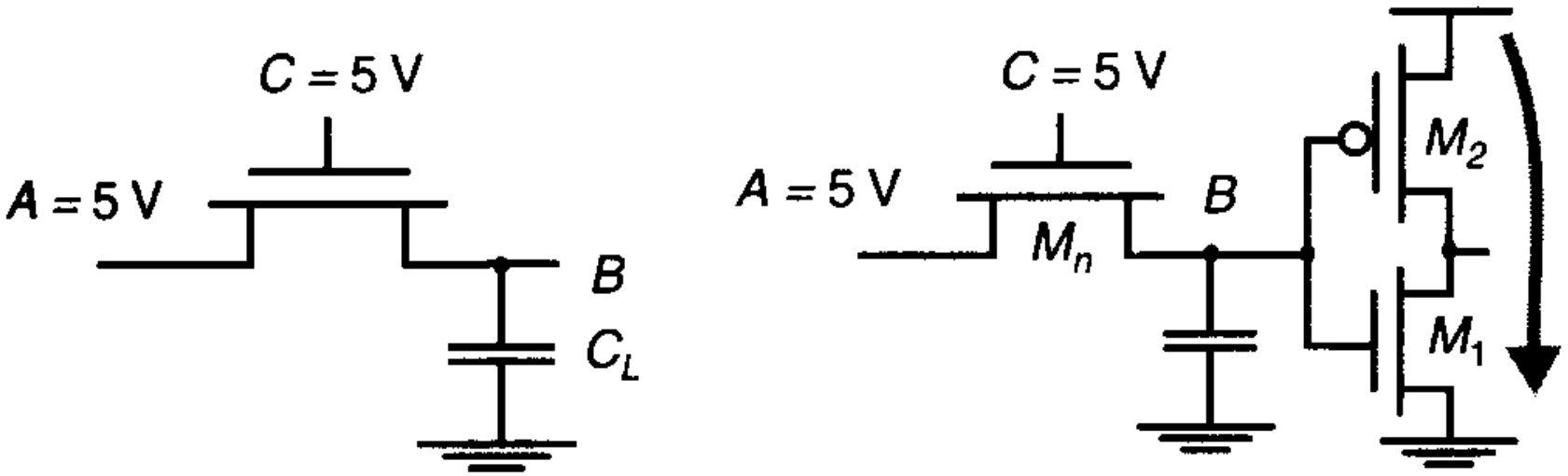
B \ A	0	1
0	-A, -B	-A, B
1	A, -B	A, B

Boolean Function Unit



Operation	P1	P2	P3	P4
AND(A,B)	0	0	0	1
XOR(A,B)	0	1	1	0
OR(A,B)	0	1	1	1
NOR(A,B)	1	0	0	0
NAND(A,B)	1	1	1	0

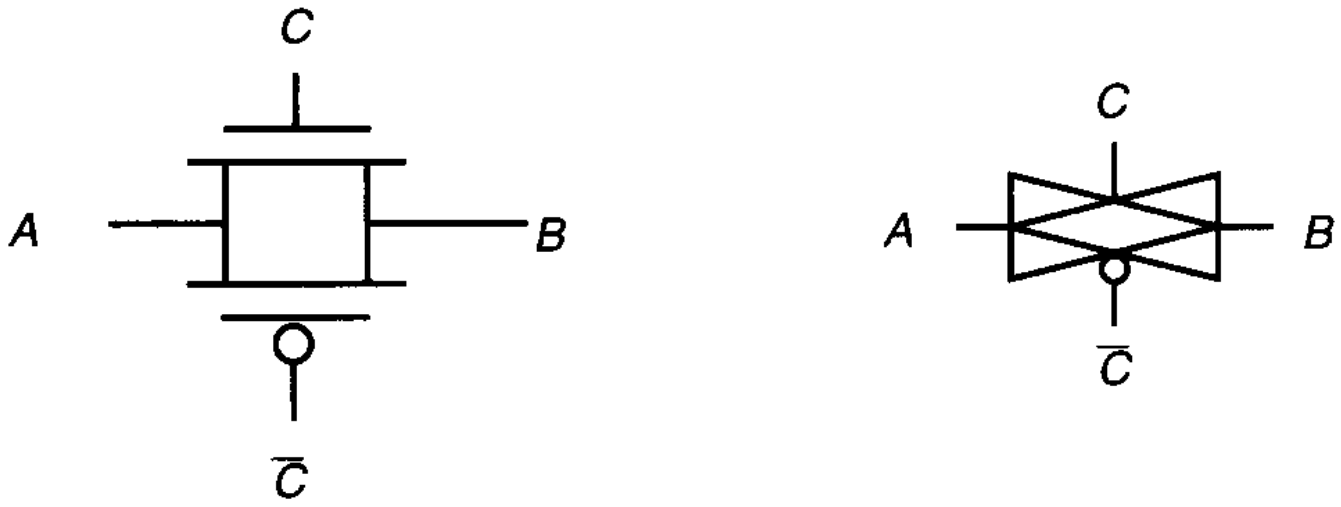
NMOS-only switch



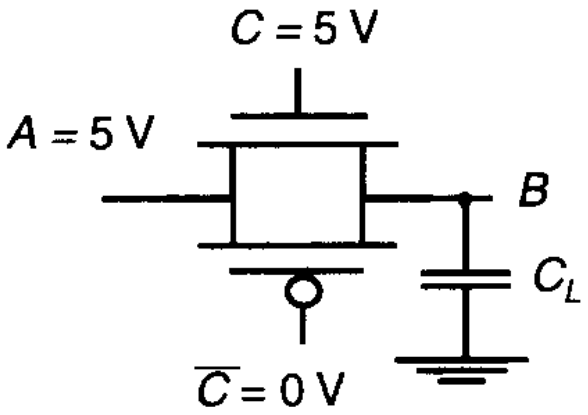
Problem: V_B does not pull up to V_{DD}, only to V_{DD} - $V_{tn(body\text{-}effect)}$

Cannot completely turn off the PMOS transistor
Causes static power consumption

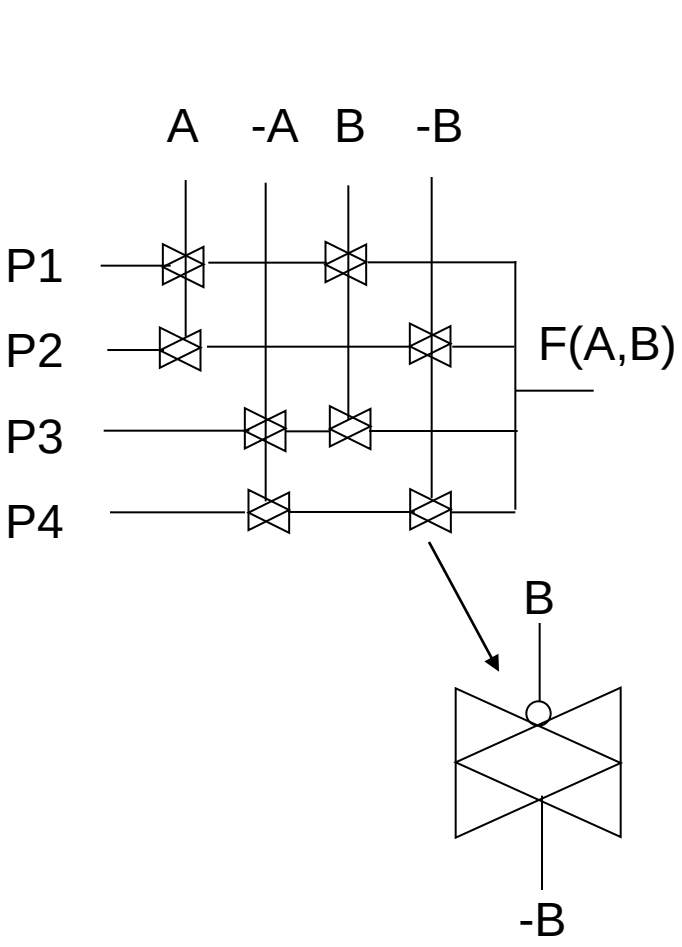
Solution 1: Transmission Gate

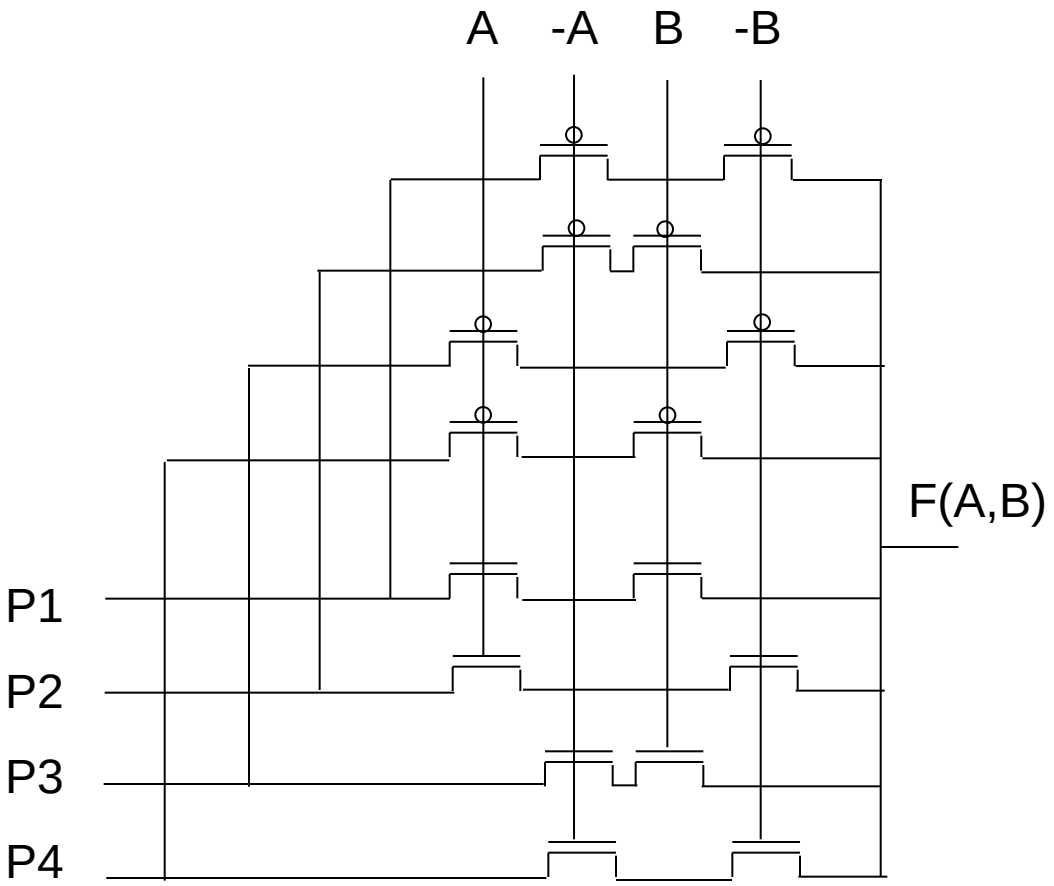


(a) Circuit

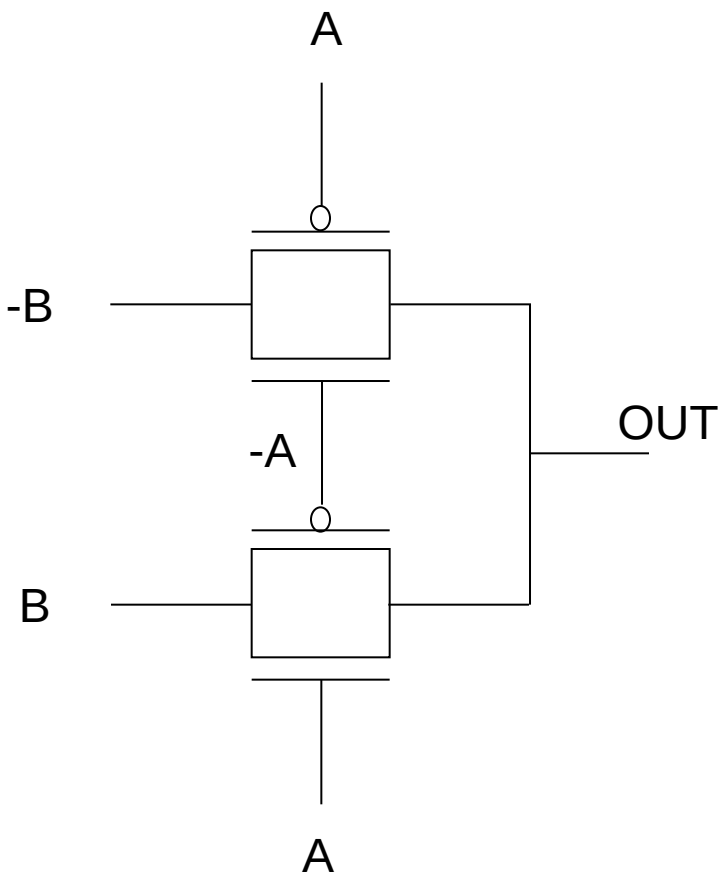


Transmission Gate Implementation

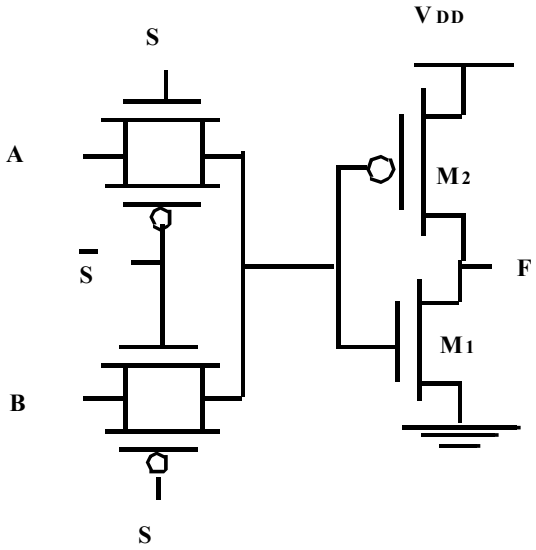


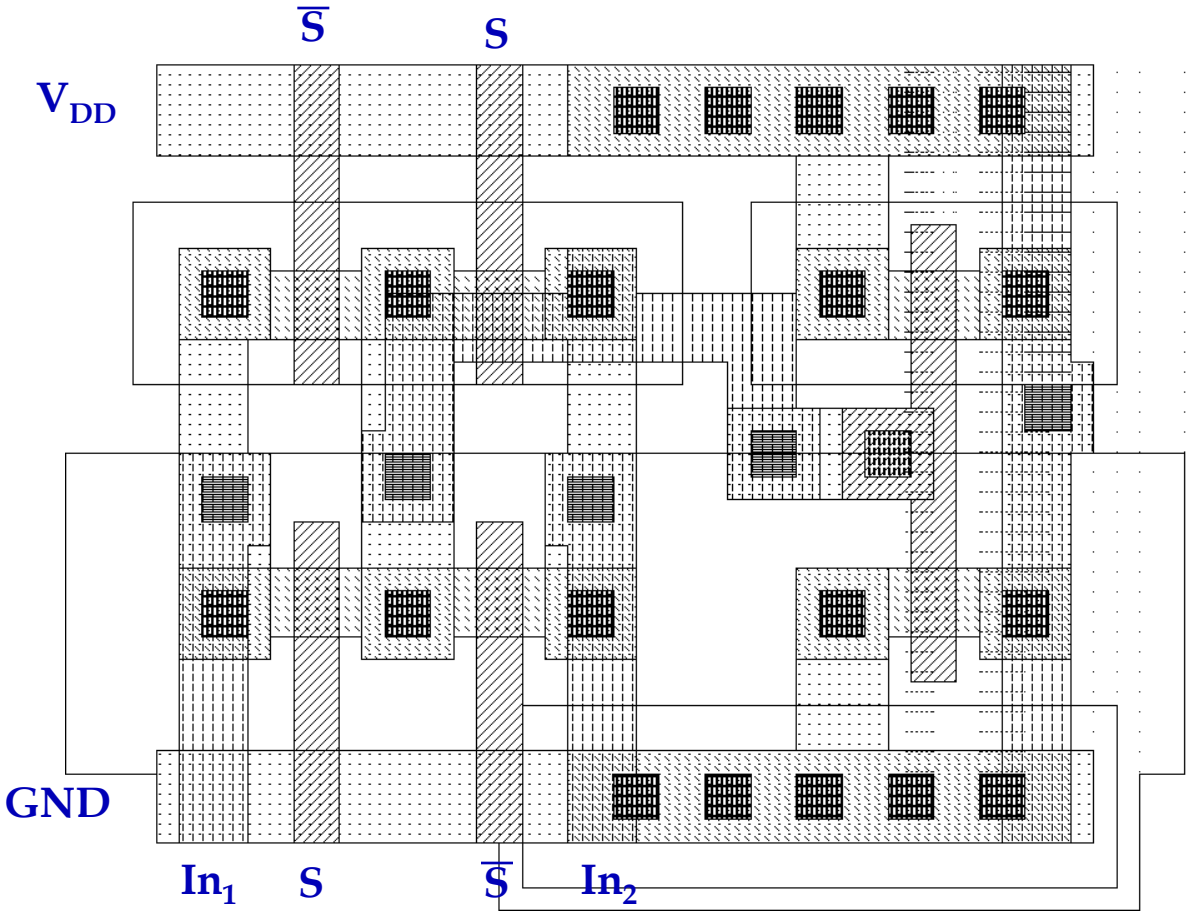


Transmission Gate XNOR

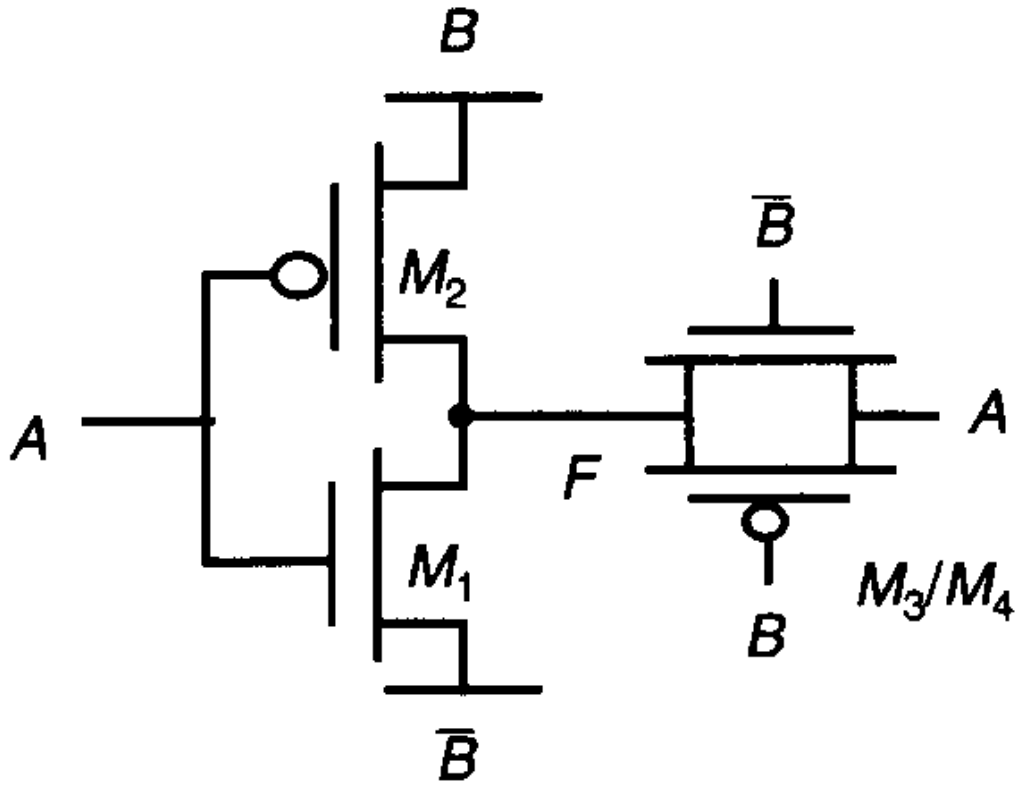


Transmission Gate (Inverting) Multiplexer

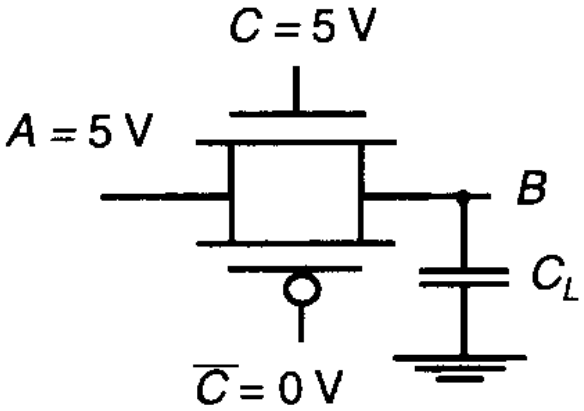




Transmission Gate XOR



Resistance of Transmission Gate



B is discharged originally

For NMOS, $V_{GS} = V_{DS}$, saturated or cutoff

For PMOS, $V_{GS} = -V_{DD,}$ V_{DS} increases from $-V_{DD}$ to 0, starts out in saturation, then transitions into non-saturation

$V_{out} < |V_{tp}|$: NMOS saturated, PMOS saturated

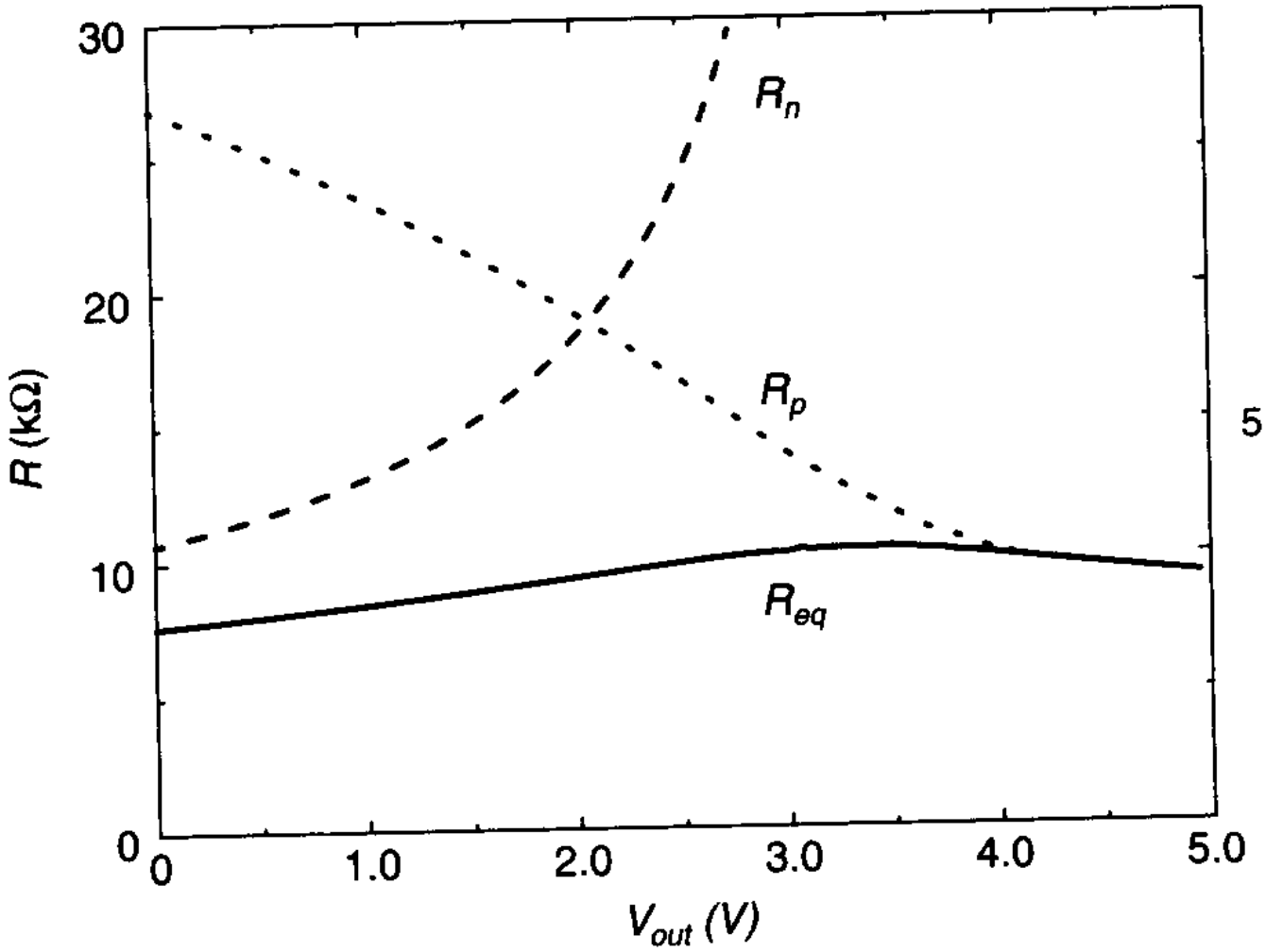
$|V_{tp}| < V_{out} < V_{DD} - V_{tn}$:

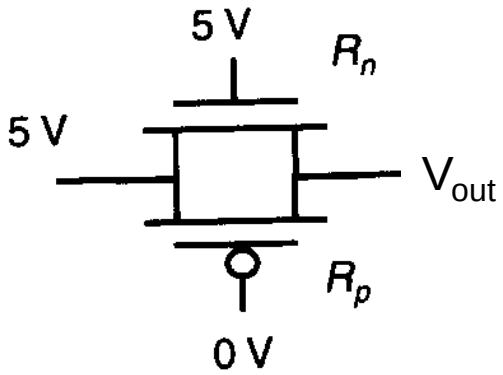
NMOS saturated, PMOS linear

$V_{DD} - V_{tn} < V_{out}$:

NMOS cutoff, PMOS linear

Resistance of Transmission Gate





Approximations

- Assume both in linear region, ignore body effect

$$G_{eq} = \frac{1}{R_{eq}}$$

$$= \frac{\beta_n (V_{DD} - V_B - V_{tn})(V_A - V_B)}{(V_A - V_B)} + \frac{\beta_p (V_{DD} + V_{tp})(V_A - V_B)}{(V_A - V_B)}$$

$$\approx \beta_n (V_{DD} - V_{tn}) + \beta_p (V_{DD} + V_{tp})$$

- Assume both in saturated region

$$G_{eq} = \frac{I_n + I_p}{V_{DD}}$$

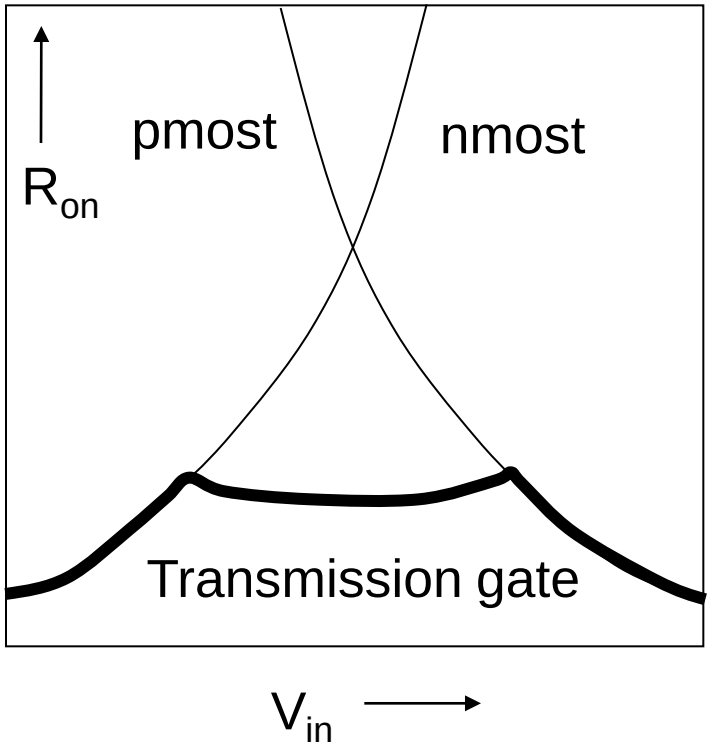
$$= \frac{\beta_n (V_{DD} - V_{tn})^2 + \beta_p (V_{DD} + V_{tp})^2}{2V_{DD}}$$

When Output Closely follows Input

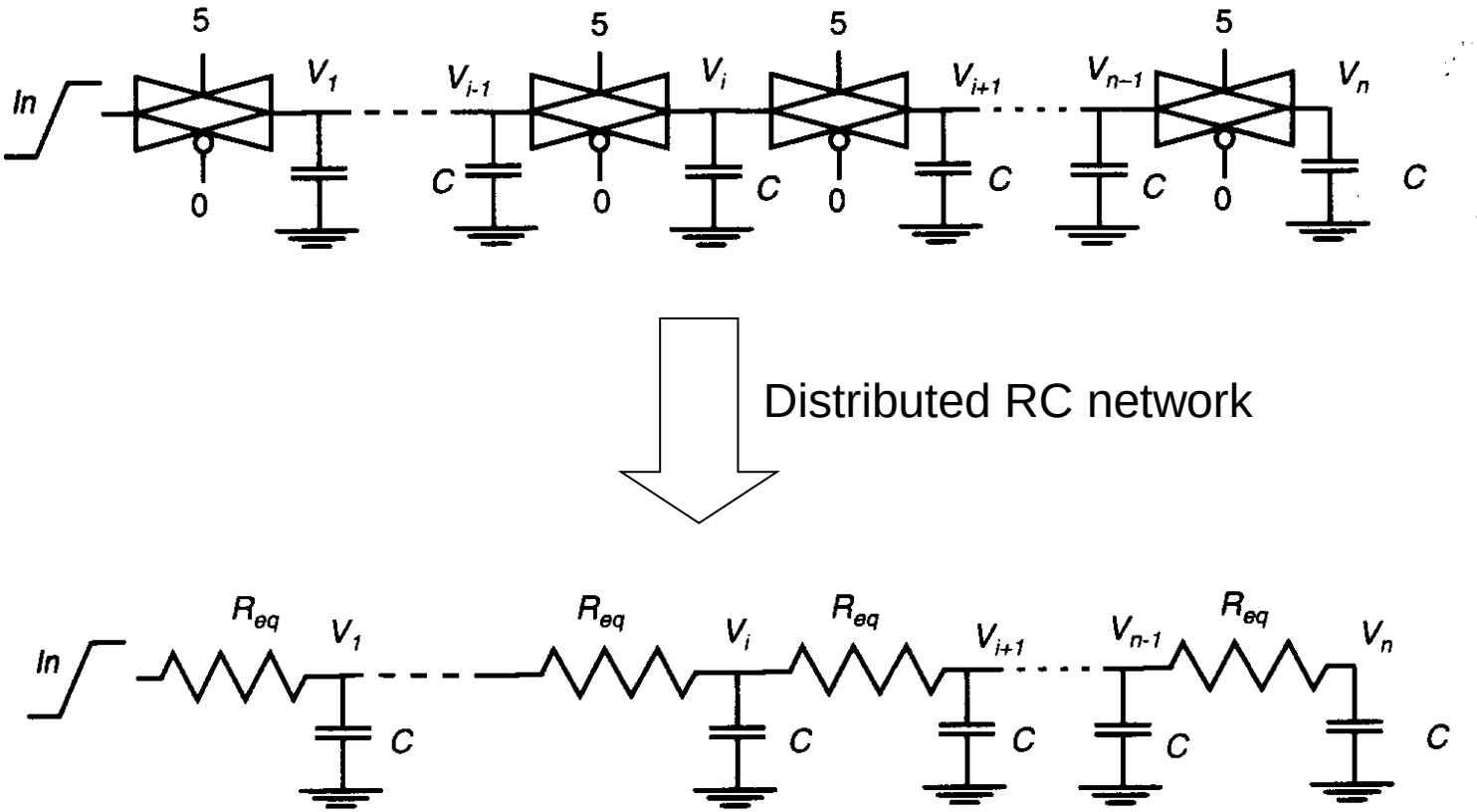
Region A:
NMOS unsaturated, PMOS off

Region B:
NMOS unsaturated, PMOS unsaturated

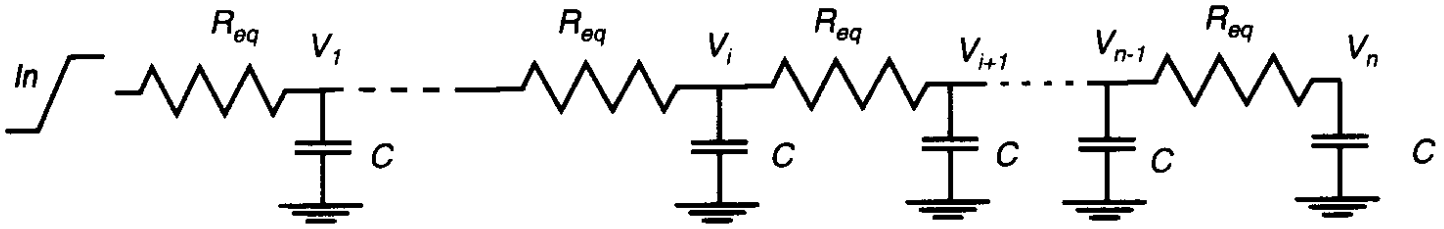
Region C:
NMOS off, PMOS unsaturated



Delay in Transmission Gate Networks



Elmore Delay



To solve for actual delay

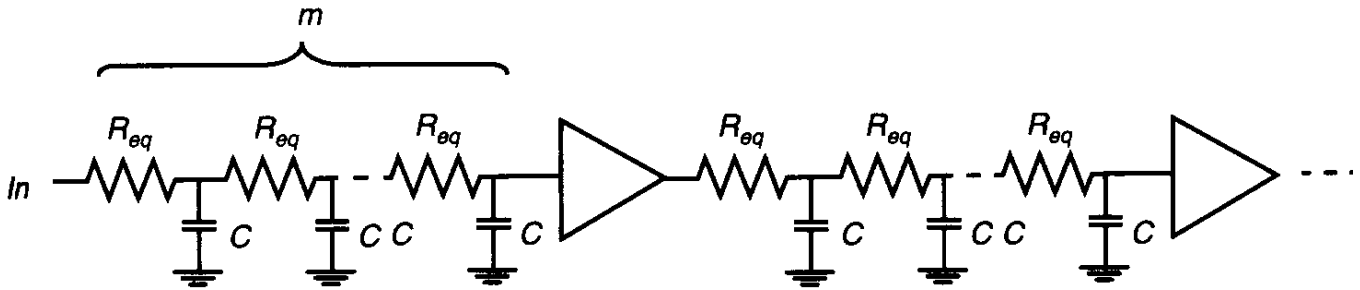
$$\frac{dV_i(t)}{dt} = \frac{1}{R_{eq}C}\left[V_{i+1}(t) + V_{i-1}(t) - 2V_i(t)\right]$$

Estimate the dominant time constant:

assume all internal nodes are pre-charged to VDD, and a step input is applied

$$\tau_N = \sum_{k=1}^{N} C \sum_{j=k}^{N} R_{eq} = \sum_{k=1}^{N} R_{eq} \sum_{j=k}^{N} C = \frac{n(n+1)}{2} R_{eq} C$$

Delay Optimization by Buffer Insertion



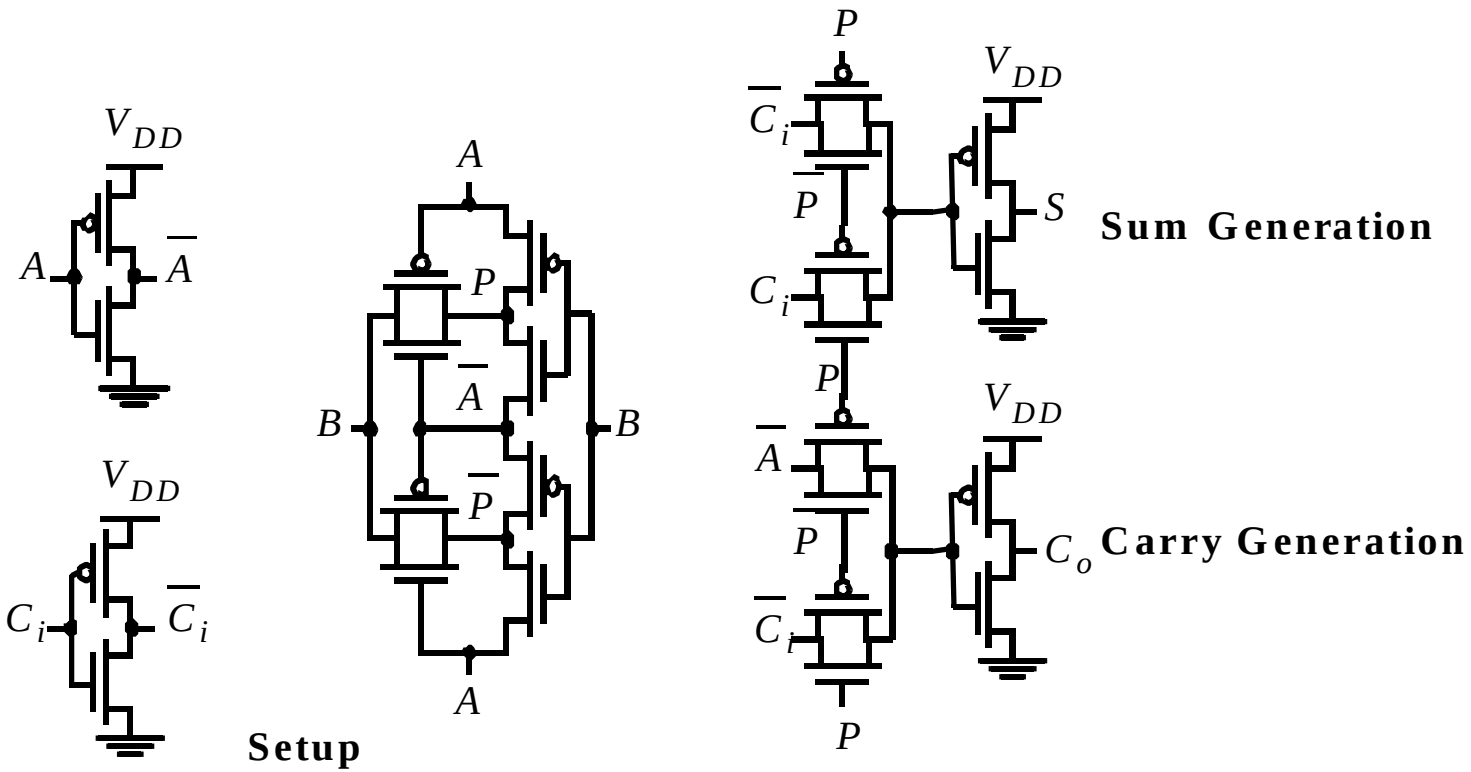
- Delay of RC chain $t_p = 0.69\,\tau_N = 0.69\,\frac{n(n+1)}{2}R_{eq}C$
- Delay of buffered chain

$$t_p = 0.69\left\lceil \frac{n}{m}\frac{m(m+1)}{2}R_{eq}C \right\rceil + \left(\frac{n}{m} - 1\right)t_{pbuf}$$

$$= 0.69\left\lceil \frac{n(m+1)}{2}R_{eq}C \right\rceil + \left(\frac{n}{m} - 1\right)t_{pbuf}$$

$$m_{opt} = 1.7\sqrt{\frac{t_{pbuf}}{R_{eq}C}}$$

Transmission Gate Full Adder



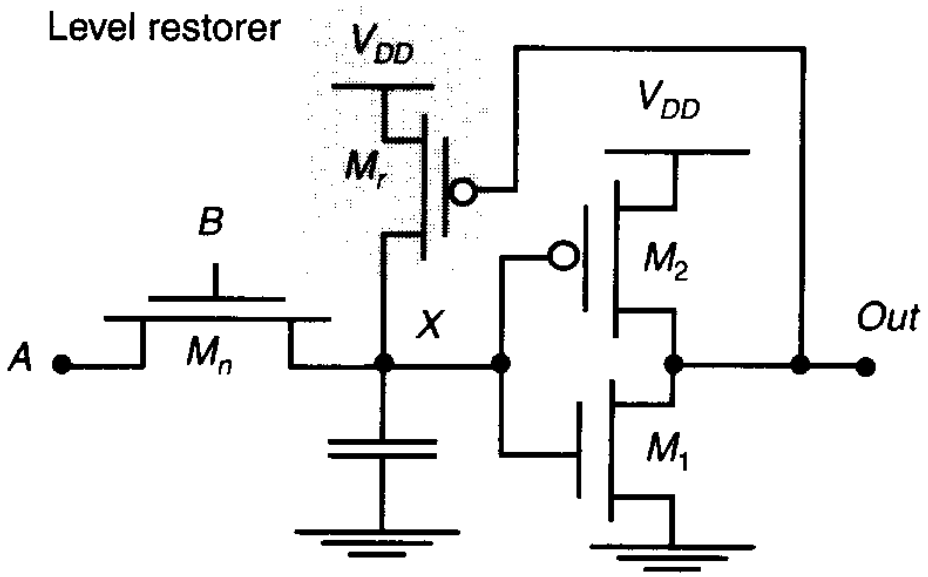
Adder Truth Table

C	A	B	A.B(G)	A+B	A⊕B(P)	SUM	CARRY
0	0	0	0	0	0	0	0
0	0	1	0	1	1	1	0
0	1	0	0	1	1	1	0
0	1	1	1	1	0	0	1
1	0	0	0	0	0	1	0
1	0	1	0	1	1	0	1
1	1	0	0	1	1	0	1
1	1	1	1	1	0	1	1

SUM = A⊕B⊕C

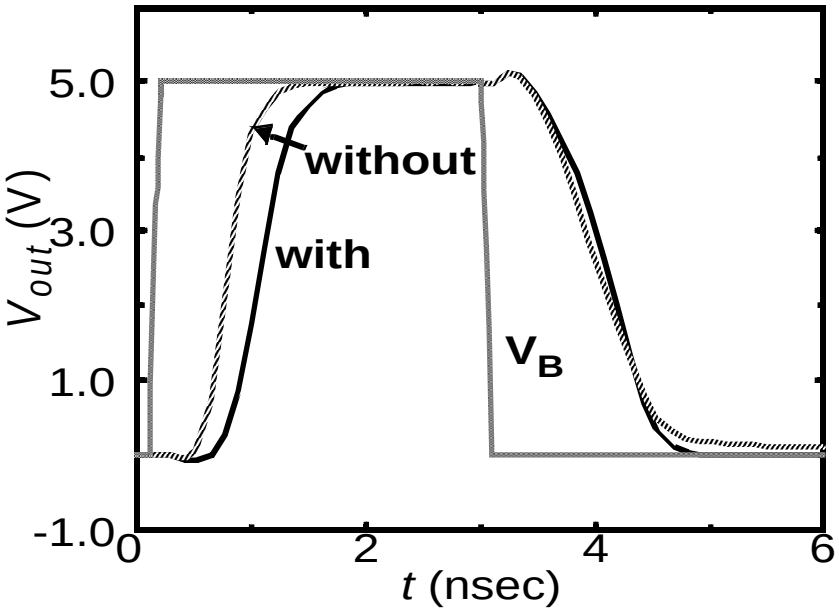
CARRY = C if A⊕B = 1
CARRY = A (or B) if A⊕B = 0

Solution 2:
Level Restoring Transistor for NMOS Only Logic

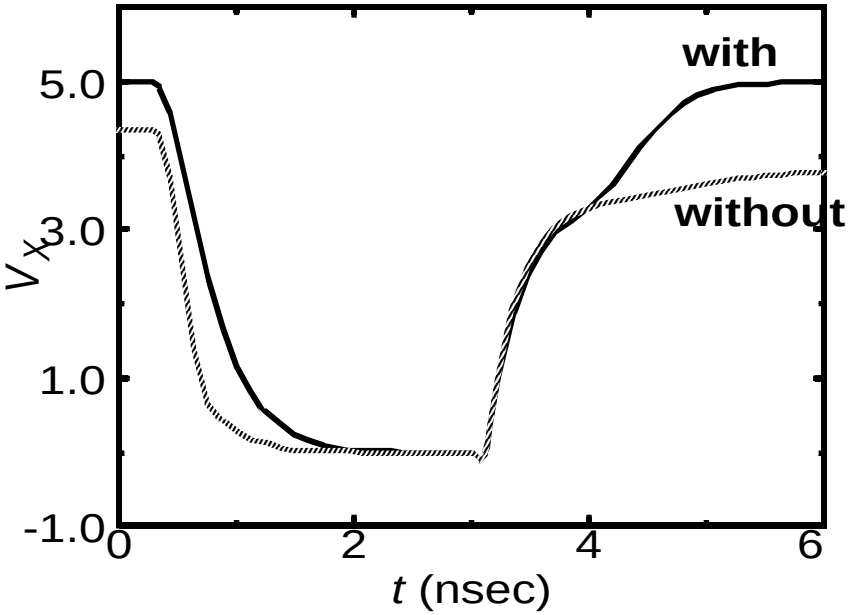


- Full Swing
- Disadvantage: More complex, larger capacitance

Level Restoring Transistor

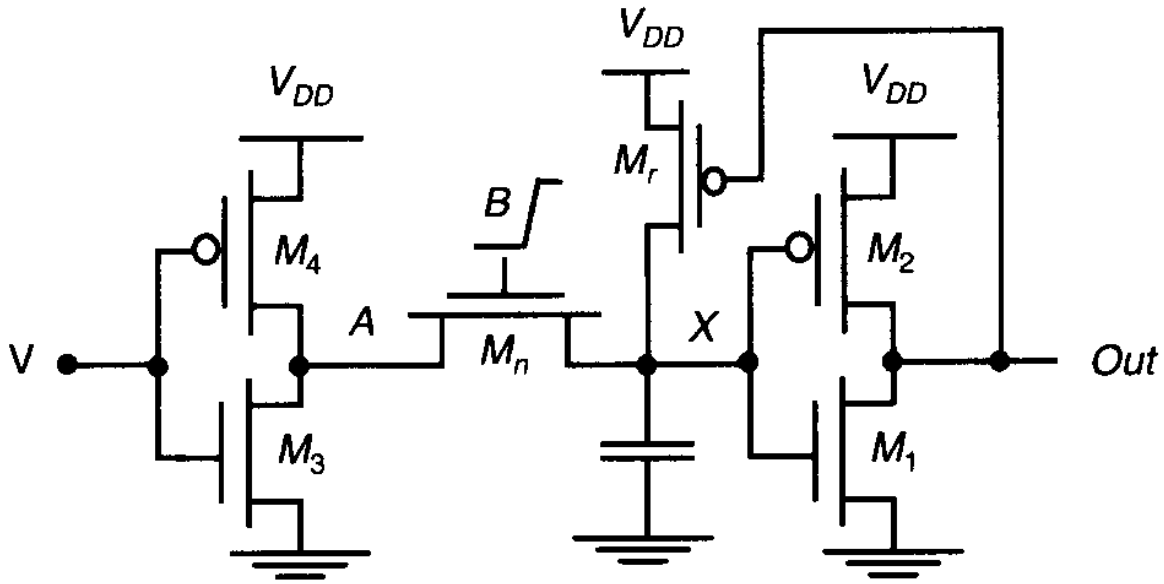


(a) Output node



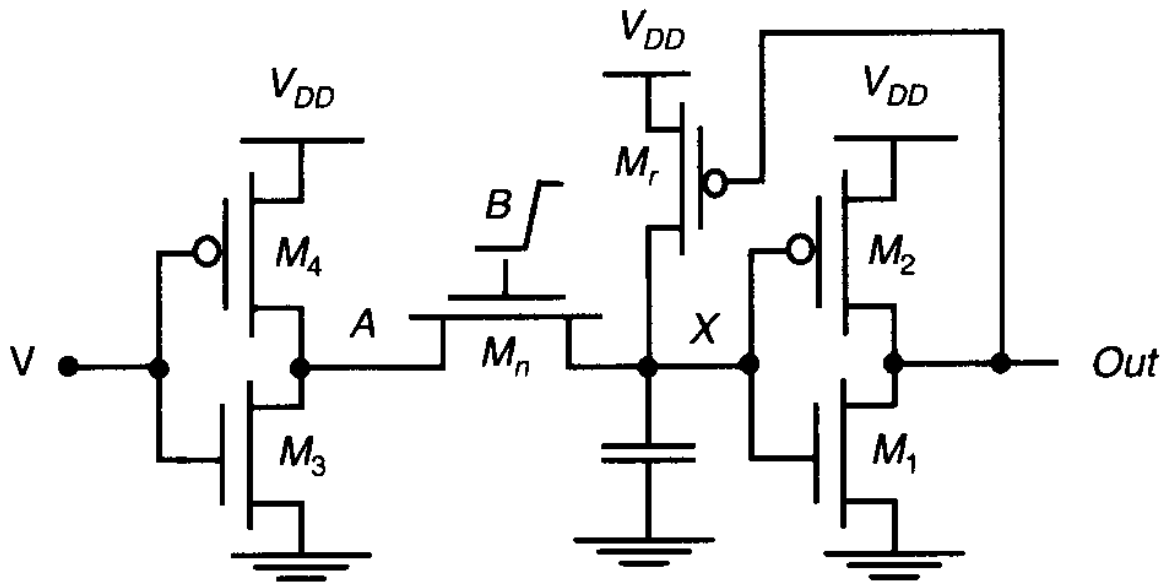
(b) Intermediate node X

Proper Sizing of Level Restoring Transistor



- In transient, conducting path from M_r to M_3 via M_n when A is low, B switches from low to high, and X is high
- M_r must not be too large, otherwise, X cannot be brought below threshold voltage, V_M, of inverter, M_r cannot be turned off

Sizing of a Level Restorer



$$I = \beta_3 (V_{DD} - V_{tn}) V_A$$

$$= \frac{\beta_n}{2} (V_B - V_A - V_{tn})^2$$

$$= \beta_r \left[(V_{DD} + V_{tp})(V_{DD} - V_M) - \frac{(V_{DD} - V_M)^2}{2} \right]$$

Sizing of a Level Restorer

$$V_{DD} = 5V$$

$$V_{tn} = -V_{tp} = 0.75V$$

$$V_M = 2.5V$$

$$I = \beta_r \left[(V_{DD} + V_{tp})(V_{DD} - V_M) - \frac{(V_{DD} - V_M)^2}{2} \right] = 7.5\beta_r$$

$$I = \beta_3 (V_{DD} - V_{tn}) V_A$$

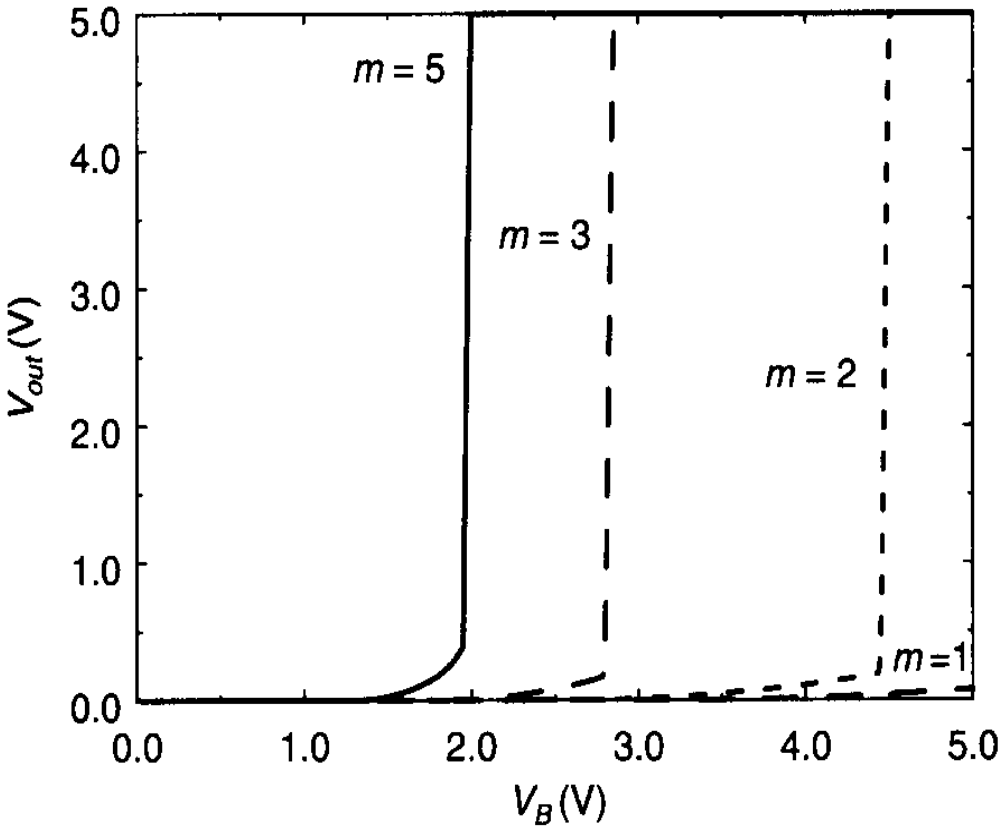
$$\Rightarrow V_A = 1.76 \frac{\beta_r}{\beta_n} \qquad \text{if } M_3 \text{ and } M_n \text{ are of equal size}$$

$$V_B \leq V_{DD}$$

$$\Rightarrow V_B = 3.87 \sqrt{\frac{\beta_r}{\beta_n}} + 1.76 \frac{\beta_r}{\beta_n} + 0.75 \leq 5V$$

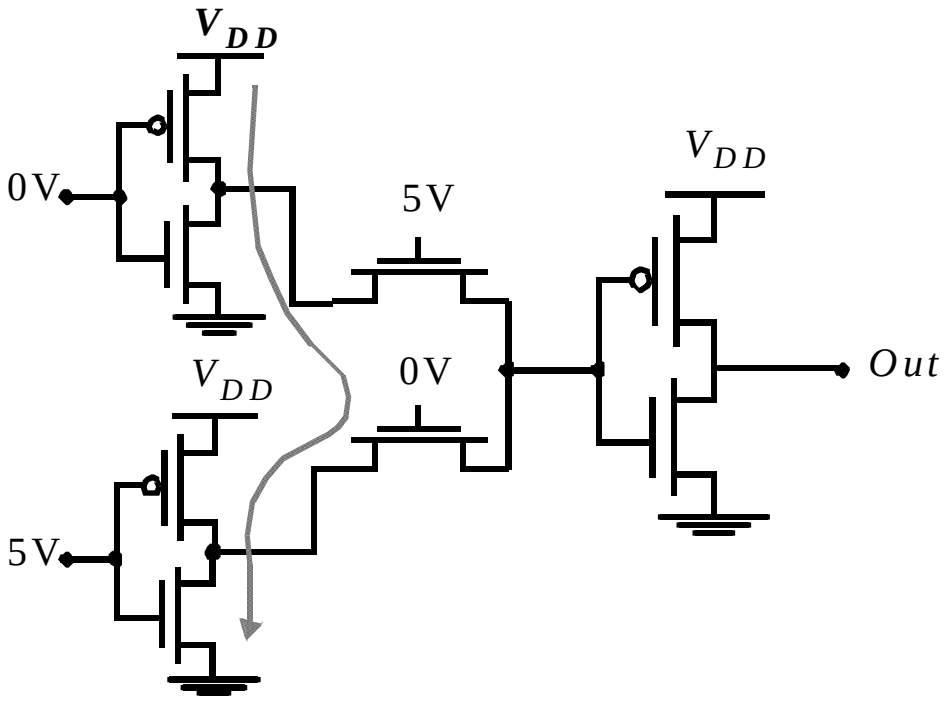
$$m = \frac{\beta_n}{\beta_r} > 1.55$$

Proper Sizes of Restorer



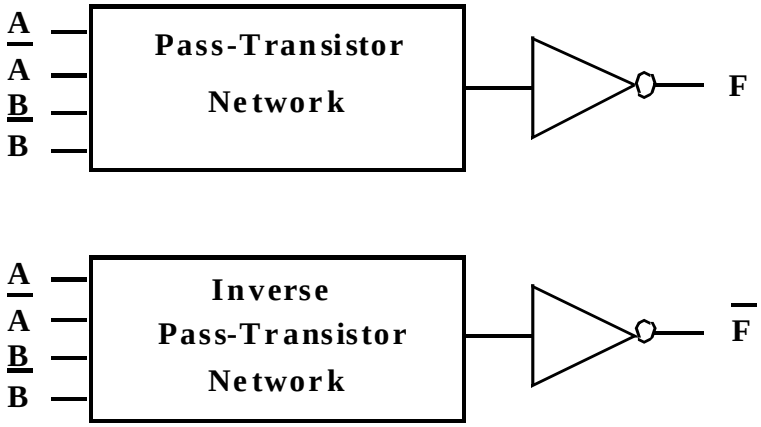
Making the NMOS pass-transistor and PMOS restorer the same size is reasonable

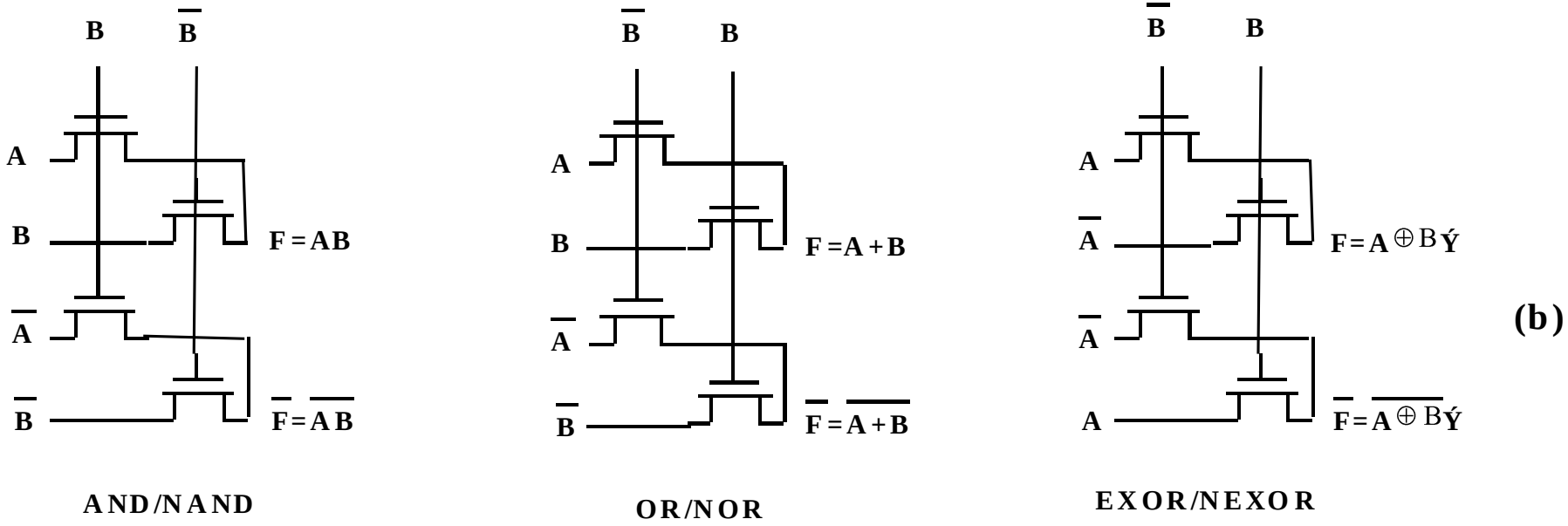
Solution 3: Single Transistor Pass Gate with V_T=0



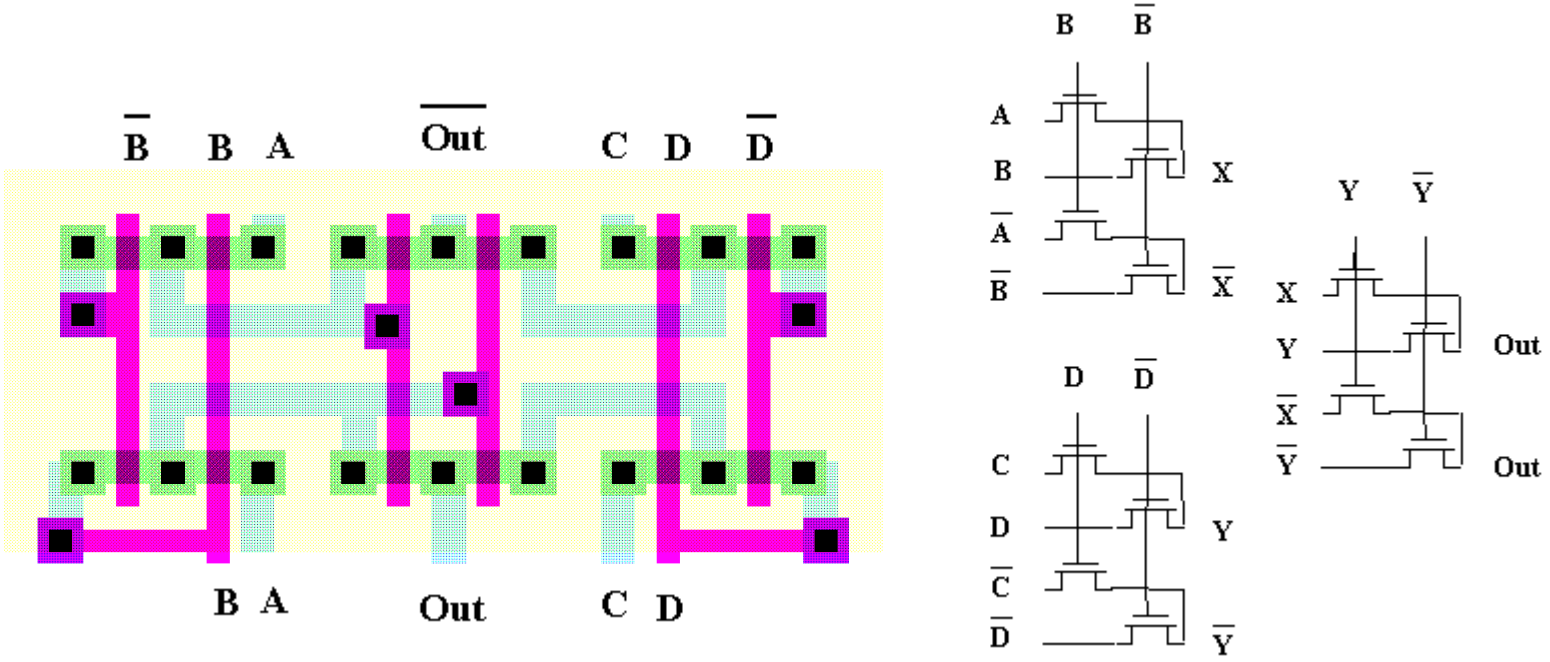
WATCH OUT FOR LEAKAGE CURRENTS

Complimentary Pass Transistor Logic





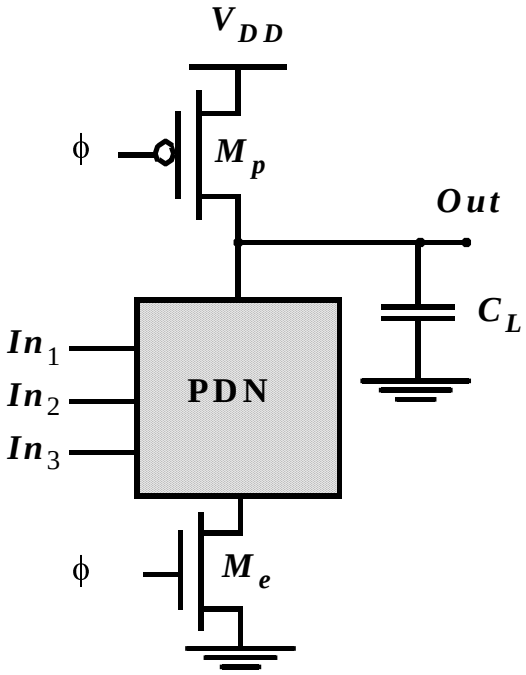
4 Input NAND in CPL



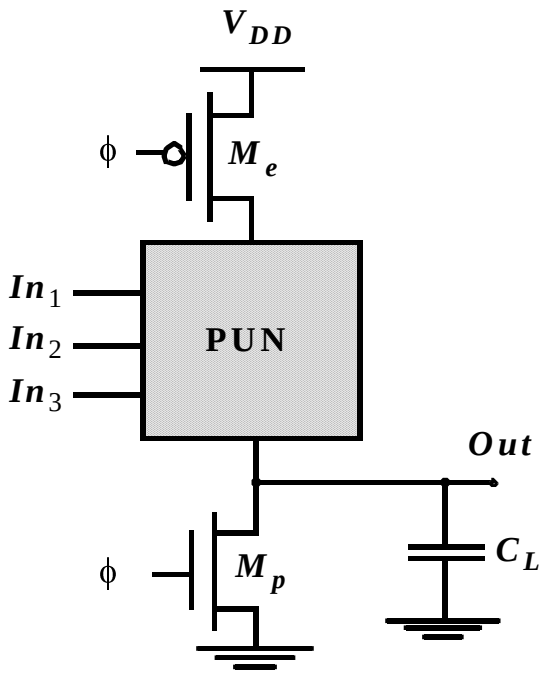
- Total number of transistors needed = 14 (including the final buffer)
- But AND function is simultaneously present
- t_{pHL} = 1.05ns, t_{pLH} = 0.45ns

Dynamic Logic

Dynamic Logic



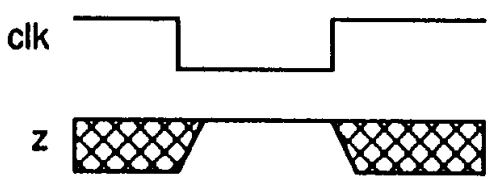
ϕn network



ϕp network

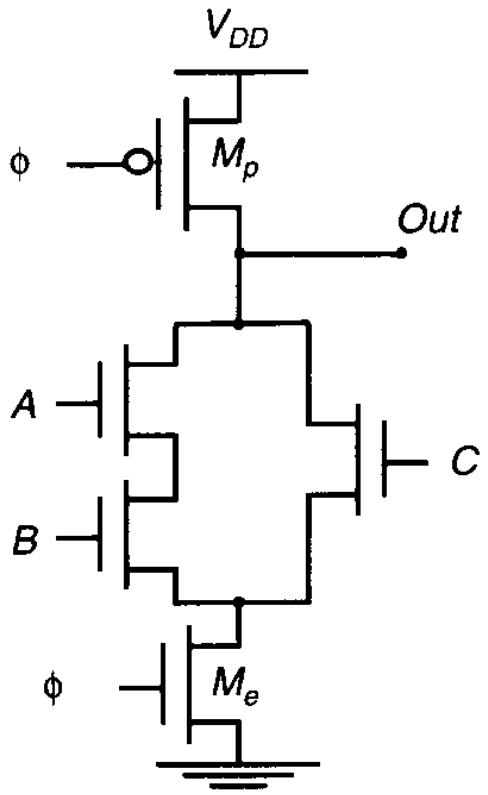
2 phase operation:

- Precharge
- Evaluation



clk=0: z = 1 (precharge)
clk=1: z = logic function

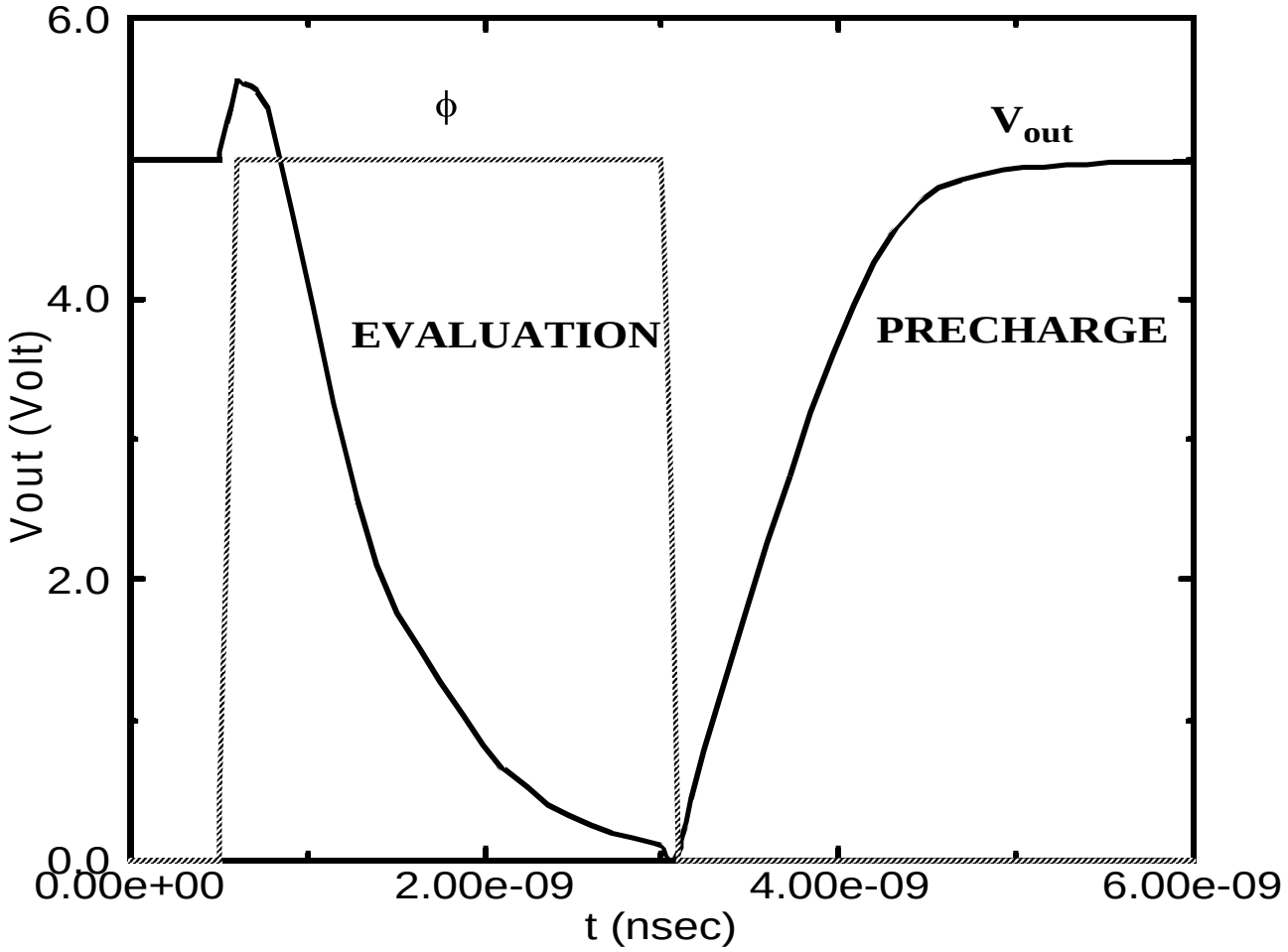
Example



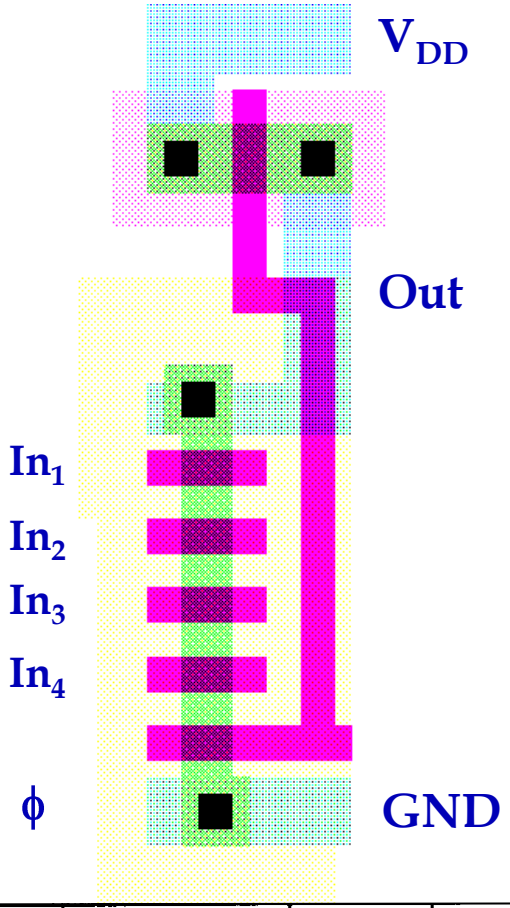
(b) Example

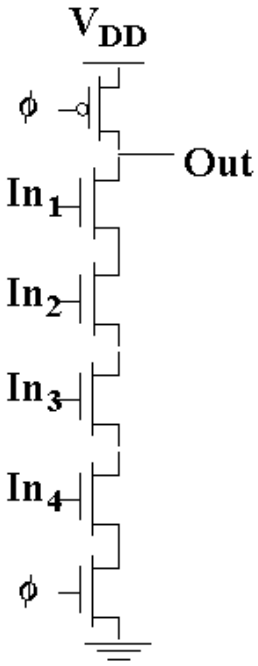
- N + 2 transistors
- Ratioless
- No static power consumption
- Small Noise Margins (NM_L)
- Requires Clock
- Pull-down resistance increases due to the evaluation transistor

Transient Response



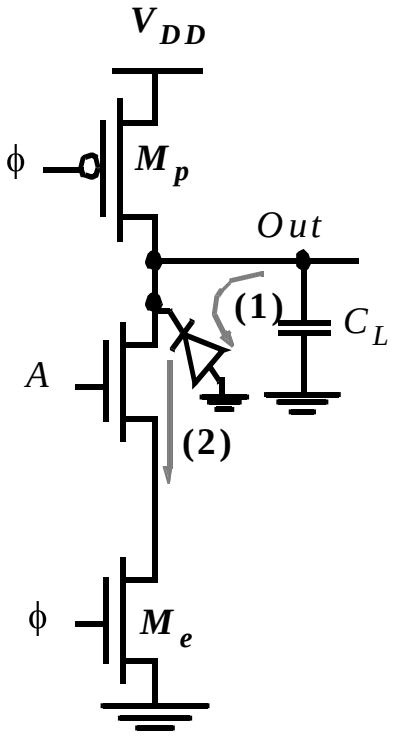
Dynamic 4 Input NAND Gate



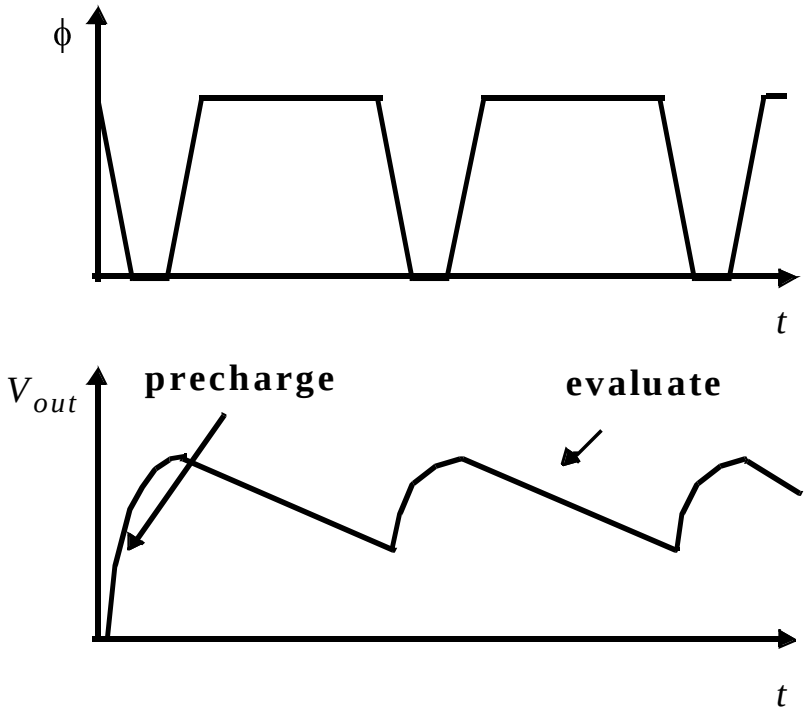


Area	Static Current	Transistors	V_{OH}	V_{OL}	V_M	NM_H	NM_L	t_{pHL}	t_{pLH}	t_p
212 μm^2	0 µA	6	5 V	0 V	0.75V	4.25 V	0.75 V	0.74 nsec	0 nsec	0.37 nsec

Reliability Problems — Charge Leakage



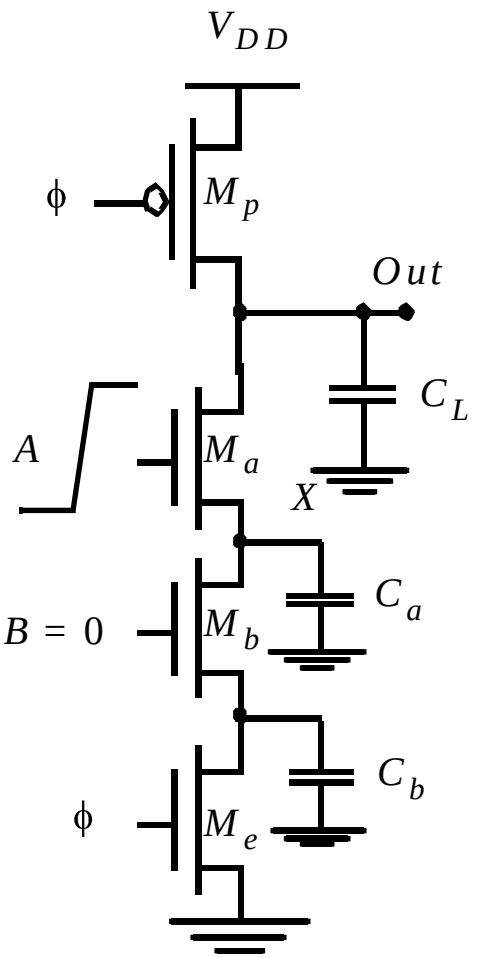
(a) Leakage sources



(b) Effect on waveforms

Dynamic circuits require a minimal clock rate

Charge Sharing (redistribution)



case 1) if $\Delta V_{out} < V_{Tn}$

$$C_L V_{DD} = C_L V_{out}(t) + C_a (V_{DD} - V_{Tn}(V_X))$$

or

$$\Delta V_{out} = V_{out}(t) - V_{DD} = -\frac{C_a}{C_L}(V_{DD} - V_{Tn}(V_X))$$

case 2) if $\Delta V_{out} > V_{Tn}$

$$\Delta V_{out} = -V_{DD}\left(\frac{C_a}{C_a + C_L}\right)$$

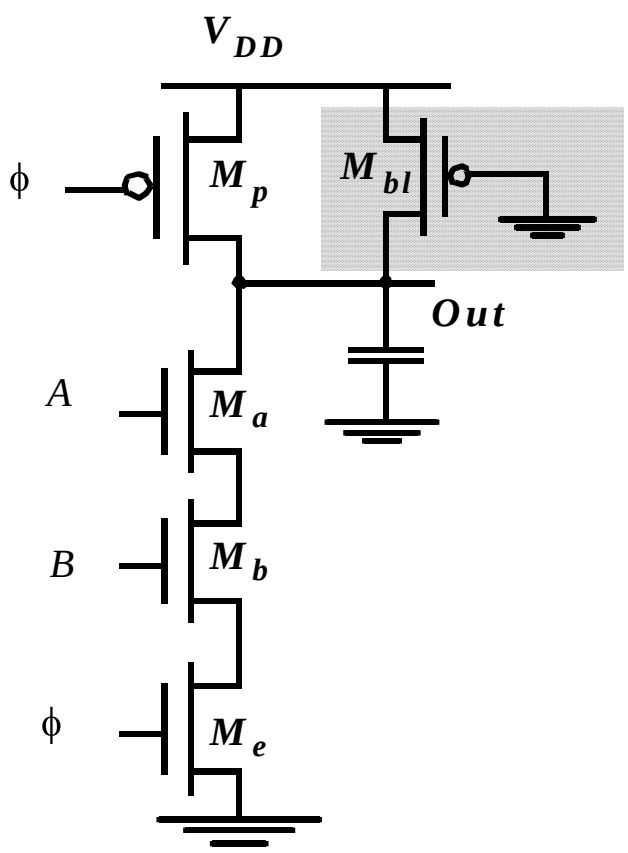
Minimize Charge Sharing

- Keep the change in storage voltage below | V_{tp} |
  - the output might be connected to a static inverter as in Domino logic

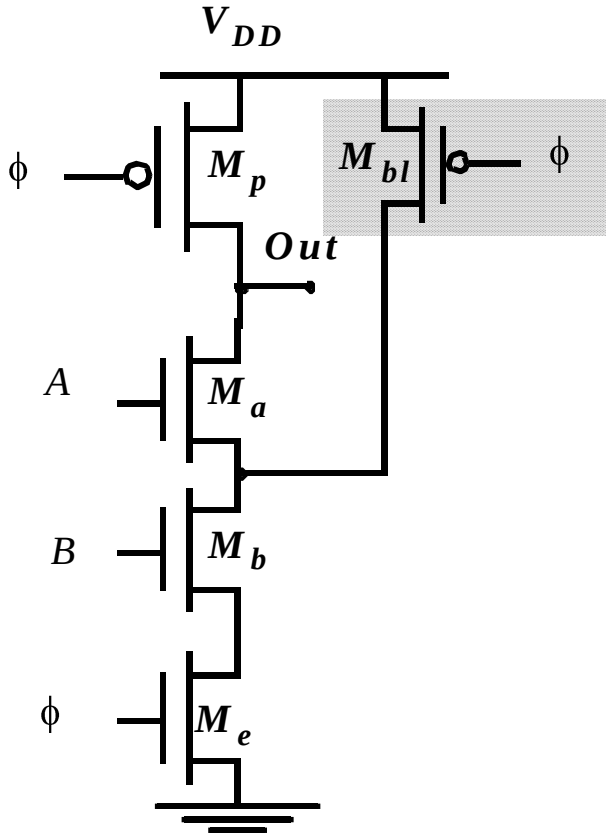
$$\frac{C_a}{C_L} < \frac{|V_{tp}|}{V_{DD} - V_{tn}} = 0.2$$

- C_a is normally smaller than C_L, but if there is series connection of NMOS transistors, internal capacitances can be strung together and that can increase the voltage change

Charge Redistribution - Solutions

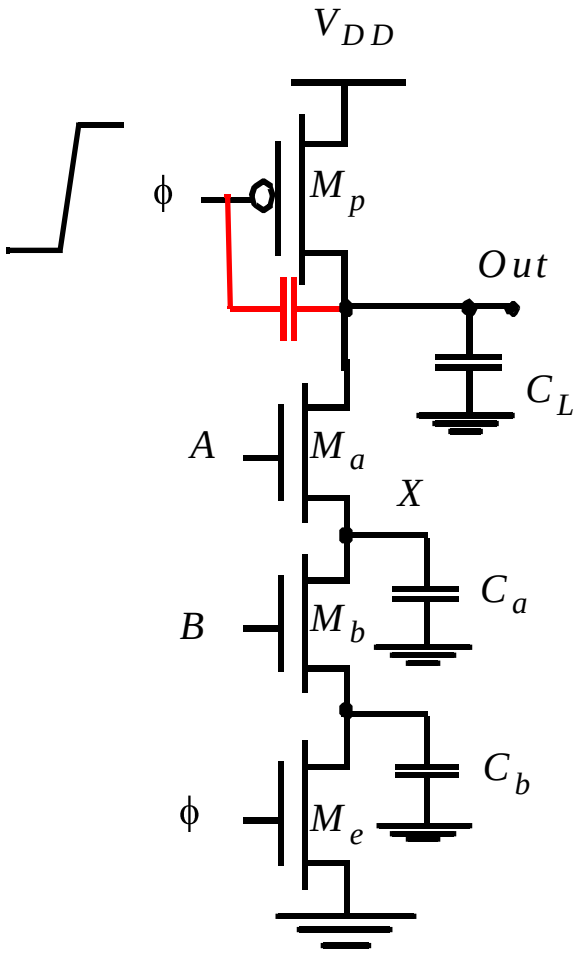


(a) Static bleeder

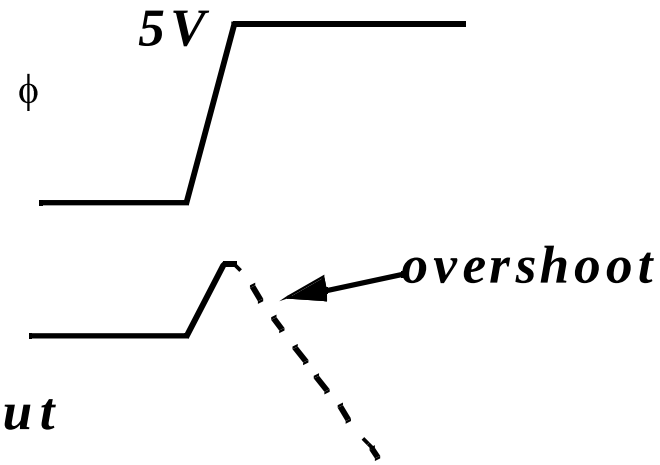


(b) Precharge of internal nodes

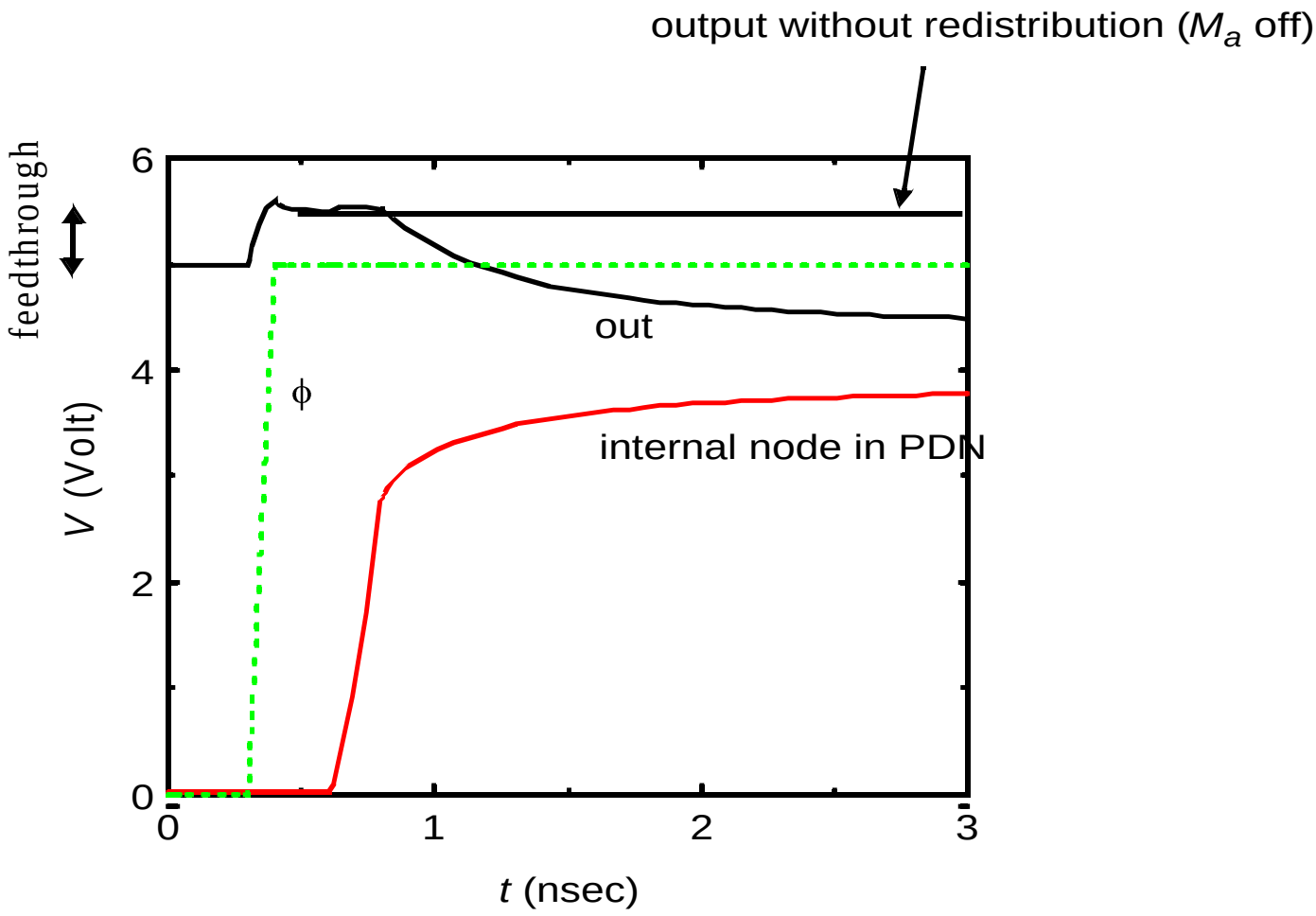
Clock Feedthrough



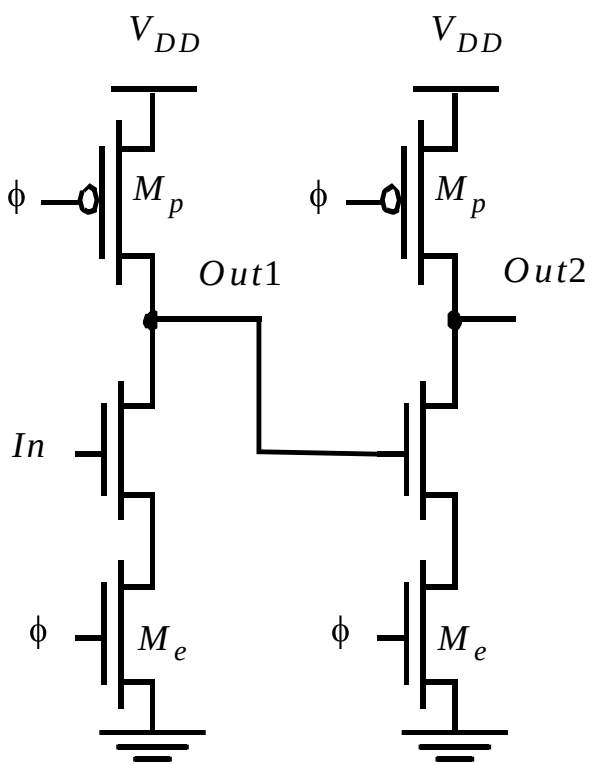
could potentially forward bias the diode



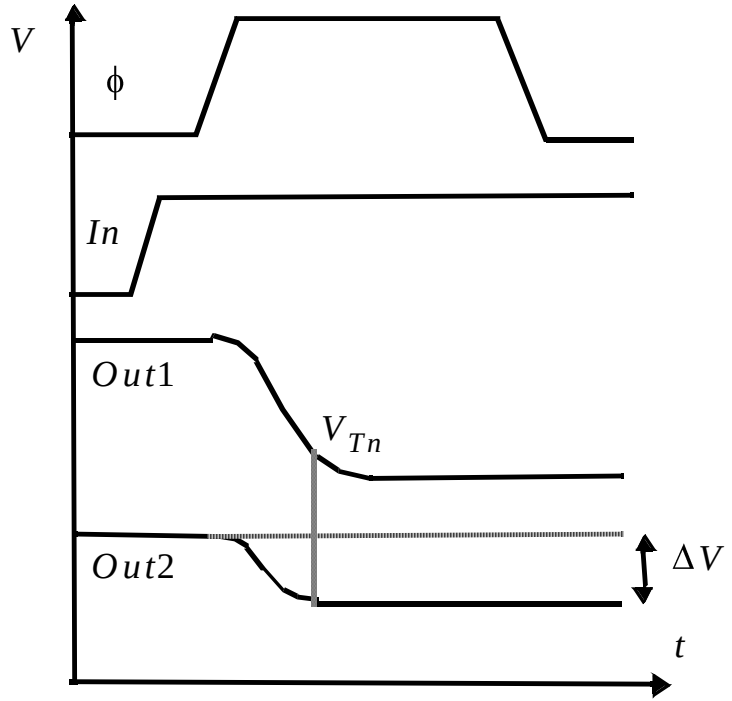
Clock Feedthrough and Charge Sharing



Cascading Dynamic Gates



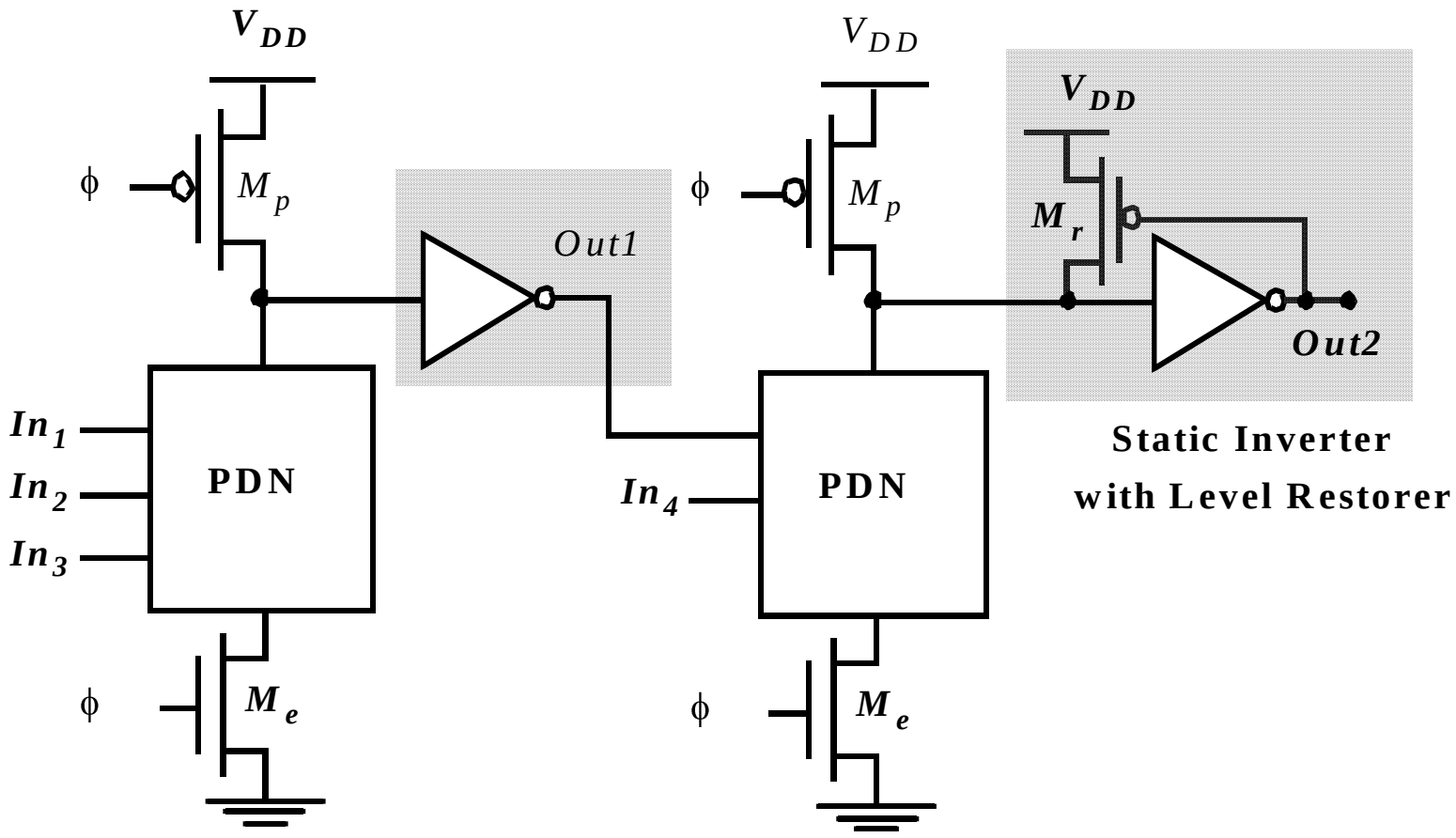
(a)



(b)

Only 0→1 Transitions allowed at inputs!

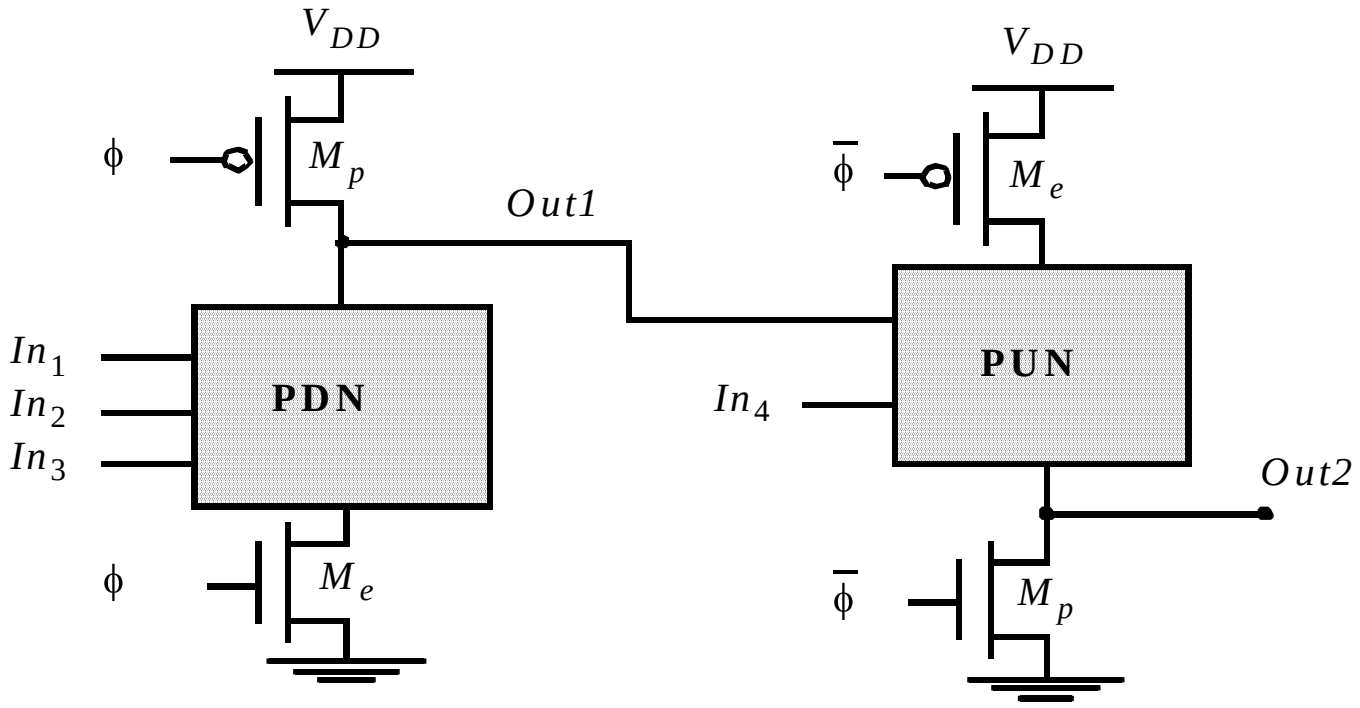
Domino Logic



Domino Logic - Characteristics

- Only non-inverting logic
- Very fast - Only $1 \rightarrow 0$ transitions at input of inverter affects the next Domino
- Static inverter increases noise immunity, increase the size of PMOS to increase V_M
- Proper sizing of inverter to drive the fan-out in optimal way
- Add a level-restoring transistor to overcome charge sharing and charge loss

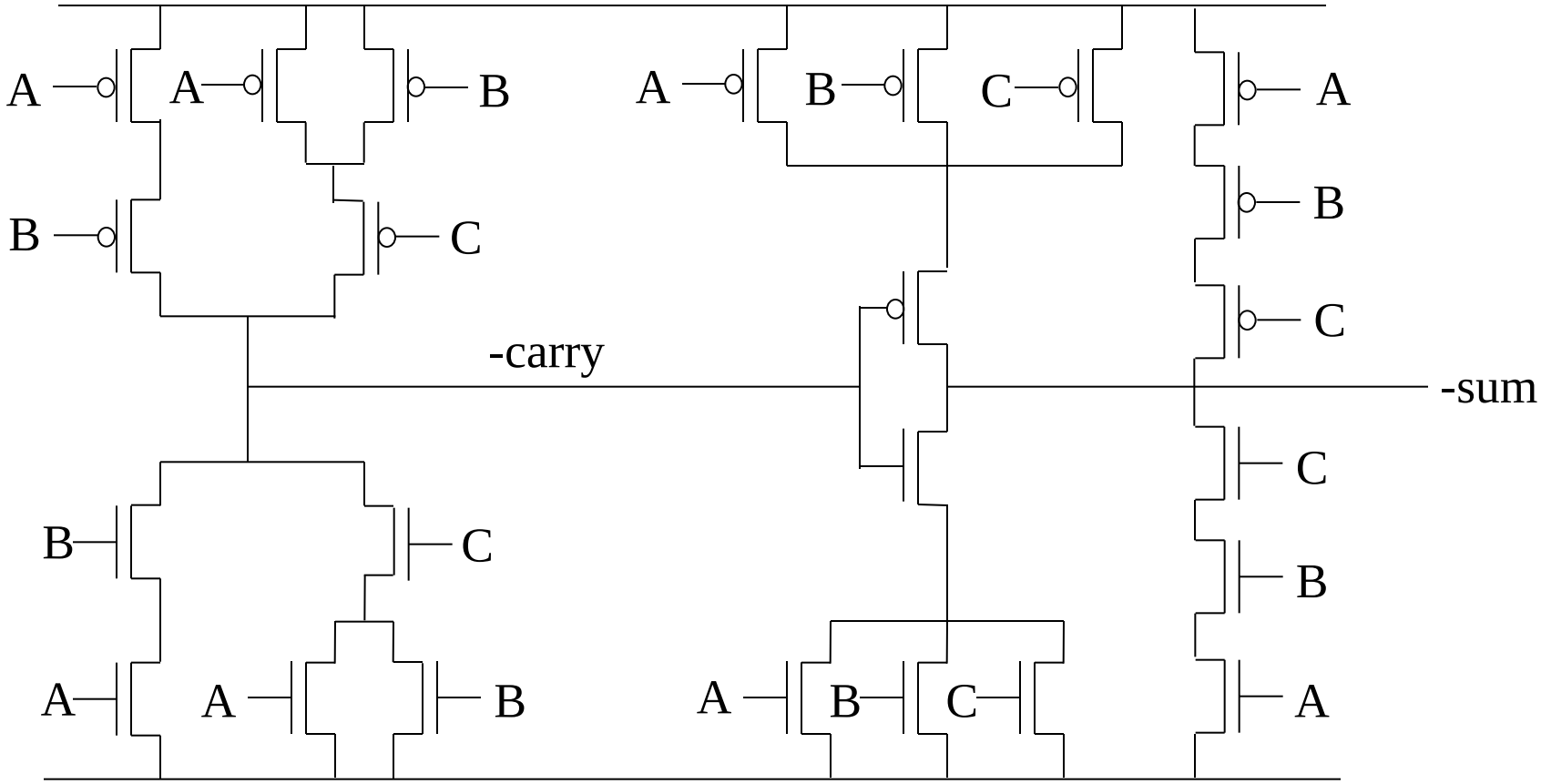
np-CMOS (Zipper CMOS)



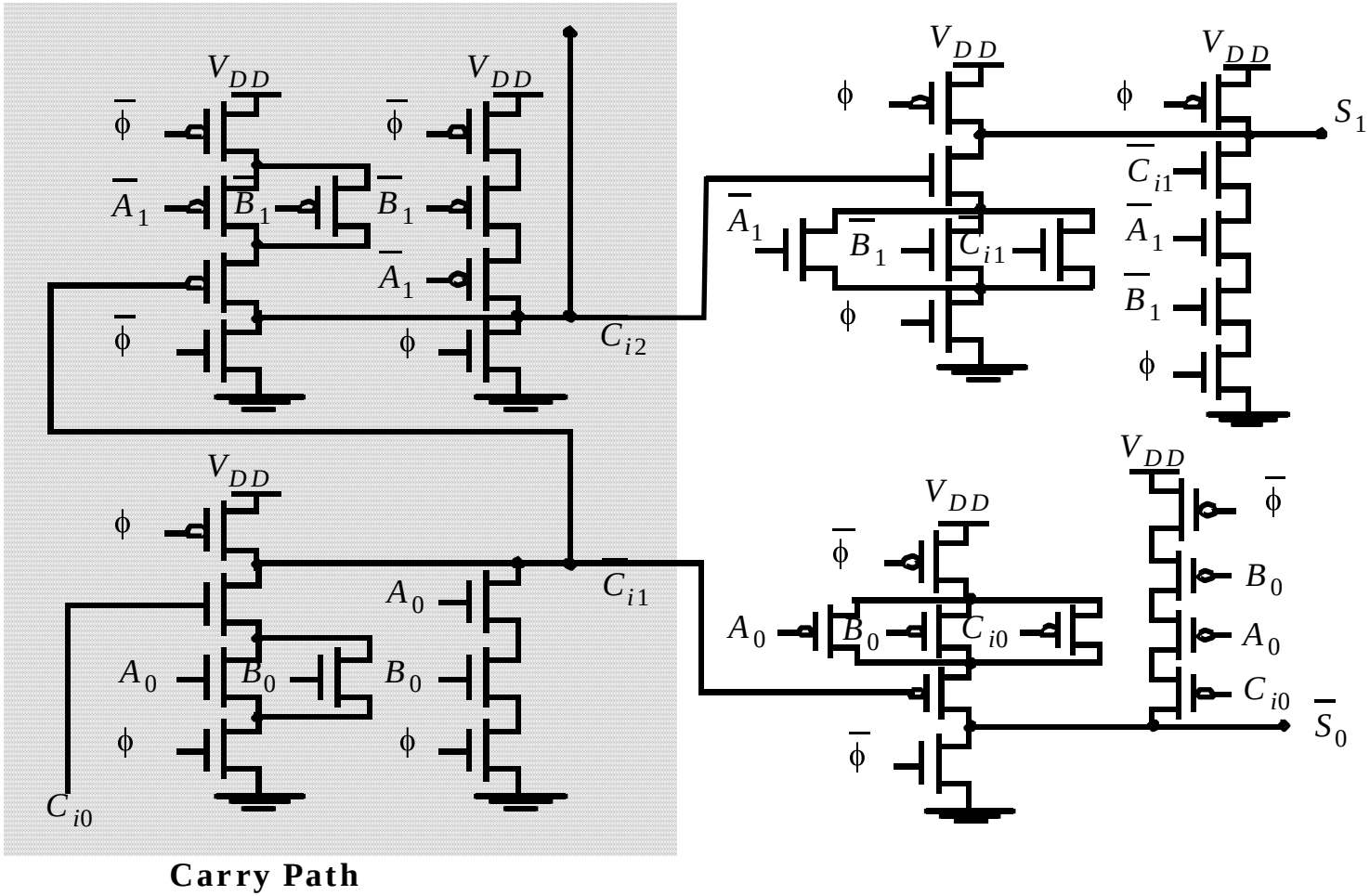
Only 1→0 transitions allowed at inputs of PUN

Reduced noise margins: $NM_H = |V_{tp}|$, $NM_L = |V_{tn}|$

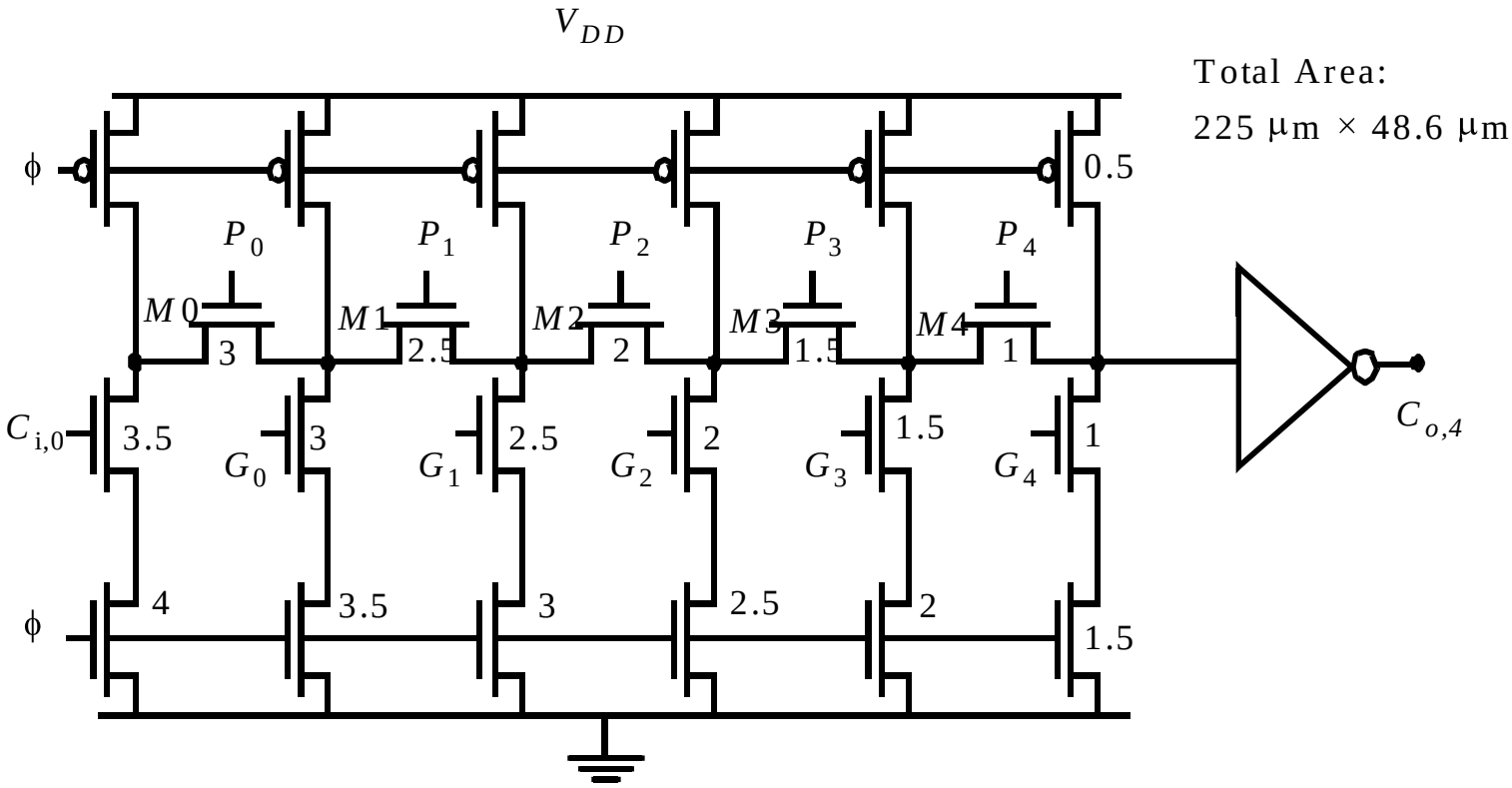
Full Adder Circuit



np CMOS Adder



Manchester Carry Chain Adder



Adder Truth Table

C	A	B	A.B(G)	A+B	A⊕B(P)	SUM	CARRY
0	0	0	0	0	0	0	0
0	0	1	0	1	1	1	0
0	1	0	0	1	1	1	0
0	1	1	1	1	0	0	1
1	0	0	0	0	0	1	0
1	0	1	0	1	1	0	1
1	1	0	0	1	1	0	1
1	1	1	1	1	0	1	1

$$SUM = A \oplus B \oplus C = P \oplus C$$

CARRY = C if P = 1
CARRY = AB if P = 0
CARRY = G + PC

CMOS Circuit Styles - Summary

Style	Ratioed	Static Power	# transistors	Area (μm^2)	Propagation Delay (nsec)
Complementary	No	No	8	533	0.61
Pseudo-NMOS	Yes	Yes	5	288	1.49
CPL	No	No	14	800	0.75
Dynamic (NP)	No	No	6	212	0.37

4-input NAND Gate