

Homework Solutions for ECE 695KR

Solution: 1

ADVANCED VLSI DESIGN

ECE 695KR

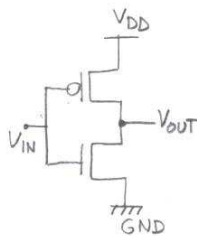
Submitted By: Debabrata Mohapatra

29th Jan 2008 (Late [Tuesday Submission])

Problem: Determine the minimum supply voltage of a CMOS inverter ensuring correct functionality.

Solution: We assume that the transistors are operating in a subthreshold region with the supply voltage below the threshold voltage. In the subthreshold region of operation, the current-voltage relationship is exponential given by

$$I_{DS} = \mu_{eff} C_{ox} \frac{W}{L} (n-1) \left(\frac{kT}{q}\right)^2 e^{\frac{q(V_{GS}-V_T)}{nKT}} \left(1 - e^{-\frac{qV_{DS}}{KT}}\right) \quad [\text{Taur \& Ning}]$$



$$V_{GS}(\text{NMOS}) = V_{IN}$$

$$V_{DS}(\text{NMOS}) = V_{OUT}$$

$$V_{GS}(\text{PMOS}) = (V_{IN} - V_{DD})$$

$$V_{DS}(\text{PMOS}) = V_{OUT} - V_{DD}$$

Equating the subthreshold current through the NMOS and PMOS and assuming symmetrical NMOS and PMOS with identical slope factors $n_{\text{NMOS}} = n_{\text{PMOS}} = n$

$$I_{DS,n} = \mu_{eff} C_{ox} \frac{W}{L} (n-1) \left(\frac{kT}{q}\right)^2 e^{\frac{q(V_{IN}-V_T)}{nKT}} \left(1 - e^{-\frac{qV_{OUT}}{KT}}\right)$$

$$I_{DS,p} = \mu_{eff} C_{ox} \frac{W}{L} (n-1) \left(\frac{kT}{q}\right)^2 e^{\frac{q(V_{DD}-V_{IN}-V_T)}{nKT}} \left(1 - e^{-\frac{q(V_{DD}-V_{OUT})}{KT}}\right)$$

Equating the NMOS and PMOS currents we have

$$e^{\frac{q(V_{IN}-V_T)}{nKT}} \left(1 - e^{-\frac{qV_{OUT}}{KT}}\right) = e^{\frac{q(V_{DD}-V_{IN}-V_T)}{nKT}} \left(1 - e^{-\frac{q(V_{DD}-V_{OUT})}{KT}}\right)$$

$$\Rightarrow e^{\frac{qV_{IN}}{nKT}} \left(1 - e^{-\frac{qV_{OUT}}{KT}}\right) = e^{\frac{q(V_{DD}-V_{IN})}{nKT}} \left(1 - e^{-\frac{q(V_{DD}-V_{OUT})}{KT}}\right)$$

Differentiating both sides wrt V_{IN} we have

$$\text{LHS} = \frac{q}{nKT} e^{\frac{qV_{IN}}{nKT}} \left(1 - e^{-\frac{qV_{OUT}}{KT}}\right) + e^{\frac{qV_{IN}}{nKT}} \cdot \frac{q}{KT} e^{-\frac{qV_{OUT}}{KT}} \cdot \frac{dV_{OUT}}{dV_{IN}}$$

$$RHS = -\frac{q}{nKT} e^{\frac{q(V_{DD}-V_{in})}{nKT}} \left(1 - e^{-\frac{q(V_{DD}-V_{out})}{KT}}\right) - e^{\frac{q(V_{DD}-V_{in})}{nKT}} \cdot \frac{q}{KT} e^{-\frac{q(V_{DD}-V_{out})}{KT}} \cdot \frac{dV_{out}}{dV_{in}}$$

Equating LHS and RHS and substituting $\frac{dV_{out}}{dV_{in}} = -1$ $V_{out} = V_{in} = \frac{V_{DD}}{2}$

$$\begin{aligned} \frac{q}{nKT} e^{\frac{qV_{DD}/2}{nKT}} \left(1 - e^{-\frac{qV_{DD}/2}{KT}}\right) - \frac{q}{KT} e^{\frac{qV_{DD}/2}{nKT}} \cdot e^{-\frac{qV_{DD}/2}{KT}} \\ = -\frac{q}{nKT} e^{\frac{qV_{DD}/2}{nKT}} \left(1 - e^{-\frac{qV_{DD}/2}{KT}}\right) + \frac{q}{KT} e^{\frac{qV_{DD}/2}{nKT}} \cdot e^{-\frac{qV_{DD}/2}{KT}} \end{aligned}$$

$$2 \cdot \frac{q}{nKT} e^{\frac{qV_{DD}/2}{nKT}} \left(1 - e^{-\frac{qV_{DD}/2}{KT}}\right) = 2 \cdot \frac{q}{KT} e^{\frac{qV_{DD}/2}{nKT}} \cdot e^{-\frac{qV_{DD}/2}{KT}}$$

$$\frac{1}{n} \left(1 - e^{-\frac{qV_{DD}/2}{KT}}\right) = e^{-\frac{qV_{DD}/2}{KT}}$$

$$(n+1) e^{-\frac{qV_{DD}/2}{KT}} = 1$$

$$e^{\frac{qV_{DD}/2}{KT}} = (n+1)$$

$$\Rightarrow V_{DD, \min} = \frac{2KT}{q} \ln(1+n)$$

Since the value of slope factor n varies between 1 and 2

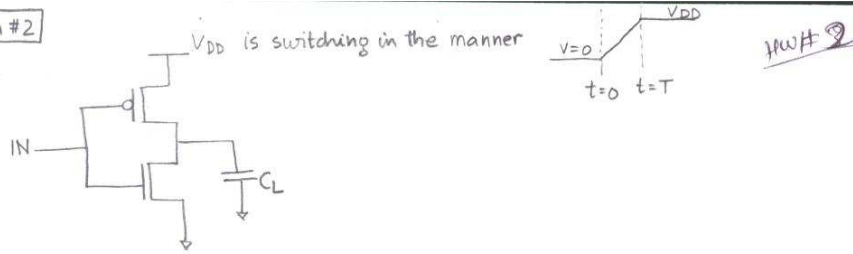
$$V_{DD, \min} \text{ (theoretical)} = \frac{2KT}{q} \ln 2$$

Assuming $\frac{kT}{q} = 26 \text{ mV}$ at room temperature

$$V_{DD, \min} = (2 \times 26 \times 0.693) \text{ mV} = \boxed{36.036 \text{ mV}}$$

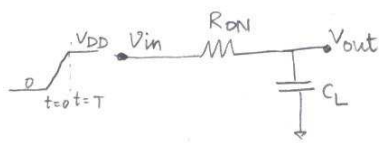
Solution:2

Problem #2



Find out the energy dissipation in the cases when (a) $T=0$ (b) $T=\infty$

The equivalent circuit model for the above problem can be represented as follows.



Let us assume the ON resistance of the PMOS to be a constant equal to R_{ON} .

Using the KCL equation we have

$$\frac{V_{in} - V_{out}}{R_{ON}} = C_L \frac{dV_{out}}{dt}$$

$$V_{in} = \begin{cases} 0, & t < 0 \\ \frac{t}{T} V_{DD}, & 0 \leq t \leq T \\ V_{DD}, & t > T \end{cases}$$

Using the expression for V_{in} , we have for V_{out}

$$\frac{dV_{out}}{dt} + \frac{1}{R_{ON}C_L} V_{out} = \frac{V_{in}}{R_{ON}C_L}$$

Let us call $R_{ON}C_L = \tau$, we have a first order differential equation

$$\frac{dV_{out}}{dt} + \frac{V_{out}(t)}{\tau} = \frac{V_{in}(t)}{\tau}$$

for $t < 0$ $V_{out} = 0$
for $t > T$ $\frac{dV_{out}}{dt} + \frac{V_{out}}{\tau} = \frac{V_{DD}}{\tau}$

General solution of a differential equation of the form

$$\frac{dy}{dx} + p(x)y = q(x) \quad \text{is given by} \quad y(x) = \frac{\int u(x)q(x) dx + C}{u(x)}$$

$$u(x) = \exp\left(\int p(x) dx\right)$$

$$u(x) = \exp\left(\int_0^t \frac{1}{\tau} dt\right) = e^{t/\tau}$$

$$V_{out}(t) = \frac{\int e^{t/\tau} \cdot \frac{t}{T} V_{DD} dt + C}{e^{t/\tau}} = \frac{\frac{V_{DD}}{T} \left[\tau t e^{t/\tau} - \tau^2 e^{t/\tau} \right] + C}{e^{t/\tau}}$$

$$= \frac{V_{DD}}{T} (\tau t - \tau^2) + C e^{-t/\tau}$$

from the boundary condition $V_{out}(0) = 0 \Rightarrow C = \frac{V_{DD}\tau}{T}$

$$\begin{aligned}
 V_{out}(t) &= 0 \quad t < 0 \\
 &= \frac{V_{DD}}{T}(t-\tau) + \frac{V_{DD}\tau}{T} e^{-t/\tau} \quad 0 \leq t < T \\
 &= V_{DD} + \frac{V_{DD}\tau}{T}(1 - e^{T/\tau}) e^{-t/\tau} \quad t > T
 \end{aligned}$$

$$\begin{aligned}
 V_{out}(t) &= \int e^{t/\tau} \frac{V_{DD}}{T} dt + c \\
 &= \frac{V_{DD} e^{t/\tau} + c}{e^{t/\tau}} \\
 &= V_{DD} + c e^{-t/\tau}
 \end{aligned}$$

$$E_{dissipated} = \int_0^{\infty} \frac{V_R^2(t)}{R_{ON}} dt = \int_0^T \frac{V_R^2(t)}{R_{ON}} dt + \int_T^{\infty} \frac{V_R^2(t)}{R_{ON}} dt$$

$$\begin{aligned}
 &V_{DD} \left(\frac{T-\tau}{T} \right) + \frac{V_{DD}\tau}{T} e^{-T/\tau} \\
 &= V_{DD} + c e^{-T/\tau}
 \end{aligned}$$

$$\text{1st term in the integral} = \int_0^T \frac{(V_{in} - V_{out})^2}{R_{ON}} dt$$

$$\frac{V_{DD}\tau}{T} [-1 + e^{-T/\tau}] e^{T/\tau} = c$$

$$c = (1 - e^{T/\tau}) \frac{V_{DD}\tau}{T}$$

$$\begin{aligned}
 RHS &= \int_0^T \frac{\left(\frac{V_{DD}}{T} \tau - \frac{V_{DD}\tau}{T} e^{-t/\tau} \right)^2}{R_{ON}} dt = \frac{\left(\frac{V_{DD}\tau}{T} \right)^2}{R_{ON}} \left[\int_0^T (1 + e^{-2t/\tau} - 2e^{-t/\tau}) dt \right]
 \end{aligned}$$

$$= \frac{V_{DD}^2 \tau^2}{T^2 R_{ON}} \left[T - \frac{\tau}{2} (e^{-2T/\tau} - 1) + 2\tau (e^{-T/\tau} - 1) \right]$$

$$\text{2nd term in the integral: } \int_T^{\infty} \frac{\left[(e^{t/\tau} - 1) \frac{V_{DD}\tau}{T} e^{-t/\tau} \right]^2}{R_{ON}} dt = \frac{\left[\frac{V_{DD}\tau}{T} (e^{T/\tau} - 1) \right]^2}{R_{ON}} \frac{\tau}{2} \left[e^{-T/\tau} \right]$$

$$E_{diss} = \frac{V_{DD}^2 R_{ON}^2 C^2}{T^2 R_{ON}} \left[T - \frac{RC}{2} e^{-2T/RC} + \frac{RC}{2} + 2RC e^{-T/RC} - 2RC \right] + \frac{V_{DD}^2 R_{ON}^2 C^2}{T^2 R_{ON}} \cdot \frac{R_{ON} C}{2}$$

$$\begin{aligned}
 E_{diss} &= \frac{V_{DD}^2 C}{T^2} (R_{ON} C) \left[T - \frac{3R_{ON}C}{2} - \frac{R_{ON}C}{2} e^{-2T/R_{ON}C} + 2R_{ON}C e^{-T/R_{ON}C} \right] \left\{ 1 + e^{-2T/R_{ON}C} - 2e^{-T/R_{ON}C} \right\} \\
 &\quad + \frac{R_{ON}C}{2} + \frac{R_{ON}C}{2} e^{-2T/R_{ON}C} - R_{ON}C e^{-T/R_{ON}C}
 \end{aligned}$$

$$= \frac{V_{DD}^2 C}{T^2} (R_{ON} C) \left[T - R_{ON}C + R_{ON}C e^{-T/R_{ON}C} \right]$$

$$= CV_{DD}^2 \left(\frac{R_{ON}C}{T} \right) \left[1 - \frac{R_{ON}C}{T} (1 - e^{-T/R_{ON}C}) \right]$$

$$\text{For } T \rightarrow \infty \Rightarrow T \gg R_{ON}C \quad E_{diss} \approx CV_{DD}^2 \left[\frac{R_{ON}C}{T} \right] \approx 0 \quad \text{for } T \rightarrow \infty$$

$$\text{For } T \rightarrow \infty \text{ or } T \ll R_{ON}C \quad E_{diss} \approx CV_{DD}^2 \frac{R_{ON}C}{T} \left[1 - \frac{R_{ON}C}{T} \left\{ 1 - \frac{T}{R_{ON}C} + \frac{T^2}{2R_{ON}^2 C^2} \right\} \right]$$

$$\approx CV_{DD}^2 \frac{R_{ON}C}{T} \cdot \frac{T}{2R_{ON}C} \approx \frac{1}{2} CV_{DD}^2 \quad \text{for } T \rightarrow 0$$

Solution:3

HOMWORK #2
ECE 695KR
Debabrata Mohapatra
Date of Submission: 6th Feb 2008

HW #3

- ① Derivation of expression for subthreshold current in a CMOS transistor.

Subthreshold current expression

The electron concentration at any point (x, y) is given by

$$n(x, y) = \frac{n_i^2}{N_A} e^{q(\psi - V)/kT} \quad \text{and the electric field is given by}$$

$$E_x^2(x, y) = \left(\frac{d\psi}{dx}\right)^2 = \frac{2kTNa}{\epsilon_{si}} \left[\left(e^{-q\psi/kT} + \frac{q\psi}{kT} - 1 \right) + \frac{n_i^2}{N_A^2} \left(e^{-q\psi/kT} \left[e^{2q\psi/kT} - 1 \right] - \frac{q\psi}{kT} \right) \right]$$

We apply the Gauss's law to obtain the total charge density in silicon

$$-Q_s = \epsilon_s E_s = \sqrt{2\epsilon_{si}kTNa} \left[\frac{q\psi_s}{kT} + \frac{n_i^2}{N_A^2} e^{q(\psi_s - V)/kT} \right]^{1/2}$$

We only keep two significant terms in the square bracket. In weak inversion, the second term in the bracket arising from the inversion charge density is much less than the first term from the depletion charge density

$$-Q_s = \sqrt{2\epsilon_{si}kTNa} \cdot \left(\frac{q\psi_s}{kT}\right)^{1/2} \left[1 + \frac{n_i^2}{N_A^2} \cdot \frac{kT}{q\psi_s} e^{q(\psi_s - V)/kT} \right]^{1/2}$$

Using the approximation $(1+x)^n = 1+nx$

$$-Q_s = \sqrt{2\epsilon_{si}kTNa} \left(\frac{q\psi_s}{kT}\right)^{1/2} \left[1 + \frac{n_i^2}{2N_A^2} \cdot \frac{kT}{q\psi_s} e^{q(\psi_s - V)/kT} \right]$$

The zeroth order term gives the depletion charge density while the first order term gives the inversion charge density

$$-Q_i \text{ (inversion charge density)} = \sqrt{\frac{\epsilon_{si}qNa}{2\psi_s}} \left(\frac{kT}{q}\right) \left(\frac{n_i}{N_A}\right)^2 e^{q(\psi_s - V)/kT}$$

The surface potential ψ_s is related to gate voltage by the relation

$$V_g = V_{fb} + \psi_s + \frac{\sqrt{2\epsilon_{si}kTNa}}{C_{ox}} \left[\frac{q\psi_s}{kT} + \frac{n_i^2}{N_A^2} e^{q(\psi_s - V)/kT} \right]^{1/2}$$

Since the inversion charge density is small, ψ_s can be considered only as a function of V_g only independent of V .

From the expression for the drain to source current we have

$$I_{DS} = \mu_{\text{eff}} \frac{W}{L} \int_0^{V_{DS}} (-Q_i[V]) dV$$

$$I_{DS} = \mu_{\text{eff}} \frac{W}{L} \int_0^{V_{DS}} \sqrt{\frac{\epsilon_{si} q N_a}{2\psi_s}} \left(\frac{kT}{q}\right) \left(\frac{n_i}{N_a}\right)^2 e^{q\psi_s/kT} \cdot e^{-qV/kT} dV$$

$$= \mu_{\text{eff}} \frac{W}{L} \sqrt{\frac{\epsilon_{si} q N_a}{2\psi_s}} \left(\frac{kT}{q}\right) \left(\frac{n_i}{N_a}\right)^2 e^{q\psi_s/kT} \left[\frac{kT}{q} (1 - e^{-qV_{DS}/kT})\right]$$

$$\Rightarrow I_{DS} = \mu_{\text{eff}} \frac{W}{L} \sqrt{\frac{\epsilon_{si} q N_a}{2\psi_s}} \left(\frac{kT}{q}\right)^2 \left(\frac{n_i}{N_a}\right)^2 e^{q\psi_s/kT} [1 - e^{-qV_{DS}/kT}]$$

Since ψ_s can be expressed in terms of V_g where only the depletion charge term is valid

$$V_g = V_{fb} + \psi_s + \frac{\sqrt{2\epsilon_{si} q N_a \psi_s}}{C_{ox}}$$

For further simplification of the result, we consider ψ_s to be slightly deviated from the threshold value, $2\psi_B$. In other words, we assume that $|\psi_s - 2\psi_B| \ll 2\psi_B$ and expand the square root term around $\psi_s = 2\psi_B$

$$V_g = V_{fb} + 2\psi_B + \frac{\sqrt{4\epsilon_{si} q N_a \psi_B}}{C_{ox}} + \left(1 + \frac{\sqrt{\epsilon_{si} q N_a / 4\psi_B}}{C_{ox}}\right) (\psi_s - 2\psi_B)$$

$f(x) = x_0 + f'(x_0)(x - x_0)$
 $\sqrt{x} = x_0 + \frac{1}{2\sqrt{x_0}}(x - x_0)$

Using the relationship $V_{th} = V_{fb} + 2\psi_B + \frac{\sqrt{4\epsilon_{si} q N_a \psi_B}}{C_{ox}}$

$$m = \text{subthreshold slope} = 1 + \frac{\sqrt{\epsilon_{si} q N_a / 4\psi_B}}{C_{ox}}$$

$$V_g = V_{th} + m(\psi_s - 2\psi_B) \quad \psi_s = \left(\frac{V_{gs} - V_{th}}{m}\right) + 2\psi_B \quad e^{\frac{2q\psi_B}{kT}}$$

Substituting in the equation for I_{DS} we get

$$I_{DS} = \mu_{\text{eff}} \frac{W}{L} \sqrt{\frac{\epsilon_{si} q N_a}{4\psi_B}} \left(\frac{kT}{q}\right)^2 e^{q(V_{gs} - V_{th})/m kT} (1 - e^{-qV_{DS}/kT})$$

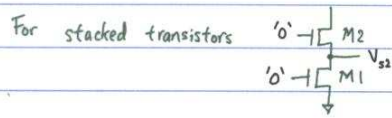
$$I_{DS} = \mu_{\text{eff}} C_{ox} \frac{W}{L} (m-1) \left(\frac{kT}{q}\right)^2 e^{q(V_{gs} - V_{th})/m kT} (1 - e^{-qV_{DS}/kT})$$

Solution:4

EE695K HW4 XUANYAO FONG

Note Title

Investigate the effect of scaling on DIBL in stacked transistors.



Sub-threshold current:

$$I_{ds} = \mu_{eff} C_{ox} \left(\frac{W}{L}\right) (m-1) \left(\frac{kT}{q}\right) e^{\frac{(V_g - V_t)/kT}{m}} (1 - e^{-V_{ds}/kT})$$

DIBL:

$$\Delta V_t = \frac{24 t_{ox}}{W_{dm}} \sqrt{\frac{q}{\epsilon_0 \epsilon_r}} \sqrt{V_{bi} (V_{bi} + V_{ds})} e^{-\pi L / 2 (W_{dm} + 3 t_{ox})}$$

Without stacking, the leakage due to DIBL will increase exponentially with scaling because

- 1) ΔV_t increases exponentially with L
- 2) I_{ds} in sub-threshold increases exponentially with ΔV_t

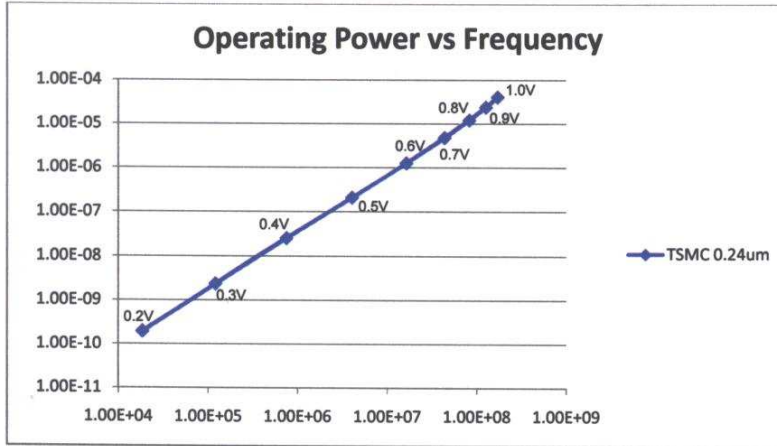
With stacking, the effect of DIBL under scaling is decreased because

- 1) ΔV_t increases exponentially with L , but because $V_{d1} = V_{s2}$ is now lower than V_{ds} of the unstacked transistor, and $\Delta V_t \sim \sqrt{V_{ds}}$, I_{ds} of the footer transistor in subthreshold is decreased
- 2) Since $V_{s2} \neq 0$, V_{ds2} is smaller and $V_{gs2} < 0$. So $I_{ds2} \sim e^{(V_{gs2} - V_{t2})/kT}$ and ΔV_{t2} is reduced, the subthreshold current of M2 is also reduced.

Therefore, in stacking, reducing L will have lower DIBL.

Solution:5

The following is a log-log plot of the operating power versus operating frequency for a 10-stage fanout of 4 inverter chain under voltage scaling. The technology used is the TSMC 0.24um.

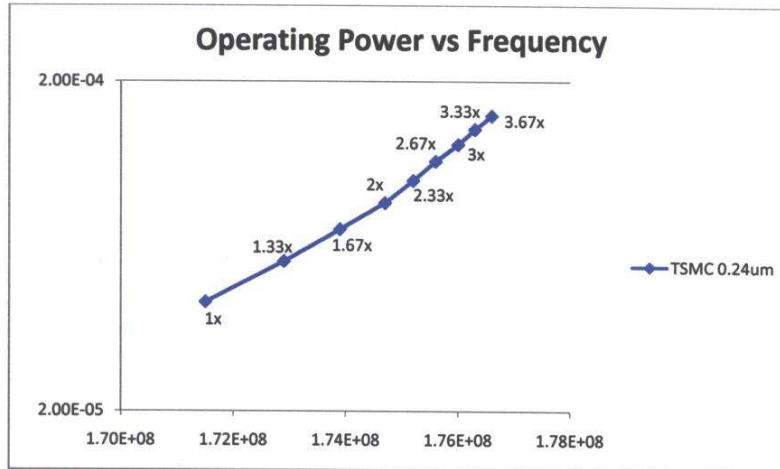


If we want to scale the voltage down and maintain the operating frequency by parallel processing, the following table provides a table of how many parallel units we need and the associated power dissipation, using the performance of a 1V supply inverter chain as the target.

Supply	Units	Power	Freq
0.2	10276	1.82E-06	1.72E+08
0.3	1624	3.37E-06	1.72E+08
0.4	263	5.87E-06	1.72E+08
0.5	48	9.26E-06	1.72E+08
0.6	12	1.39E-05	1.72E+08
0.7	4	1.97E-05	1.72E+08
0.8	3	2.65E-05	1.72E+08
0.9	2	3.42E-05	1.72E+08
1	1	4.28E-05	1.72E+08

As can be seen, there is a diminishing returns in terms of increasing the number of inverter chains to lower the power consumption at iso-frequency. Going from a supply of 1V to 0.2 V gets an order of magnitude power reduction better than going from 1V to 0.7V but the number of units needed is nearly 2500x difference. The "sweet spot" is between 0.6V and 0.8V. Going from 0.8V to 0.7V, we need 33.33% increase in area for power reduction of more than 20% but going from 0.7V to 0.6V, the area increase is 200% for a power reduction of about 60%!

The following figure shows the impact of sizing on the power versus frequency plot of the same inverter chain at 1V supply voltage. An inverter of 1x is the same size as that from the previous analysis and the inverter's beta ratio is maintained for each size increase.



Power increases almost exponentially with each size increase but the frequency increase is worse than linear. Thus, for this exercise, sizing should be used to achieve the initial frequency target and then voltage scaling is used to meet the power consumption specifications. If this methodology fails the area target for this technology node, then the overall specifications will have to be revised by either increasing power consumption and maintaining the frequency target, or lowering the frequency target while maintaining power consumption.