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Effects of forming gas anneal on ultrathin InGaAs nanowire metal-oxide-semiconductor field-effect transistors

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InGaAs gate-all-around metal-oxide-semiconductor field-effect transistors (MOSFETs) with 6 nm nanowire thickness have been experimentally demonstrated at sub-80 nm channel length. The effects of forming gas anneal (FGA) on the performance of these devices have been systematically studied. The 30 min 400 °C FGA (4% H_2/96% N_2) is found to improve the quality of the Al_2O_3/InGaAs interface, resulting in a subthreshold slope reduction over 20 mV/dec (from 117 mV/dec in average to 93 mV/dec). Moreover, the improvement of interface quality also has positive impact on the on-state device performance. A scaling metrics study has been carried out for FGA treated devices with channel lengths down to 20 nm, indicating excellent gate electrostatic control. With the FGA passivation and the ultra-thin nanowire structure, InGaAs MOSFETs are promising for future logic applications. © *2013 American Institute of Physics*. [http://dx.doi.org/10.1063/1.4794846]

Recently, InGaAs has been considered as one of the promising channel materials for CMOS beyond the 10 nm technology node because of its large electron mobility. 3D InGaAs devices such as fin field-effect transistors and the gate-all-around (GAA) metal-oxide-semiconductor field effect transistors have been shown to offer large drive current and excellent immunity to short channel effects (SCE).[1–6] In particular, the GAA MOSFETs provide the best gate electrostatic control and therefore the ultimate channel length (L_{ch}) scalability. It is known that better SCE control can be obtained by reducing the nanowire size, enabling further L_{ch} scaling. InGaAs nanowires fabricated by top-down technology with sub-10 nm wire dimension, either nanowire width (W_{NW}) or thickness (T_{NW}), have not been reported. On the other hand, the interface quality is one of the critical problems for III-V MOSFETs. Superior interface quality is required for optimizing both the on-state and off-state performance of MOSFETs. Al_2O_3 is commonly used as the gate insulator for InGaAs MOSFETs for the relatively low interface trap density (D_{it}). Various passivation methods have been developed and optimized on the Al_2O_3/InGaAs interface such as $(NH_4)_2S$ passivation,[7,8] surface nitridation,[9,10] and phosphor passivation.[11] Forming gas anneal is another common post metallization treatment used to improve the interface quality of Al_2O_3/InGaAs. Interface traps, oxide charges, and border traps reduction after FGA have been reported by CV methods.[12,13] Recent study of effects of FGA on planar devices shows that on-state performances such as drive current (I_{on}) and transconductance (g_m) are improved after FGA.[14] However, the impacts of FGA have not been studied in short channel devices with GAA structure. The compatibility between FGA and other passivation methods have not been studied either.

In this letter, 20–80 nm L_{ch} short channel $In_{0.65}Ga_{0.35}As$ GAA MOSFETs with 6 nm T_{NW} and 30 nm W_{NW} have been fabricated with or without FGA treatment. FGA offers improvement in the on-state and off-state performance of the devices. The reduction of subthreshold slope (SS) and the increase of g_m and I_{on} verify the improvement of the interface quality. The average interface trap density drops by 40% on average after FGA. Moreover, SS and drain induced barrier lowering (DIBL) do not increase when L_{ch} scales from 80 nm down to 20 nm, demonstrating the excellent scalability of InGaAs GAA MOSFET with sub-10 nm nanowire dimension. It is also found that the 30 min 400 °C FGA passivation is fully compatible with the $(NH_4)_2S$ passivation. The interface trap density is significantly improved in devices with $(NH_4)_2S$ passivation and FGA together than those with $(NH_4)_2S$ passivation only.

Figure 1(a) shows the schematic diagram of the InGaAs GAA MOSFET fabricated in this work and the cross sectional transmission electron microscope (TEM) image of an InGaAs nanowire with 6 nm T_{NW}. The fabrication process flow of the devices is shown in Figure 1(b). The top-down fabrication process is similar to that demonstrated in Ref. 4. The starting material is a 2 in. semi-insulating InP substrate. 100 nm undoped $In_{0.52}Al_{0.48}As$ etch stop layer, 80 nm undoped InP layer, 10 nm undoped $In_{0.65}Ga_{0.35}As$ channel layer, and 2 nm undoped InP layer were sequentially grown by molecular beam epitaxy. Source/drain implantation was performed at an energy of 20 keV and a dose of 10^{14} cm^{-2}, followed by dopant activation at 600 °C for 15 s in nitrogen ambient. After fabricating nanowire fins using BCl_3/Ar reactive ion etching, HCl based release process was performed to create the free-standing InGaAs nanowires. Before the gate

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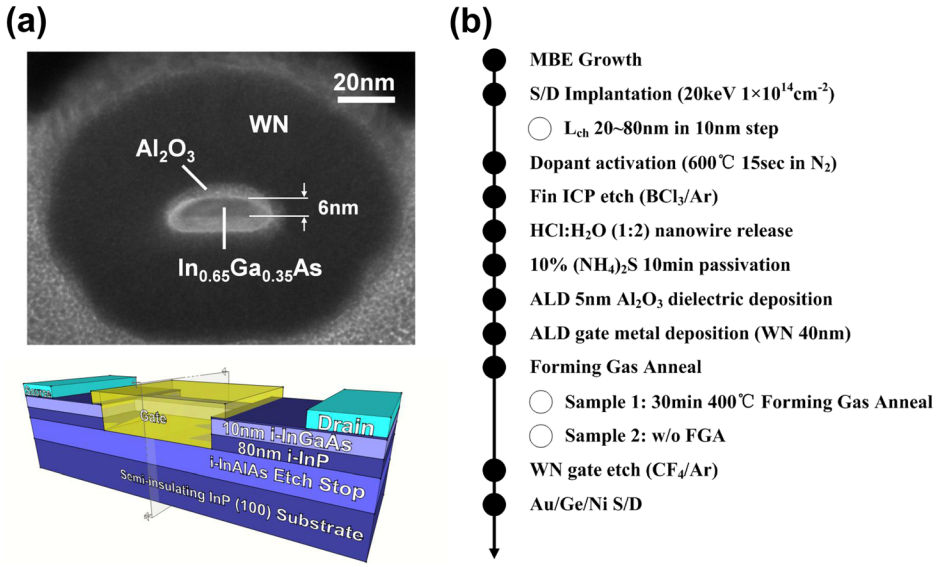

FIG. 1. (a) Cross sectional TEM image and schematic diagram of an InGaAs GAA MOSFET with $T_{NW} = 6$ nm. (b) Fabrication process flow of the InGaAs GAA MOSFETs.

stack deposition, 10% $(NH_4)_2S$ passivation was performed. The gate dielectric is 5 nm atomic layer deposited (ALD) Al_2O_3 to study the effect of FGA on Al_2O_3/InGaAs interface while maintaining a low gate leakage current. Following ALD WN gate metallization process, the devices are divided into two groups. One was treated with 30 min 400 °C FGA (4% H_2/96% N_2) and the other served as the control group. After gate etch process, source/drain contacts were formed with Au/Ge/Ni alloy. Each device has four nanowires fabricated in parallel. All patterns were defined by a Vistec UHR electron beam lithography system.

Figures 2(a) and 2(a) show the I-V characteristics comparison between two typical devices with $L_{ch} = 20$ nm, $W_{NW} = 30$ nm with and without 30 min 400 °C FGA. Device with FGA shows an 89% increase in on-current (I_{on}) at $V_{ds} = V_{gs} - V_T = 0.8$ V and the SS of device with FGA is 93 mV/dec, which is 23 mV/dec smaller than that of device without FGA. Maximum g_m of device with FGA is also found to be 59% larger than that of control device without FGA. After being normalized by the perimeter of the nanowire, the best I_{on} and peak g_m at $V_{ds} = V_{gs} - V_T = 1$ V is 505 μA/μm and 665 μS/um, respectively. The saturation-currents of devices in this work are lower compared to InGaAs GAA MOSFETs with 30 nm T_{NW} and the same W_{NW} and L_{ch}.[4] The reduction in drive current is attributed to the larger impact of surface roughness which decreases the channel mobility. Details of the transport properties of the ultra-thin nanowires are under investigation.

To study the effects of FGA, the average SS, threshold voltage V_T, and I_{on} of InGaAs GAA MOSFETs with L_{ch} between 20 nm and 80 nm have been extracted. Figures 3(a), 3(b), and 4(a) show the statistical data of SS, V_T and I_{on} for devices with and without FGA. As shown in Figure 3(a), devices with FGA has a much lower SS for all channel lengths compared to the control devices without FGA. The average of SS shows an obvious reduction from about 117 mV/dec to 93 mV/dec. The improvement of off-state performance indicates that FGA can reduce the interface traps within the bandgap. The threshold voltage is found to increase with FGA treatment, as shown in Figure 3(b). It is known that traps at the Al_2O_3/InGaAs interface are mostly donor type. The reduction of donor interface trap does not have a significant impact on the threshold voltage while the reduction of acceptor trap leads to negative V_T shift.[15] Thus, the positive shift of V_T in this study is attributed to the reduction of positive fixed charge density and the ion charge density in oxide layer. Figure 4(a) shows the comparison of on-current. I_{on} is found to increase by 14% on average with

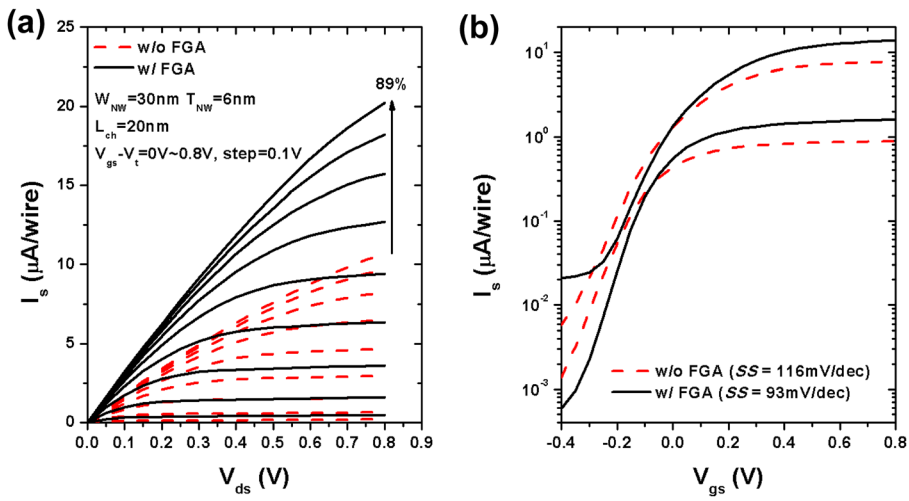

FIG. 2. (a) Output and (b) transfer characteristics of two typical InGaAs GAA MOSFETs with $L_{ch} = 20$ nm, $W_{NW} = 30$ nm, and $T_{NW} = 6$ nm with and without FGA treatment. Due to the significant reverse junction leakage current, I_S is presented instead of I_D.

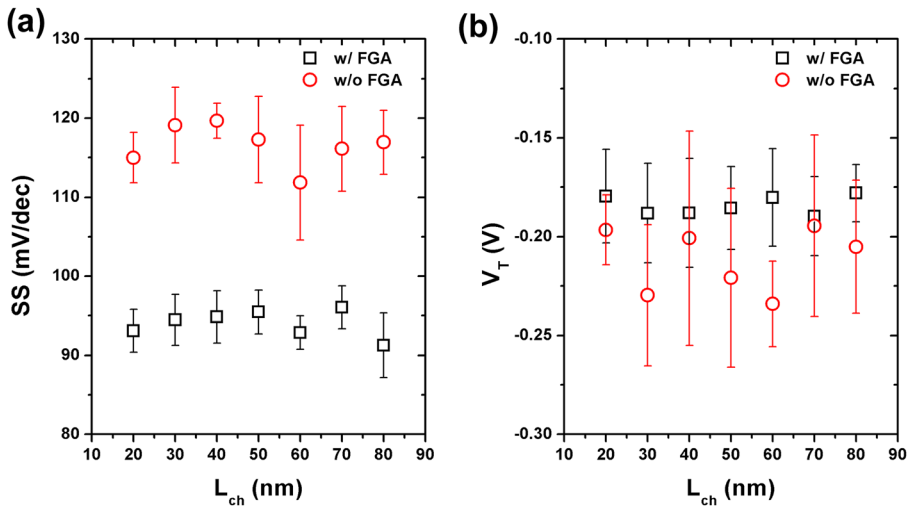

FIG. 3. (a) SS and (b) V_T of these devices with $W_{NW} = 30\,nm$ and $T_{NW} = 6\,nm$ versus L_{ch}. With FGA and their control devices are in comparison. Each data point represents 5–10 measured devices. V_T is extracted from linear extrapolation at $V_{ds} = 50\,mV$.

FGA, accompanied by 25% g_m enhancement (not shown). One origin for the I_{on} enhancement is the reduction of interface trap density near the conduction band edge. Another origin is that mobility is improved due to the reduction in Coulomb scattering as a result of oxide charge reduction.

Interface trap density of the devices are extracted with the approximate formula $SS = 60(1 + (qD_{it} + C_D)/C_{ox})\,mV/dec$,[16] where C_D is the depletion capacitance and C_{ox} is the gate capacitance. The depletion capacitance can be neglected for its weak impact on SS. Devices in Ref. 4 show the minimum SS of 63 mV/dec, which indicates C_D contribute to at most 3 mV/dec to SS in the InGaAs GAA MOSFET structure. As the device structure is similar as Ref. 4, C_D is also negligible in this work. Thus, subthreshold swing can be written as $SS = 60(1 + qD_{it}/C_{ox})\,mV/dec$. It is estimated that the upper limit of mid-gap D_{it} is reduced by 40% percent with FGA, indicating that FGA can improve the interface quality of the Al_2O_3/InGaAs interface.

Another interesting phenomenon found in this work is the standard deviation (STD) comparison for SS, V_T, and I_{on}. The SS STD and V_T STD of devices with FGA are smaller than the control devices without FGA, while the I_{on} STD and g_m STD of devices with FGA are larger than devices without FGA. The STD of SS and V_T reduces with FGA treatment because of the improvement of the interface quality as shown earlier. However, the larger on-state STD seems unexpected and contradictory to the D_{it} reduction. The most possible reason is that the ohmic contact of the devices with FGA is worse than those without FGA, which can in turn increase on-state variation. To confirm this hypothesis, external resistance (R_{ext}) is extracted by linear fitting R_{tot} and $1/(V_{gs} - V_T - V_{ds}/2)$ at small V_{ds}.[17] As shown in Figure 4(b), both average value of R_{ext} and STD of R_{ext} of devices with FGA is much larger than devices without FGA. The larger R_{ext} of devices with FGA suggests that the intrinsic current improvement of devices with FGA is even larger than that shown in Figure 4(a). Although the exact reason for the increased R_{ext} after FGA has not been clearly understood, it is likely that the Au/Ge/Ni alloy based ohmic contact is sensitive to FGA treatment. More advanced source/drain contact technologies need to be explored to reduce the R_{ext} and improve on-state variation.

Furthermore, we investigate the scaling metrics of InGaAs GAA MOSFETs with 6 nm T_{NW} and FGA. The T_{NW} scaling of an InGaAs GAA MOSFET theoretically has the same effect as the W_{NW} scaling in terms of the electrostatic control.[4] However, the scaling of T_{NW} can reduce the surface area that has underwent dry etching process during the nanowire formation, leading to the reduced surface roughness. Figure 5 shows SS and DIBL versus L_{ch} with $W_{NW} = 30\,nm$.

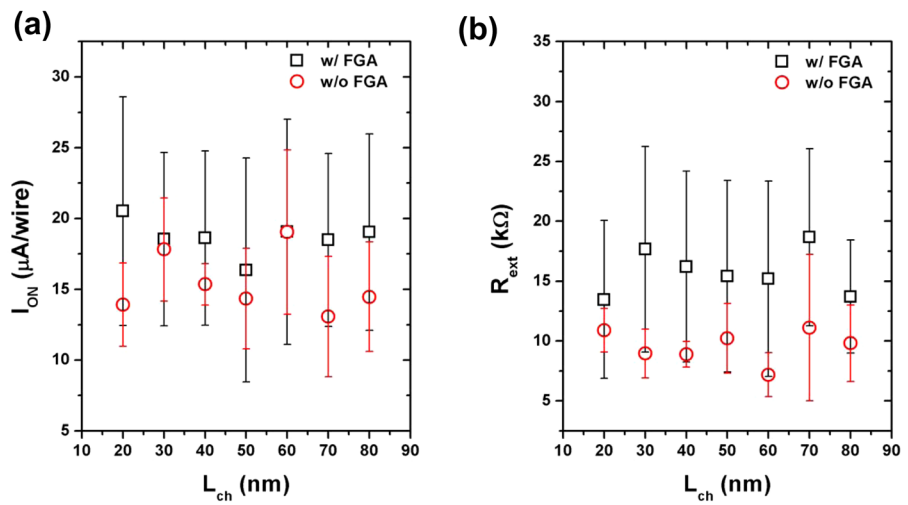

FIG. 4. (a) I_{on} and (b) R_{ext} versus L_{ch} in comparison between FGA devices and their control ones.

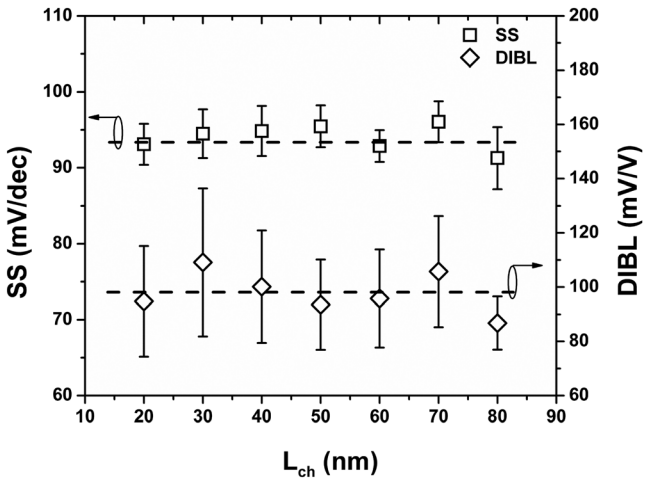

FIG. 5. SS and DIBL versus L_{ch} of FGA treated InGaAs GAA MOSFETs with $W_{NW} = 30$ nm and $T_{NW} = 6$ nm.

No evidence of L_{ch} dependence of SS and DIBL are observed in this work, as opposed to the InGaAs GAA MOSFETs with larger T_{NW}.[4] The results show that the InGaAs GAA MOSFETs with extremely thin T_{NW} offer better immunity to SCE and improved scalability which can be further improved by equivalent oxide thickness (EOT) scaling.[4,18,19]

In conclusion, InGaAs GAA MOSFETs with 6 nm T_{NW} have been fabricated. The effects of FGA on the performance of the devices are systematically studied. It is found that the 30 min 400 °C forming gas anneal results in an improved Al_2O_3/InGaAs interface and is also fully compatible with the $(NH_4)_2S$ passivation. A scaling metrics study of the InGaAs GAA MOSFETs has also been carried out. The extremely thin nanowire structure has been shown to improve SCE immunity, and it is very promising for future logic applications.

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