High performance atomic-layer-deposited $LaLuO_3$/Ge-on-insulator p-channel metal-oxide-semiconductor field-effect transistor with thermally grown GeO_2 as interfacial passivation layer

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Enhancement-mode p-channel metal-oxide-semiconductor field-effect transistor (MOSFET) on germanium-on-insulator substrate is fabricated with atomic-layer-deposited (ALD) $LaLuO_3$ as gate dielectric. Significant improvement in both on-state current and effective hole mobility has been observed for devices with thermal GeO_2 passivation. The negative threshold voltage (V_T) shift in devices with GeO_2 interfacial layer (IL) further demonstrates the effectiveness of surface passivation. Results from low temperature mobility characterization show that phonon scattering is the dominant scattering mechanism at a large inversion charge, indicating good interface quality. The combination of higher-*k* $LaLuO_3$ and ultrathin GeO_2 IL is a promising solution to the tradeoff between the aggressive equivalent oxide thickness scaling and good interface quality. © *2010 American Institute of Physics*. [doi:10.1063/1.3462303]

As device scaling of silicon complementary metal-oxide-semiconductor (MOS) is approaching its fundamental physical limits, innovative device structures such as Fin-field-effect transistors (FETs) and Gate-all-around FETs have been proposed and demonstrated for superior electrostatic control. An alternative approach to continue the trend of scaling is by implementing novel channel materials with superior transport properties. Extensive research has been done on using III–V compound semiconductors as n-channel and germanium as p-channel substrate, mainly due to their high electron and hole mobility, respectively. In both cases, one challenging task is the formation of high-quality gate stack with low interface trap density and low equivalent oxide thickness (EOT). Among all the Ge passivation techniques, thermally grown GeO_2 is the most natural choice that has been proven effective in passivating germanium surface.[1–5] However, the dielectric constant of GeO_2 is low (k=6), so it cannot be used as the gate dielectric for aggressively scaled devices. On the other hand, high-*k* dielectric (k>20) is favorable for aggressive EOT scaling. Ternary rare earth oxides such as $LaLuO_3$ have been considered as promising candidates for "higher-*k*" gate dielectric.[6] Recently, superior $LaLuO_3$/Ge MOS capacitance-voltage (CV) characteristics have been demonstrated with high pressure oxygen annealing.[7] However, in that work the GeO_2 interfacial layer is around 9 nm, which increases the total EOT significantly. For device applications, a much thinner GeO_2 layer is required for proper oxide thickness scaling.

In this letter, we systematically study the effect of a thin thermal GeO_2 passivation layer at $LaLuO_3$/Ge interface at the transistor level, using germanium-on-insulator (GeOI) formed by Smart Cut technology as the starting substrate. GeOI substrate is attractive because of its transport properties superior to silicon, low capacitance coupling, better electrostatic control and integration potential on Si-platform. Promising pMOSFET results have been reported on GeOI substrates obtained either by Ge condensation technique,[8] rapid melt growth method,[9] or Smart Cut technology.[10–12] Here we present well-behaved transistor performance with atomic-layer-deposited (ALD) $LaLuO_3$ as gate dielectric. The effectiveness of thin thermal GeO_2 as a passivation layer is demonstrated from both transistor I-V characteristics and the measured effective hole mobility. The high interface quality is further verified by temperature dependent mobility characterization down to 10 K, which shows the dominant phonon scattering mechanism.

MOSFET fabrication starts with a 100 mm GeOI wafer from Soitec. The germanium layer is about 100 nm thick, with (100) orientation and an n-type Sb doping lower than 4×10^{15} cm^{-3}. The Ge film is produced by layer transfer from bulk Ge, and it is separated from the Si substrate by 400 nm SiO_2 layer. The Si handle wafer has a p-type doping with a resistivity around 14 to 22 Ω cm. From the substrate parameters, the maximum depletion width is calculated to be around 350 nm. Since the maximum depletion width is much larger than the Ge film thickness, the fabricated devices operate in a fully depleted GeOI regime.

The GeOI wafer was first treated with cyclic 2% hydrofluoric (HF) acid and de-ionized water rinse to remove any native oxide present. The rinse was stopped at HF to maintain a hydrophobic surface. Then the wafer was transferred to an oxidation furnace immediately. About 1.5 nm of GeO_2 was thermally grown at 450 °C in dry oxygen ambient. Control samples without thermal oxidation were also prepared. Then 5 nm $LaLuO_3$ was grown at 350 °C in a horizontal gas flow ALD chamber, with $La(amd)_3$ and $Lu(amd)_3$ as precursors. The procedure is one monolayer of La_2O_3 deposition followed by one monolayer of Lu_2O_3 deposition and then repeats alternatively. Therefore the final ratio of

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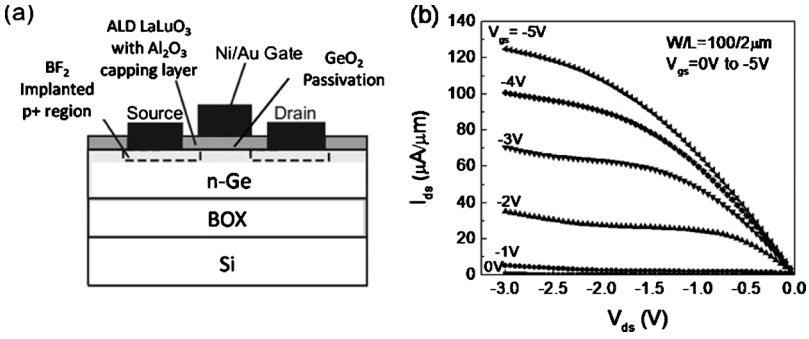

FIG. 1. (a) Cross section schematic view of ALD $LaLuO_3$/GeOI PMOSFET with GeO_2 passivation layer. (b) Output characteristics of a typical channel length $L_{ch}=2$ μm device with gate voltage V_{gs} from 0 to −5 V.

La_2O_3:Lu_2O_3 is 1:1. Since $LaLuO_3$ is water soluble, a 5 nm Al_2O_3 capping layer was deposited in an ASM F-120 ALD reactor at a substrate temperature of 300 °C to protect the gate stack throughout the fabrication process. Note that devices without Al_2O_3 capping layer suffer from severe gate leakage, suggesting that the gate oxide is being damaged during fabrication. Thus the results presented in this Letter are all from devices with the protection layer. After gate stack formation, a p-type dopant BF_2 was implanted at 10 keV with a dose of 1×10^{15} cm^{-2}. The dopant activation was carried out in a N_2 furnace at 450 °C for 30 min. Contact windows were opened by BCl_3 dry etching to protect the gate stack from water exposure. After a short 10% HCl dip, metal contacts consisting of 10 nm Ti and 70 nm Al were electron beam evaporated, followed by contact annealing at 440 °C in N_2. Finally, 30 nm Ni and 80 nm Au was deposited as a gate metal.

Figure 1(a) shows the schematic cross section of the device structure of an ALD $LaLuO_3$/GeOI MOSFET with thermal GeO_2 passivation and an Al_2O_3 protection layer. The fabricated MOSFETs have a gate width of 100 μm and nominal channel length ranging from 2 to 40 μm. The contact resistance and sheet resistance of the p-implanted region is determined to be 0.87 Ω mm and 260.4 Ω/sq, respectively, both using transfer length method. The dielectric constant of the ALD $LaLuO_3$ is determined to be 24 from previous MOS capacitor measurements. Since GeO_2 has a dielectric constant of about 6, the total EOT is estimated to be around 1.14 nm for 5 nm $LaLuO_3$ and 1.5 nm GeO_2, not counting the capping layer. Further reduction in GeO_2, $LaLuO_3$, and, in particular, Al_2O_3 capping layer is needed to achieve 1 nm EOT for ultimately scaled devices. Figure 1(b) shows the output characteristics of a typical 2 μm device with gate voltage ranging from 0 to −5 V. The maximum drain current reaches 125 $\mu A/\mu m$ at a drain bias of −3 V and the transistor is pinched off at zero gate bias. Transfer characteristics show an on-off current ratio of 2300 at $V_{ds}=-2$ V, mainly limited by reverse biased drain junction leakage current. The threshold voltage (V_T) of devices with GeO_2 passivation is found to be around −0.53 V determined by linear extrapolation method at a low drain bias. However, devices with direct $LaLuO_3$ deposition at the same gate length show a threshold voltage of around −0.03 V. This means that there is a ~0.5 V positive V_T shift for devices without GeO_2 passivation. Positive V_T shift is an indirect evidence that the samples without GeO_2 passivation have a significantly higher interface trap density.[13] The charge neutrality level (CNL) in Ge lies close to the valence band. The unpassivated n-type surface gives a larger negative interface trap density from acceptor traps, which tend to facilitate inversion. As a result, the measured threshold voltage for unpassivated surface is shifted to positive gate voltage. Furthermore, the current-voltage characteristics as shown in Fig. 2 give a direct proof of the effect of GeO_2 passivation. After normalizing the EOT and subtracting the threshold voltage, devices with thermal GeO_2 interfacial layer show a 33% increase in drive current. The transconductance is also improved after GeO_2 passivation.

To further investigate the transport properties and the scattering mechanism, low temperature mobility measurements are performed in a Janis cryogenic system with temperature varying from 300 K down to 10 K. Figure 3(a) shows the low temperature transfer characteristics for a 40 μm device at a drain bias of −50 mV. The off-currents are found to be very low for temperatures below 150 K. This indicates that the leakage source at room temperature is mainly from source and drain junctions. In addition, both on-current and maximum transconductance increase as temperature decreases. This shows that phonon scattering dominates and that the interface is of reasonably good quality. Split CV measurements are also carried out at the same time. By integrating the C_{gc}-V_g curve, the inversion charge density is obtained. With the drain conductance calculated from the above I-V measurement, the effective hole mobility as a function of inversion charge density at various temperatures are plotted in Fig. 3(b). The mobility for devices without GeO_2 passivation is also plotted for comparison. First of all, the thermal GeO_2 interfacial layer clearly provides a factor of 1.5 improvement of the effective hole mobility. This is a direct evidence that GeO_2 passivation is beneficial to $LaLuO_3$/Ge interface. Second, as temperature decreases, devices with GeO_2 show improvement from a room tempera-

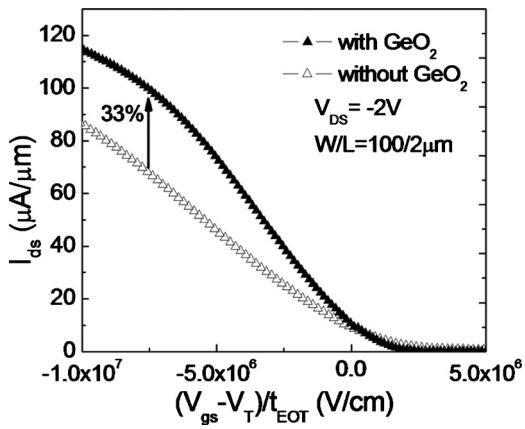

FIG. 2. Comparison of normalized drain current (I_{ds}) at $V_{ds}=-2$ V for devices with or without thin GeO_2 interfacial layer.

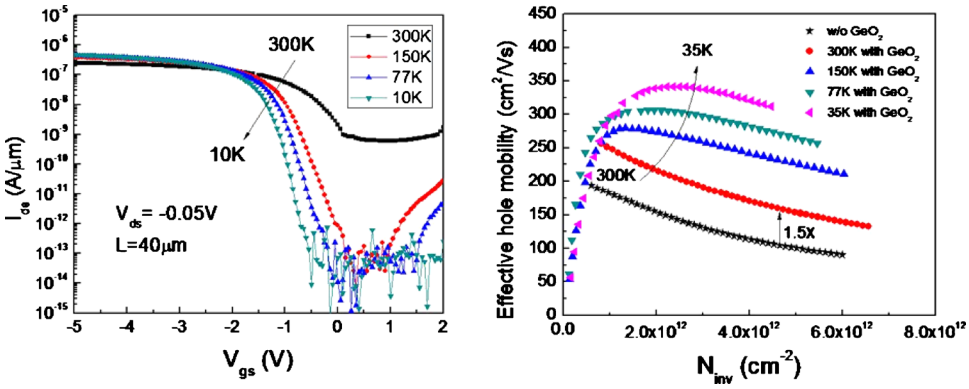

FIG. 3. (Color online) (a) Temperature dependent transfer characteristics for a 40 μm gate length $LaLuO_3$/GeOI PMOSFET when drain voltage (V_{ds}) is biased at −50 mV. (b) Effective mobility (μ_{eff}) vs inversion charge density (N_{inv}) for devices with and without GeO_2 interfacial layer.

ture mobility of 260 cm^2/V s and reach a maximum mobility of about 350 cm^2/V s at 35 K. This suggests again that electron-phonon scattering is the dominant mechanism at large vertical fields instead of Coulomb or surface roughness scattering at the interface.

In conclusion, high performance ALD $LaLuO_3$ GeOI pMOSFETs have been demonstrated with thermal GeO_2 passivation. A maximum drain current of 125 $\mu A/\mu m$ for a 2 μm device and a maximum effective hole mobility of 260 cm^2/V s at room temperature are obtained. The effect of GeO_2 passivation on $LaLuO_3$/Ge interface has been confirmed with the increase in on-current and transconductance, positive threshold voltage shift, and 50% improvement in effective hole mobility. This shows that ALD $LaLuO_3$ with ultrathin GeO_2 passivation layer is a promising gate stack for future Ge pMOSFETs.

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[1]A. Delabie, F. Bellenger, M. Houssa, T. Conard, S. V. Elshocht, M. Caymax, M. Heyns, and M. Meuris, Appl. Phys. Lett. **91**, 082904 (2007).
[2]H. Matsubara, T. Sasada, M. Takenaka, and S. Takagi, Appl. Phys. Lett. **93**, 032104 (2008).
[3]Y. Nakakita, R. Nakane, T. Sasada, H. Matsubara, M. Takenaka, and S. Takagi, Tech. Dig. - Int. Electron Devices Meet. **2008**, 877.
[4]R. Xie, T. H. Phung, W. He, Z. Sun, M. Yu, Z. Cheng, and C. Zhu, Tech. Dig. - Int. Electron Devices Meet. **2008**, 393.
[5]H.-Y. Yu, M. Ishibashi, J.-H. Park, M. Kobayashi, and K. C. Saraswat, IEEE Electron Device Lett. **30**, 675 (2009).
[6]J. M. J. Lopes, M. Roeckerath, T. Heeg, E. Rije, J. Schubert, S. Mantl, V. V. Afanas'ev, S. Shamuilia, A. Stesmans, Y. Jia, and D. G. Schlom, Appl. Phys. Lett. **89**, 222902 (2006).
[7]T. Tabata, C. H. Lee, K. Kita and A. Toriumi, ECS Trans. **16**(5), 479 (2008).
[8]T. Irisawa, T. Numata, T. Tezuka, K. Usuda, N. Hirashita, N. Sugiyama, E. Toyoda, and S.-I. Takagi, IEEE Trans. Electron Devices **53**, 2809 (2006).
[9]J. Feng, G. Thareja, M. Kobayashi, S. Chen, A. Poon, Y. Bai, P. B. Griffin, S. S. Wong, Y. Nishi, and J. D. Plummer, IEEE Electron Device Lett. **29**, 805 (2008).
[10]C. Le Royer, L. Clavelier, C. Tabone, K. Romanjek, C. Deguet, L. Sanchez, J.-M. Hartmann, M.-C. Roure, H. Grampeix, S. Soliveres, G. L. Carval, R. Truche, A. Pouydebasque, M. Vinet, and S. Deleonibus, Solid-State Electron. **52**, 1285 (2008).
[11]K. Romanjek, E. Augendre, W. Van Den Daele, B. Grandchamp, L. Sanchez, C. Le Royer, J.-M. Hartmann, B. Ghyselen, E. Guiot, K. Bourdelle, S. Cristoloveanu, F. Boulanger, and L. Clavelier, Microelectron. Eng. **86**, 1585 (2009).
[12]K. Romanjek, L. Hutin, C. Le Royer, A. Pouydebasque, M.-A. Jaud, C. Tabone, E. Augendre, L. Sanchez, J.-M. Hartmann, H. Grampeix, V. Mazzocchi, S. Soliveres, R. Truche, L. Clavelier, P. Scheiblin, X. Garros, G. Reimbold, M. Vinet, F. Boulanger, and S. Deleonibus, Solid-State Electron. **53**, 723 (2009).
[13]P. Tsipas and A. Dimoulas, Appl. Phys. Lett. **94**, 012114 (2009).