Inversion-mode GaAs wave-shaped field-effect transistor on GaAs (100) substrate

Jingyun Zhang, Xiabing Lou, Mengwei Si, Heng Wu, Jiayi Shao, Michael J. Manfra, Roy G. Gordon, and Peide D. Ye

Articles you may be interested in

Effects of gate-last and gate-first process on deep submicron inversion-mode InGaAs n-channel metal-oxide-semiconductor field effect transistors
J. Appl. Phys. **109**, 053709 (2011); 10.1063/1.3553440

Low damage fully self-aligned replacement gate process for fabricating deep sub-100 nm gate length GaAs metal-oxide-semiconductor field-effect transistors
J. Vac. Sci. Technol. B **28**, C6L1 (2010); 10.1116/1.3501355

Self-aligned inversion-type enhancement-mode GaAs metal-oxide-semiconductor field-effect transistor with Al 2 O 3 gate dielectric
Appl. Phys. Lett. **92**, 203505 (2008); 10.1063/1.2931708

Fabrication of gate stack with high gate work function for implantless enhancement-mode GaAs n -channel metal-oxide-semiconductor field effect transistor applications
Appl. Phys. Lett. **92**, 123513 (2008); 10.1063/1.2905259

Correlation of surface chemistry of GaAs substrates with growth mode and stacking fault density in ZnSe epilayers
J. Vac. Sci. Technol. A **20**, 1948 (2002); 10.1116/1.1513645

Inversion-mode GaAs wave-shaped field-effect transistor on GaAs (100) substrate

Jingyun Zhang,[1] Xiabing Lou,[2] Mengwei Si,[1] Heng Wu,[1] Jiayi Shao,[3] Michael J. Manfra,[1,3,4] Roy G. Gordon,[2] and Peide D. Ye[1,a)]

[1]School of Electrical and Computer Engineering and Birck Nanotechnology Center, Purdue University, West Lafayette, Indiana 47907, USA
[2]Department of Chemistry and Chemical Biology, Harvard University, Cambridge, Massachusetts 02138, USA
[3]Department of Physics, Purdue University, West Lafayette, Indiana 47907, USA
[4]School of Materials Engineering, Purdue University, West Lafayette, Indiana 47907, USA

Inversion-mode GaAs wave-shaped metal-oxide-semiconductor field-effect transistors (WaveFETs) are demonstrated using atomic-layer epitaxy of La_2O_3 as gate dielectric on (111)A nano-facets formed on a GaAs (100) substrate. The wave-shaped nano-facets, which are desirable for the device on-state and off-state performance, are realized by lithographic patterning and anisotropic wet etching with optimized geometry. A well-behaved $1\,\mu m$ gate length GaAs WaveFET shows a maximum drain current of $64\,mA/mm$, a subthreshold swing of $135\,mV/dec$, and an I_{ON}/I_{OFF} ratio of greater than 10^7. © 2015 AIP Publishing LLC. [http://dx.doi.org/10.1063/1.4913431]

GaAs has been considered to replace Si in logic applications for decades due to its high electron mobility.[1] To achieve high on-current surface-channel inversion-mode n-channel metal-oxide-semiconductor field-effect transistors (MOSFETs) on GaAs (100) substrate is a long-time challenge. The main obstacle is the lack of high-quality, thermodynamically stable dielectric on GaAs that can match the device criteria as SiO_2 on Si such as a mid-gap interface trap density (D_{it}) around $10^{10}\,cm^{-2}\,eV^{-1}$. During the past decades, tremendous efforts have been made to improve the oxide/GaAs interface with most of focus on different types of oxides and formation methods.[2–10] Recent work finds that the oxide/GaAs interface quality is strongly dependent on semiconductor surface orientations. GaAs MOSFETs fabricated on (111)A surface exhibit much higher on-state current (I_{ON}) than other surface-orientations such as (100) and (111)B even with the same atomic-layer-deposited (ALD) oxide.[11] More interestingly, much larger I_{ON} can be achieved on GaAs (111)A substrate with single crystalline La-based oxide dielectrics by atomic-layer-epitaxy (ALE).[12] Mid-gap D_{it} or Fermi-level-pinning problem is significantly reduced with epitaxial La_2O_3 on GaAs (111)A surface,[13,14] because the number of dangling bonds are dramatically reduced due to the nature of epitaxial oxide/semiconductor interface. However, GaAs (111)A substrate is technologically less important than the widely available GaAs (100) substrate, in particular, for the development of a manufacturable device technology.

In this letter, we demonstrate GaAs wave-shaped MOSFETs (WaveFETs) on a GaAs (100) substrate by nano-engineering to form ALE La_2O_3 on (111)A nano-facets. GaAs (111)A surface is achieved on a GaAs (100) substrate by the development of a well-controlled anisotropic wet etching process. GaAs MOSFETs are formed on wave-shaped (111)A surface channels with epitaxial La_2O_3 as

dielectric. But, all devices are fabricated on GaAs (100) substrates. These devices have on-state current (I_{ON}) of $64\,mA/mm$ and transconductance (g_m) of 32 mS/mm with sub-threshold swing (SS) around $135\,mV/dec$. This work opens a route to realize high-performance GaAs MOSFETs on (100) substrates potentially. The process development and deep understanding of surface chemistry on these nano-facets could also be very important for the emerging 3D III–V devices.[15–23]

Figures 1(a) and 1(b) show the schematic view and cross-sectional view of a GaAs WaveFET in this work fabricated on a semi-insulating GaAs (100) substrate with an ALE high-k dielectric. The detailed process flow is described following. An HF and H_2O_2 based anisotropic wet etching process[24] was applied to form the wave structure with Ti/Au as hard mask illustrated in Figure 2. MOSFET fabrication starts with 2-in. semi-insulating GaAs (100) substrates. As-received wafers were first degreased at room temperature by acetone for 10 min, methanol for 5 min, and isopropanol
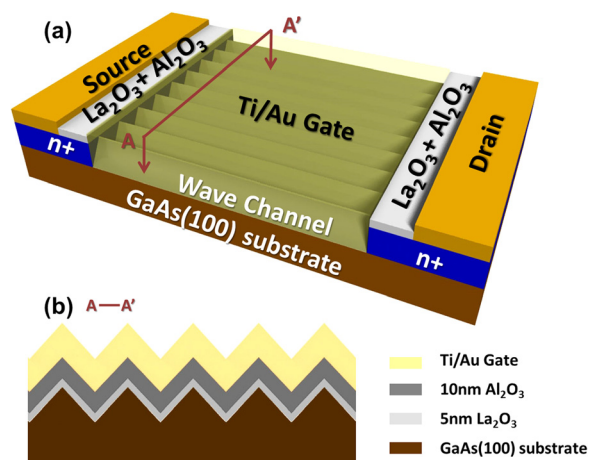

FIG. 1. (a) Schematic and (b) Cross-sectional view of an inversion-mode GaAs (100) WaveFET with ALE La_2O_3.

a)Author to whom correspondence should be addressed. Electronic mail: yep@purdue.edu
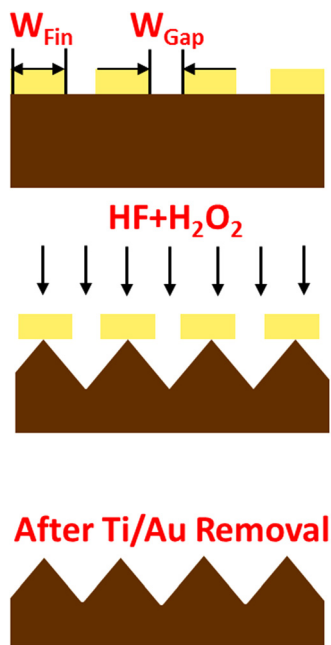
FIG. 2. Illustration of wave channel formation by anisotropic wet etching. GaAs (111)A surface on these nano-facets is achieved by anisotropic wet etching of GaAs using HF solution.

for 5 min, respectively. The wave patterns were defined by electron beam lithography and Ti/Au (2 nm/10 nm) were deposited by electron beam evaporation. After lift-off process, periodically patterned Ti/Au strip hard masks were formed as illustrated in Figure 2. Then, the wafers were dipped into HF (49%): H_2O_2 (30%) (10:129) based solution to form the wave-shaped channels for 3 s. The wet etching time depends on the design of the fin-width (W_{Fin}) and the gap-width (W_{Gap}) as depicted in Figure 2. W_{Fin}, W_{Gap}, and etching time were optimized to achieve the maximum effective length width. The (111)A surface was obtained due to the anisotropic property of the wet etching process.[25] The realization of (111)A other than (111)B is further confirmed by the electrical properties of the fabricated devices since the Fermi level on (111)B is expected to be pinned.[11] After removal of Ti/Au hard mask by KI solution, the wafers were dipped into buffered oxide etch (BOE) for 30 s and then soaked in 10% $(NH_4)_2S$ for 15 min for surface passivation. After deionized water rinse, the wafers were quickly transferred into ALD deposition chamber. 5 nm epitaxial La_2O_3 and 10 nm amorphous Al_2O_3 were then deposited by ALE/ALD. GaAs WaveFETs with 8 nm amorphous Al_2O_3 only as gate dielectric were also fabricated as the control sample. The epitaxial La_2O_3 thin films employed here were deposited from the precursors lanthanum tris(N,N′-diisopropylformamidinate) and H_2O at 385 °C, while the amorphous Al_2O_3 oxide capping layer was deposited with precursors of trimethylalumnum (TMA) and H_2O at 300 °C. The precursor and pulse time was all 1 s. The purpose of Al_2O_3 capping layer is to prevent the reaction between La_2O_3 and moisture in air and water during the process. Source and drain (S/D) regions were formed by a two-step Si implantation with dose of 1×10^{14} cm^{-2} at 30 keV and 1×10^{14} cm^{-2} at 80 keV, followed by an 850 °C rapid thermal annealing (RTA) in N_2 for 15 s. S/D ohmic contact area was first defined by

electron-beam lithography, and then BCl_3/Ar inductively coupled plasma (ICP) dry etching was applied to remove the Al_2O_3 and HCl wet etching was applied to remove the La_2O_3 above metal contact area. Au/Ge/Au/Ni/Au (5 nm/12.5 nm/15 nm/9 nm/50 nm) contact was then formed followed by a 420 °C RTA in N_2 for 15 s. Then, Ti/Au (30 nm/60 nm) were deposited as gate electrodes and test pads. All patterns were defined by a Vistec VB-6 UHR electron beam lithography system. The fabricated devices have gate lengths (L_g) of 1 μm, 2 μm, and 4 μm.

The illustration of anisotropic wet etch process (HF and H_2O_2) is shown in Fig. 3. In this process, the wave patterned direction is critical. The wave structure has to be patterned along $(01\bar{1})$ other than (011) as shown in Figure 3(a). The effect of wave pattern direction is shown by cross-sectional scanning electron microscopy (SEM) pictures in Figures 3(b) and 3(c). Hard mask strips were patterned along $(01\bar{1})$ in Figure 3(b) and along (011) in Figure 3(c). Clear (111) surface is shown in Figure 3(b), but irregular structures are formed if hard mask strips were patterned along (011). Meanwhile, optimized W_{Fin} and W_{Gap} are also important to form compact wave structure with sharp corners, so that the maximum channel width with (111)A surface can be realized within the fixed channel pitch from the top. Figure 4(a) shows the transmission electron microscopy (TEM) picture of the cross section of the wave channel. A high-resolution TEM image of the epitaxial interface, taken from a sample with 5 nm La_2O_3/10 nm Al_2O_3 as gate dielectric, is also shown in Figure 4(b). The lattice mismatch of La_2O_3 on GaAs (111)A is ∼0.04%. It is evident from TEM image that a flat and sharp interface is formed even on fabricated (111)A nano-facet. It has been proved by C-V measurement that the epitaxial La_2O_3/GaAs (111)A interface exhibits D_{it} on the order of 10^{11} cm^{-2}eV^{-1}, which is far below the D_{it} level of traditional amorphous oxide on GaAs (111)A surface.[12,13] Figure 4(c) depicts the top view SEM image of one finished GaAs WaveFET with a gate length of 2 μm.

Well-behaved output, transfer, and trans-conductance characteristics of a 1 μm-gate-length inversion-mode GaAs WaveFET are plotted in Figure 5, showing a maximum drain current ($I_{D,max}$) of 64 mA/mm at a gate bias (V_{GS}) of 4 V and a drain bias (V_{DS}) of 2 V, a maximum g_m of 32 mS/mm at $V_{DS} = 2$ V, and threshold voltage (V_T) of 1.32 V. SS of
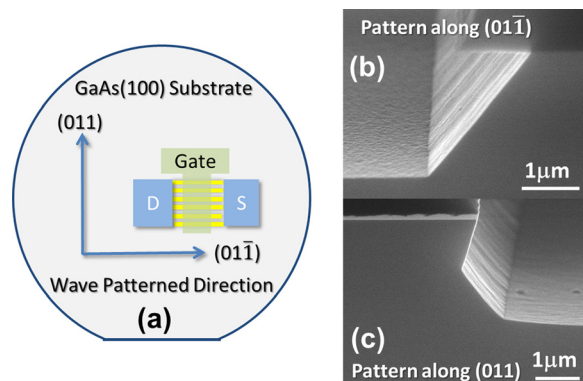

FIG. 3. (a) Schematic diagram of wave patterned orientation. (b) and (c) Cross-sectional SEM images of wave structures patterning along $(01\bar{1})$ and (011) orientations.
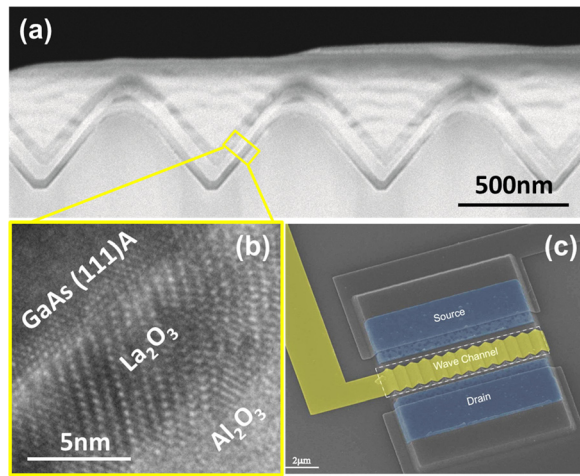
FIG. 4. (a) Cross-sectional STEM image of GaAs WaveFET structure covered with La_2O_3 and Al_2O_3. (b) HRTEM image of La_2O_3/GaAs interface. Epitaxial La_2O_3 forms a flat and sharp interface on wave surface. (c) SEM image of a GaAs (100) WaveFET device top view with $L_g = 2\ \mu m$. Parallel wave structures are clearly shown as device channel.

$\sim 135\ mV/dec$ is obtained with an equivalent oxide thickness (EOT) of $\sim 6\ nm$, indicating a mid-gap interface trap density of $4.5 \times 10^{12}\ cm^{-2}\,eV^{-1}$, which is simply estimated from equation $SS \sim 60 \times (1 + qD_{it}/C_{ox})$ mV/dec. SS could be further improved by optimizing fabrication process and reducing EOT. It will also improve the extrinsic drain current and trans-conductance by reducing the EOT of the dielectric and improving interface quality. Devices with different gate length L_g (1, 2 and $4\ \mu m$) show similar SS and V_T (not

shown), indicating that these devices are weakly affected by short channel effects. It is also expected that these GaAs devices with a large bandgap and 3D wave structures must have better immunity to short channel effects. The GaAs WaveFET with epitaxial La_2O_3 demonstrated here has $I_{D,max}$ about $1000 \times$ larger than that of the reference GaAs sample with amorphous Al_2O_3 dielectric (not shown) and about $10\,000 \times$ larger than that of GaAs planar MOSFET on GaAs (100) substrate with amorphous Al_2O_3.[11] GaAs planar MOSFETs on GaAs (100) substrate with La_2O_3 as gate dielectric were also fabricated. Without the special surface orientation to form (111) hexagonal template, poor quality La_2O_3 dielectric was formed on GaAs (100) surface showing a weak gate modulation and minuscule $I_{D,max}$. Figure 5(d) summarizes the effective gate length L_{eff} and the series resistance (R_{SD}) extracted by plotting R_{tot} versus L_g, where R_{tot} represents the total channel resistance measured from devices with various gate lengths under $V_{GS}-V_T$ from 1 to 2.5 V. R_{SD} is determined to be $1.62\ \Omega\cdot mm$, which is reasonable for implanted S/D on GaAs and can be further reduced by optimizing the processes of ion implantation and activation during S/D contact fabrication. Contact resistance (R_C) of $0.27\ \Omega\cdot mm$ is extracted from transmission line method. Two third of R_{SD} is from the access resistance between Ohmic contacts to the channel underneath the gate. ΔL, defined as the difference between the mask gate length L_g and L_{eff}, is estimated to be $\sim 0.36\ \mu m$, due to the lateral dopant diffusion caused by high-temperature activation and/or the lithographic misalignment.

In conclusion, by realizing (111)A nano-facets on (100) surface by anisotropic wet etching and a high-quality epitaxial La_2O_3/GaAs (111)A interface by ALE, we demonstrate inversion-mode GaAs WaveFETs on GaAs (100) substrates with much larger drain currents than those formed on planar GaAs (100) surface using the same dielectric process. The work opens up a way to improve the III–V device performance by nano-engineering semiconductor 3D structures and interfaces with high-k dielectric.
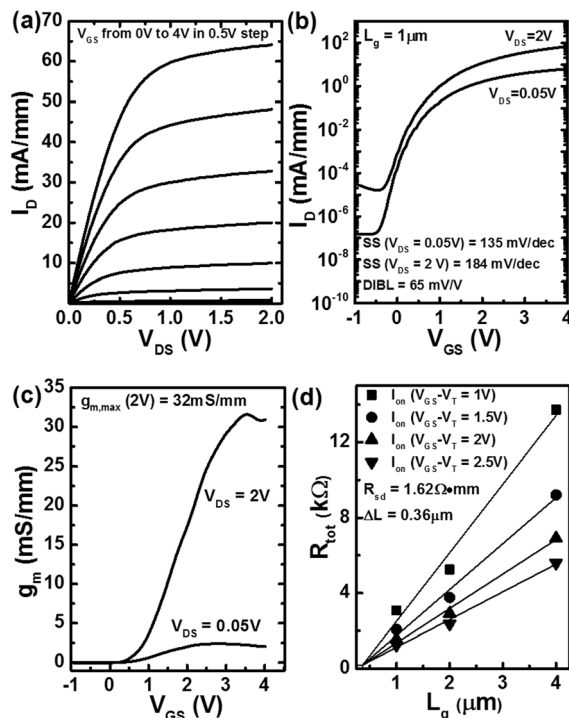
FIG. 5. (a) Output and (b) transfer (c) g_m characteristics of a GaAs WaveFET with $L_g = 1\ \mu m$. The device shows maximum drain current of 64 mA/mm, a subthreshold swing of 135 mV/dec, a peak trans-conductance of 32 mS/mm, and an I_{ON}/I_{OFF} greater than 10^7. (d) Measured total resistance versus different mask gate lengths as a function of gate bias. R_{SD} of $1.62\ \Omega\cdot mm$ and ΔL of $\sim 0.36\ \mu m$ are determined from the fitting lines.

[1]H. Becke, R. Hall, and J. White, Solid-State Electron. **8**(10), 813 (1965).
[2]M. Hong, J. Kwo, A. R. Kortan, J. P. Mannaerts, and A. M. Sergent, Science **283**(5409), 1897 (1999).
[3]M. Passlack, M. Hong, J. P. Mannaerts, J. R. Kwo, and L. W. Tu, Appl. Phys. Lett. **68**, 3605 (1996).
[4]P. D. Ye, G. D. Wilk, J. Kwo, B. Yang, H.-J. L. Gossmann, M. Frei, S. N. G. Chu, J. P. Mannaerts, M. Sergent, and M. Hong, IEEE Electron Devices Lett. **24**, 209 (2003).
[5]S. J. Koester, E. W. Kiewra, Y. Sun, D. A. Neumayer, J. A. Ott, M. Copel, D. K. Sadana, D. J. Webb, J. Fompeyrine, and J. P. Locquet, Appl. Phys. Lett. **89**, 042104 (2006).
[6]D. Shahrjerdi, M. M. Oye, A. L. Holmes, Jr., and S. K. Banerjee, Appl. Phys. Lett. **89**, 043501 (2006).

[7] I. Ok, H. Kim, M. Zhang, T. Lee, F. Zhu, L. Yu, S. Koveshnikov, W. Tsai, V. Tokranov, and M. Yakimov, IEEE Int. Electron Devices Meet. **2006**, 829.

[8] C. H.-C. Chin, M. Zhu, Z.-C. Lee, X. Liu, K.-M. Tan, H. K. Lee, L. Shi, L.-J. Tang, C.-H. Tung, and G.-Q. Lo, IEEE Int. Electron Devices Meet. **2008**, 553.

[9] R. J. W. Hill, D. A. J. Moran, X. Li, H. P. Zhou, D. Macintyre, S. Thoms, A. Asenov, P. Zurcher, K. Rajagopalan, and J. Abrokwah, IEEE Electron Devices Lett. **28**, 1080 (2007).

[10] Y. C. Chang, W. H. Chang, C. Merckling, J. Kwo, and M. Hong, Appl. Phys. Lett. **102**, 093506 (2013).

[11] M. Xu, K. Xu, R. Contreras, M. Milojevic, T. Shen, O. Koybasi, Y. Q. Wu, R. M. Wallace, and P. D. Ye, IEEE Int. Electron Devices Meet. **2009**, 865.

[12] X. W. Wang, L. Dong, J. Y. Zhang, Y. Q. Liu, P. D. Ye, and R. G. Gordon, Nano Lett. **13**(2), 594 (2013).

[13] L. Dong, X. W. Wang, J. Y. Zhang, X. F. Li, R. G. Gordon, and P. D. Ye, IEEE Electron Devices Lett. **34**, 487 (2013).

[14] L. Dong, X. W. Wang, J. Y. Zhang, X. F. Li, X. B. Lou, N. Conrad, H. Wu, R. G. Gordon, and P. D. Ye, Symp. VLSI Technol. Circuits **2014**, 50.

[15] Y. Q. Wu, R. S. Wang, T. Shen, J. J. Gu, and P. D. Ye, IEEE Int. Electron Devices Meet. **2009**, 331.

[16] M. Radosavljevic, G. Dewey, J. M. Fastenau, J. Kavalieros, R. Kotlyar, B. Chu-Kung, W. K. Liu, D. Lubyshev, M. Metz, K. Millard, N. Mukherjee, L. Pan, R. Pillarisetty, W. Rachmady, U. Shah, and R. Chau, IEEE Int. Electron Devices Meet. **2010**, 126.

[17] F. Xue, A. Jiang, Y.-T. Chen, Y. Wang, F. Zhou, Y.-F. Chang, and J. Lee, IEEE Int. Electron Devices Meet. **2012**, 632.

[18] M. Radosavljevic, G. Dewey, D. Basu, J. Boardman, B. Chu-Kung, J. M. Fastenau, S. Kabehie, J. Kavalieros, V. Le, W. K. Liu, D. Lubyshev, M. Metz, K. Millard, N. Mukherjee, L. Pan, R. Pillarisetty, W. Rachmady, U. Shah, H. W. Then, and R. Chau, IEEE Int. Electron Devices Meet. **2011**, 765.

[19] J. J. Gu, X. W. Wang, J. Shao, A. T. Neal, M. J. Manfra, R. G. Gordon, and P. D. Ye, IEEE Int. Electron Devices Meet. **2012**, 633.

[20] A. V. Thathachary, N. Agrawal, L. Liu, and S. Datta, Nano Lett. **14**, 626 (2014).

[21] N. Waldron, C. Merckling, L. Teugels, P. Ong, S. A. U. Ibrahim, F. Sebaai, A. Pourghaderi, K. Barla, N. Collaert, and A. V. Y. Thean, IEEE Electron Devices Lett. **35**, 1097 (2014).

[22] C. Zota, L. Wernersson, and E. Lind, IEEE Electron Devices Lett. **35**, 342 (2014).

[23] T. W. Kim, D. H. Kim, D. H. Koh, H. M. Kwon, R. H. Baek, D. Veksler, C. Huffman, K. Matthews, S. Oktyabrsky, A. Greene, Y. Ohsawa, A. Ko, H. Nakajima, M. Takahashi, T. Nishizuka, H. Ohtake, S. K. Banerjee1, S. H. Shin, D. H. Ko, C. Kang, D. Gilmer, R. J. W. Hill, W. Maszara, C. Hobbs, and P. D. Kirsch, IEEE Int. Electron Devices Meet. **2013**, 427.

[24] W. T. Tsang and A. Y. Cho, Appl. Phys. Lett. **30**, 293 (1977).

[25] W. T. Tsang and S. Wang, Appl. Phys. Lett. **28**, 44 (1976).