GaAs metal–oxide–semiconductor field-effect transistor with nanometer-thin dielectric grown by atomic layer deposition

P. D. Ye,[a] G. D. Wilk, B. Yang, J. Kwo, S. N. G. Chu, S. Nakahara, H.-J. L. Gossmann, J. P. Mannaerts, M. Hong, K. K. Ng, and J. Bude
Agere Systems, 600 Mountain Avenue, Murray Hill, New Jersey 07974

(Received 27 January 2003; accepted 7 May 2003)

A GaAs metal–oxide–semiconductor field-effect transistor (MOSFET) with thin Al_2O_3 gate dielectric in nanometer (nm) range grown by atomic layer deposition is demonstrated. The nm-thin oxide layer with significant gate leakage current suppression is one of the key factors in downsizing field-effect transistors. A 1 μm gate-length depletion-mode *n*-channel GaAs MOSFET with an Al_2O_3 gate oxide thickness of 8 nm, an equivalent SiO_2 thickness of ~3 nm, shows a broad maximum transconductance of 120 mS/mm and a drain current of more than 400 mA/mm. The device shows a good linearity, low gate leakage current, and negligible hysteresis in drain current in a wide range of bias voltage. © *2003 American Institute of Physics.* [DOI: 10.1063/1.1590743]

GaAs metal–oxide–semiconductor field-effect transistor (MOSFET) has attracted great interest for decades.[1–13] GaAs-based devices potentially have great advantages over Si-based devices for high-speed and high-power applications, in part from an electron mobility in GaAs that is ~5× greater than that in Si, the availability of semi-insulating GaAs substrates, and higher breakdown field. Currently, the metal–semiconductor field-effect transistor (MESFET) is the dominant GaAs device for high-speed and microwave circuits. MESFETs feature gates formed by metal–semiconductor (Schottky-barrier) junctions, while MOSFETs have oxide layers (higher barrier) between metals and semiconductors. Compared to GaAs MESFETs, GaAs MOSFETs feature a larger maximum drain current, much lower gate leakage current, a better noise margin, and much greater flexibility in digital integrated circuit design. The main obstacle to GaAs-based MOSFET devices is the lack of high-quality, thermodynamically stable insulators on GaAs that can match the device criteria as SiO_2 on Si. After a decade of efforts, much progress has been made recently to form a high-quality oxide on III–V semiconductor, e.g., molecular beam epitaxy (MBE) grown $Ga_2O_3(Gd_2O_3)$ dielectric films on GaAs surface[14–19] and atomic layer deposition (ALD) grown Al_2O_3 on III–V semiconductors.[20]

To achieve higher transconductance as well as to downsize the device for higher integrated density, the reduction of the gate oxide thickness is critical. A gate material with a much wider band gap providing a higher potential barrier with GaAs is able to significantly reduce the gate leakage current for the same layer thickness of other materials. Al_2O_3 is a highly desirable gate dielectric with a high band gap of ~9 eV, which is much higher than other feasible gate oxide, e.g., Ga_2O_3 with a band gap of ~2.45 eV. As a popular high-*k* gate oxide, Al_2O_3 has the dielectric constant as high as 8.6–10, compared to 3.9 for SiO_2. In this letter, we report a MOSFET on a III–V substrate with a nanometer thin Al_2O_3 gate dielectric deposited by ALD. The deposited oxide layer is as thin as 8 nm, which is equivalent to the thickness of 3.1 nm for SiO_2. Al_2O_3 is a highly desirable gate dielectric not only because it has high band gap, but also it has a high breakdown field (5–10 MV/cm), high thermal stability, and remains amorphous under typical processing conditions. ALD itself is an *ex situ*, robust manufacturing process which is already commonly used for high-*k* gate dielectrics in Si complementary MOS (CMOS) technology.[21] It does not require ultrahigh-vacuum conditions for wafer transfer between semiconductor epilayer growth and oxide layer deposition, and may soon find wide applications in microelectronics manufacturing.

Figure 1(a) shows the device structure of the fabricated depletion-mode *n*-channel Al_2O_3/GaAs MOSFET. A 1500 Å undoped GaAs buffer layer and a 700 Å Si-doped GaAs layer ($6\times10^{17}/cm^3$) were sequentially grown by MBE on a (100)-oriented semi-insulating 2 in. GaAs substrate. After the semiconductor epilayer growth, the wafer was transferred *ex situ* to an ASM Pulsar2000™ ALD module. A 8-nm-thick Al_2O_3 oxide layer was deposited at a substrate temperature of 300 °C, by using alternating pulses of $Al(CH_3)_3$ (the Al precursor) and H_2O (the oxygen precursor) in a carrier N_2 gas flow. The thickness and uniformity of deposited oxide layer was well controlled at angstrom level. ALD grown Al_2O_3 process results in an abrupt interface with the GaAs substrate, as illustrated by the high-resolution transmission

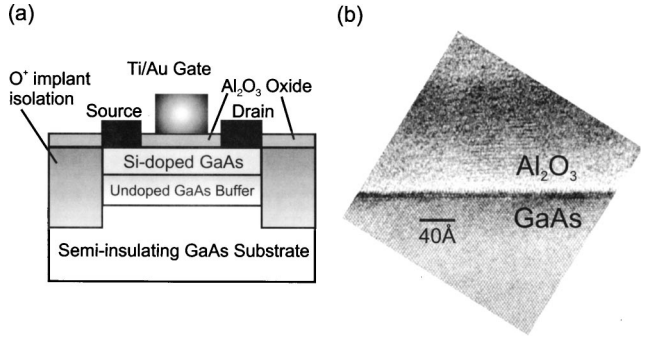

FIG. 1. (a) Schematic view of a depletion-mode *n*-channel GaAs MOSFET with ALD-grown Al_2O_3 as gate dielectric. (b) Cross-sectional high-resolution TEM image of an Al_2O_3/GaAs interface from a similar device.

[a]Electronic mail: peterye@agere.com

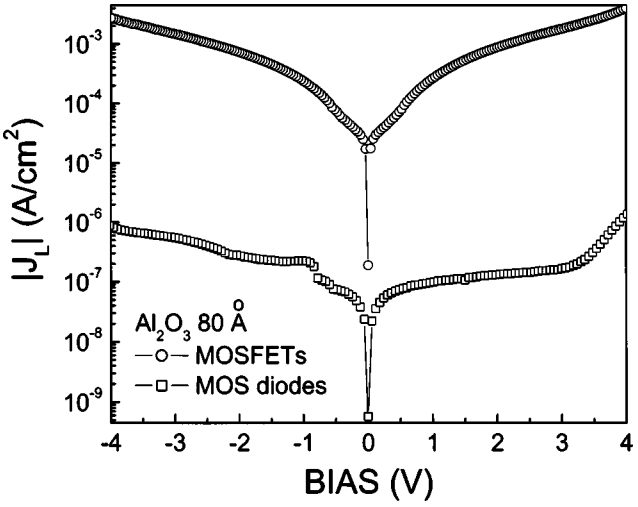

FIG. 2. Measured $I-V$ characteristics for both MOS capacitors (open squares) and MOSFETs between the gate and the source (open circles).

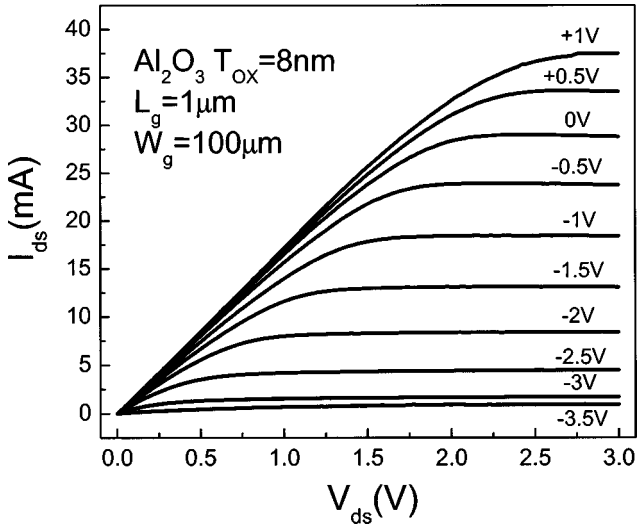

FIG. 3. Drain current vs drain bias as a function of gate bias.

electron microscopy (TEM) image in Fig. 1(b). The oxide layer appears as a desirable amorphous form, while the GaAs exhibits clear lattices. The ALD process removes the native oxide and excess As on GaAs surface, resulting in a very thin Ga–oxide interfacial layer. Medium energy ion scattering experiment suggests as thick as 6 Å Ga–oxide could exist in certain conditions. The interface quality was further improved by a post-deposition anneal at 600 °C for 60 s in an oxygen ambient. Device isolation was achieved by oxygen implantation. Activation annealing was performed at 450 °C in a helium gas ambient. Using a wet etch in diluted HF, the oxide on the source and drain regions was removed while the gate area was protected by photoresist. Ohmic contacts were formed by electron (e)-beam deposition of Au/Ge/Au/Ni/Au and a lift-off process, followed by a 435 °C anneal in a forming gas ambient. Finally, Ti/Au metals were e-beam evaporated, followed by lift-off to form the gate electrodes. The gate length, the source-to-gate, and the drain-to-gate spacings were ~1 μm. The sheet resistance of the channel and its contact resistance, measured by the transfer length method on the same wafer, were 740 $\Omega/\square$ and 1.5 Ω mm. The process requires four levels of lithography (alignment, isolation, ohmic, and gate), all done using a contact printer. The MOS capacitors for oxide characterization were fabricated separately by direct metal deposition through a shadow mask on n^+-GaAs substrate. The gate oxide of MOS capacitors was not exposed to any chemical process after ALD growth.

First, we focus on the intrinsic properties of the ALD oxide itself instead of the finished MOSFETs. The open squares in Fig. 2 show the measured results for the MOS capacitors with 8-nm-thick Al_2O_3 layer, the same thickness as used for the MOSFETs. This insulating layer significantly suppresses the leakage current both in forward and in reverse biases by several orders of magnitude, compared to Schottky diodes in MESFETs. For gate operation between a bias (V_g) of +4 to −4 V, the gate leakage current density is less than 1×10^{-6} A/cm^2. The breakdown voltage is >4 V for an 8-nm-thick Al_2O_3 layer, which corresponds to a breakdown electric field larger than 5 MV/cm. This demonstrates the high electric properties of as-grown ALD films. Considering a much higher dielectric constant, this lower breakdown field is not a penalty compared to SiO_2. Second, we study the gate $I-V$ characteristics of a MOSFET with the same thickness of 8 nm gate oxide. The open circles in Fig. 2 show characteristics of a MOSFET with 1 μm gate length and 100 μm gate width. For gate operation of the same bias range, the gate leakage current density increases by three orders of magnitude, compared to the data from MOS capacitors. Note that the gate leakage current of less than 10^{-3} A/cm^2 or a few hundred picoampere is still several orders of magnitude lower than for MESFETs under similar bias, and is much lower than the channel current. The degradation of oxide quality in MOSFETs is mainly because the gate oxide is not protected in our nonoptimized process flow, as compared to Si CMOS technology, and the Al_2O_3 was exposed to chemicals during processing. The degradation is less pronounced once the oxide thickness is beyond 10 nm. A dry-etch process using self-aligned WSi gate to protect gate oxide directly after ALD growth is under development.

Figure 3 shows the measured drain current versus drain voltage (I_{ds} vs V_{ds}) characteristics of the device. The gate voltage is varied from −3.5 to +1 V with 0.5 V step. The plot shows a clean pinch-off at a gate voltage of −3.5 V. No substantial $I-V$ hysteresis is observed in the drain current drift in comparing forward and reverse gate–voltage sweep directions. This indicates that no significant mobile bulk oxide charge is present and that the density of slow interface traps is low. The MOSFETs can operate under accumulation mode between −1 and +1 V beyond the flatband condition of ~−1.1 V. The flatband condition in the depletion mode MOSFET is roughly at the gate bias where the transconductance g_m appears maximum (see Fig. 4). The more the gate is biased below the flatband condition, the smaller the g_m is, because the distance from the gate to channel increases by increasing depletion width in semiconductor. On the other hand, when the gate bias is above flatband condition, additional carriers are confined to the interface and the gate to channel distance is fixed to the oxide thickness in this accumulation region. But the reduced surface mobility and saturation velocity v_{sat} leads to g_m reduction. That is why g_m vs V_{gs} measurement gives the rough estimation of flatband condition. It is further confirmed by the capacitance–voltage

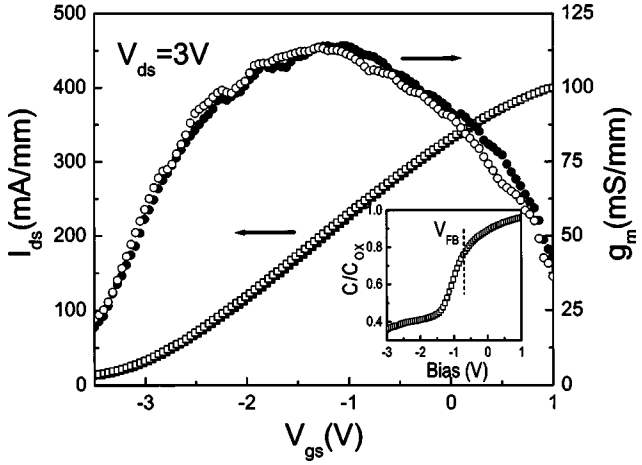

FIG. 4. Drain current vs gate bias in both forward (closed squares) and reverse (open squares) sweep directions. Closed circles (forward) and open circles (reverse) are transconductance vs gate bias at $V_{ds}=3$ V. Inset: $C-V$ characteristic of a MOS capacitor with 8 nm Al_2O_3 on n^+-type (100) GaAs.

($C-V$) measurement (see the inset of Fig. 4) which is widely used to determine the flatband voltage. The good gate modulation or large g_m at accumulate region demonstrates the high quality of Al_2O_3/GaAs interface. Furthermore, as will be reported, the g_m versus frequency study gives an upper limit for interface trap density (D_{it}) of $5\times10^{11}-10^{12}/cm^2$ eV at such Al_2O_3/GaAs structures.[20] The nanometer-thin oxide relaxes the device requirement for D_{it}, because it is easier to realize the condition of $C_{it}\ll C_{ox}$, where C_{it} is the interface-trap capacitance and C_{ox} is the oxide capacitance.

Figure 4 illustrates the drain current as a function of gate bias in both the forward and reverse gate–voltage sweep directions in the saturation region. The device shows almost linear relation of I_{ds} vs V_{gs} in the wide bias range. The slope of the drain current shows that the maximum extrinsic transconductance (g_m) of the 1 μm gate length device is ~120 mS/mm. Both quasilinear I_{ds} vs V_{gs} trace and the broad g_m vs V_{gs} trace show negligible hysteresis in forward and reverse gate–voltage sweep directions. The lack of hysteresis and high g_m near dc further confirms that both fast and slow states are significantly small in our devices. The theoretical intrinsic g_m in saturation regime can be estimated to be ~470 mS/mm by $g_m=v_{sat}\cdot C_{ox}$, where v_{sat} is $\sim5\times10^6$ cm/s in GaAs. Counting on the series resistance of the device $R_s\sim2.5\ \Omega$ mm, the theoretical extrinsic g_m is ~210 mS/mm which is 75% off from the measured peak g_m value. We ascribe this reduction of g_m to the following reasons. First, at the flatband condition, roughly where the peak g_m appears, the total capacitance has two parts including C_{ox} and the capacitance induced by the Debye length. g_m is overestimated by simply using C_{ox} earlier. Second, v_{sat} could become smaller from the bulk value at flatband condition because carriers start to approach to the interface. Third, the existing interface traps ($D_{it}\sim5\times10^{11}-10^{12}/cm^2$ eV) could screen the modulation effect of the gate bias to the channel and reduce the transconductance g_m. Compared to conventional Si-based devices, GaAs MOSFETs show superior high-speed characteristics,[20] because of its much higher electron mobility.

In summary, we have demonstrated ALD-grown insulated gate MOSFETs, using nanometer-thin Al_2O_3 gate dielectric for n-channel depletion-mode GaAs devices. The 1 μm gate length device exhibits a broad extrinsic transconductance of 120 mS/mm with negligible $I-V$ hysteresis, which indicates that the ALD-grown Al_2O_3 film and the Al_2O_3/GaAs interface are of high quality. A thin gate dielectric in nm range is essential for extending downsizing limits of GaAs MOSFETs.

[1] T. Mimura and M. Fukuta, IEEE Trans. Electron Devices **ED-27**, 1147 (1980), and references therein.
[2] *Physics and Chemistry of III–V Compound Semiconductor Interfaces*, edited by C. W. Wilmsen (Plenum, New York, 1985), and references therein.
[3] M. Hong, C. T. Liu, H. Reese, and J. Kwo, in *Encyclopedia of Electrical and Electronics Engineering*, edited by J. G. Webster (Wiley, New York, 1999), Vol. 19, p. 87, and references therein.
[4] S. Tiwari, S. L. Wright, and J. Batey, IEEE Electron Device Lett. **9**, 488 (1988).
[5] C. L. Chen, F. W. Smith, B. J. Clifton, L. J. Mahoney, M. J. Manfra, and A. R. Calawa, IEEE Electron Device Lett. **12**, 306 (1991).
[6] Y. H. Jeong, K. H. Choi, and S. K. Jo, IEEE Electron Device Lett. **15**, 251 (1994).
[7] E. I. Chen, N. Holonyak, and S. A. Maranowski, Appl. Phys. Lett. **66**, 2688 (1995).
[8] J. Y. Wu, H. H. Wang, Y. H. Wang, and M. P. Houng, IEEE Electron Device Lett. **20**, 18 (1999).
[9] T. Waho and F. Yanagawa, IEEE Electron Device Lett. **9**, 548 (1988).
[10] G. W. Pickrell, J. H. Epple, K. L. Chang, K. C. Hsieh, and K. Y. Cheng, Appl. Phys. Lett. **76**, 2544 (2000).
[11] J. C. Ferrer, Z. Liliental-Weber, H. Reese, Y. J. Chiu, and E. Hu, Appl. Phys. Lett. **77**, 205 (2000).
[12] S. Yokoyama, K. Yukitomo, M. Hirose, Y. Osaka, A. Fischer, and K. Ploog, Surf. Sci. **86**, 835 (1979).
[13] J. Reed, G. B. Gao, A. Bochkarev, and H. Morkoc, J. Appl. Phys. **75**, 1826 (1994).
[14] M. Hong, M. Passlack, J. P. Mannaerts, J. Kwo, S. N. G. Chu, N. Moriya, S. Y. Hou, and V. J. Fratello, J. Vac. Sci. Technol. B **14**, 2297 (1996).
[15] M. Passlack, M. Hong, J. P. Mannaerts, R. L. Opila, S. N. G. Chu, N. Moriya, F. Ren, and J. R. Kwo, IEEE Trans. Electron Devices **44**, 214 (1997).
[16] M. Hong, J. Kwo, A. R. Kortan, J. P. Mannaerts, and A. M. Sergent, Science **283**, 1897 (1999).
[17] J. Kwo, D. W. Murphy, M. Hong, R. L. Opila, J. P. Mannaerts, A. M. Sergent, and R. L. Masaitis, Appl. Phys. Lett. **75**, 1116 (1999).
[18] F. Ren, M. Hong, W. S. Hobson, J. M. Kuo, J. R. Lothian, J. P. Mannaerts, J. Kwo, S. N. G. Chu, Y. K. Chen, and A. Y. Cho, Solid-State Electron. **41**, 1751 (1997).
[19] Y. C. Wang, M. Hong, J. M. Kuo, J. P. Mannaerts, J. Kwo, H. S. Tsai, J. J. Krajewski, Y. K. Chen, and A. Y. Cho, IEEE Electron Device Lett. **20**, 457 (1999).
[20] P. D. Ye, G. D. Wilk, J. Kwo, B. Yang, H.-J. L. Gossmann, M. Frei, S. N. G. Chu, J. P. Mannaerts, M. Sergent, M. Hong, K. Ng, and J. Bude, IEEE Electron Device Lett. (to be published).
[21] G. D. Wilk, R. M. Wallace, and J. M. Anthony, J. Appl. Phys. **89**, 5243 (2001).