Photo-assisted capacitance-voltage characterization of high-quality atomic-layer-deposited Al_2O_3/GaN metal-oxide-semiconductor structures

Y. Q. Wu, T. Shen, and P. D. Ye[a)]
School of Electrical and Computer Engineering, Purdue University, West Lafayette, Indiana 47907 and Birck Nanotechnology Center, Purdue University, West Lafayette, Indiana 47907

G. D. Wilk
ASM America, 3440 East University Drive, Phoenix, Arizona 85034

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The authors report on an Al_2O_3 gate oxide deposited on *n*-type GaN by atomic layer deposition technique. The high-frequency *C-V* characteristic shows deep-depletion behavior at room temperature due to the wide band gap semiconductor nature of GaN. Systematic photoassisted *C-V* measurements demonstrate the importance of postdeposition-annealing process which could improve the average interface trap density D_{it} of $(1-2)\times10^{12}/cm^2\,eV$ on the as-grown films to $7\times10^{10}/cm^2\,eV$ on the same films after 800 °C rapid thermal annealing in a N_2 ambient. The high-frequency *C-V* technique or Terman technique is also applied to estimate the mid-gap D_{it} and compare to the results from photoassisted *C-V* technique. © *2007 American Institute of Physics*.
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GaN is a promising semiconductor electronic material for applications in high-temperature, high-speed, and high-power electronics due to its fundamental physical properties such as wide band gap and high saturation velocity. The progress made in GaN electronic device field in the past decade is astonishing.[1] One of the major factors that limit the performance and reliability of GaN high-electron-mobility transistors (HEMTs) to be finally commercialized for rf high-power applications is their relatively high gate leakage and its stability of Schottky contacts at high temperatures. The gate leakage reduces the breakdown voltage and the power-added efficiency while increasing the noise figure. To help solve the problem, the use of atomic-layer-deposited (ALD) gate dielectrics adopted from the state-of-the-art Si complementary metal-oxide-semiconductor (CMOS) technology could be one of the attractive solutions.

In the research front of dielectrics on GaN, significant progress has also been made on GaN metal-insulator-semiconductor high-electron-mobility transistors (MIS-HEMTs) and GaN metal-oxide-semiconductor high-electron-mobility transistors (MOS-HEMTs) using SiO_2,[2–6] Si_3N_4,[7–9] Al_2O_3,[10,11] and other oxides.[12] Recently, there is a growing interest in exploring GaN metal-oxide-semiconductor field-effect transistors (MOSFETs) for digital applications because GaN devices could provide low off drain currents, excellent transport properties, high-quality epilayers on Si, and material compatibility for Si process temperatures. Furthermore, GaN based electronic devices could find wide applications by integrating with GaN optoelectronic devices. The major motivation on GaN MOSFET research is to realize high-performance enhancement mode[13] or even inversion-type devices[14] with scalable gate dielectrics. ALD is a surface controlled layer-by-layer process for the deposition of thin films with atomic layer accuracy. Each atomic layer formed in the sequential process is a result of saturated surface controlled chemical reactions. The thickness control of the ALD films, which is very important for MOSFET scalability, is much superior to the control ability of SiO_2 or Si_3N_4 using plasma-enhanced chemical-vapor deposition. The ALD Al_2O_3 process is *ex situ*, robust, and highly manufacturable. Al_2O_3 offers additional advantages of a large band gap (9 eV), high dielectric constant ($k\sim8.6-10$), high breakdown field (10–30 MV/cm), thermal stability, and chemical stability against GaN. Furthermore, ALD is the most promising approach to high-*k* dielectrics (i.e., HfSiON) and given Si industry's familiarity with ALD for front-end processes, the transition to ALD GaN MOSFETs integrated on Si CMOS platform must be easier. We reported earlier high-performance GaN MOS-HEMTs and depletion-mode GaN MOSFETs with ALD Al_2O_3.[11,15] In this Letter, we report on the systematic photoassisted *C-V* studies of ALD Al_2O_3/GaN MOS structures. The excellent MOS interface property is a must to realize high-performance inversion type of GaN enhancement-mode MOSFETs.

The cross section of an ALD Al_2O_3/GaN MOS capacitor is shown in the inset of Fig. 1(b). A 40 nm undoped AlN buffer layer, a 3 μm undoped GaN layer, and a 100 nm, $5\times10^{17}/cm^3$ Si-doped GaN layer were sequentially grown by metal-organic chemical vapor deposition on a 2 in. sapphire substrate. After the standard RCA cleaning, the wafers were transferred via room ambient to an ASM Pulsar2000™ ALD module. A 40-nm-thick Al_2O_3 layer was deposited at a substrate temperature of 300 °C using alternately pulsed chemical precursors of $Al(CH_3)_3$ (the Al precursor) and H_2O (the oxygen precursor) in a carrier N_2 gas flow. A 200-nm-thick Ni/Au layer was electron-beam deposited and lithographically defined to form circular MOS capacitors with various diameters. Since the *n*-type GaN layer is epitaxially grown on an insulating sapphire substrate, electrical contact to the GaN layer in this work was made via a serial capacitor with an area of approximately 1000 times larger than that of the device under study. An HP4284 *LCR* meter was used for the capacitance measurement. The samples were measured sequentially after they underwent a postmetal-deposition annealing (PMA) of 600–800 °C. The similar results are ob-

[a)]Author to whom correspondence should be addressed; electronic mail: yep@purdue.edu

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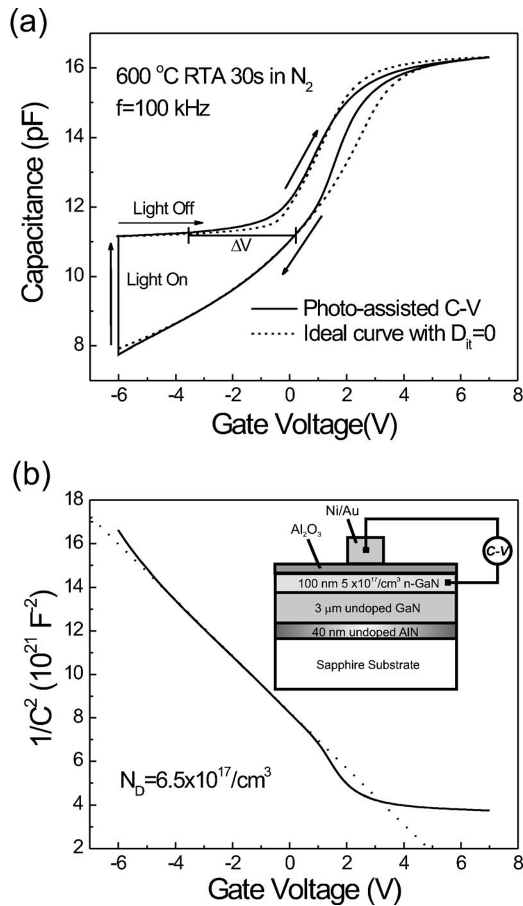

FIG. 1. (a) Photoassisted *C-V* curves on a *n*-type GaN MOS capacitor at room temperature. The sample is swept from accumulation to deep depletion in the dark, held at −6 V and illuminated to form an inversion layer, then swept back to accumulation in the dark. The dashed lines are theoretical calculated curves with $D_{\rm it}=0$ and the dielectric constant of 7.2. The area of the measured capacitor is $\sim 1.0\times 10^{-4}/\mathrm{cm}^2$. (b) $1/C^2$ characteristics as a function of gate voltage. N_d obtained from the slope is $6.5\times 10^{17}/\mathrm{cm}^3$. The dotted line is a guide to the eyes. Inset: schematic view of a GaN capacitor MOCVD grown on sapphire with ALD grown Al_2O_3 as gate dielectric.

tained for postdielectric-deposition annealing (PDA).

The high-frequency *C-V* technique, or Terman technique, is the simplest and most straightforward method for characterizing the interface trap density $D_{\rm it}$ at the SiO_2/Si interface. Unfortunately, this technique does not work well for wide band gap semiconductors such as GaN and can lead to gross underestimation of the interface trap density at room temperature. A quick method for estimating the total number of interface states across the band gap is the room temperature photo-*CV* technique, developed by Tan *et al.* for SiC (Ref. 16) and other groups for GaN.[17–20] The solid curves in Fig. 1(a) show typical photoassisted *C-V* curves measured at room temperature. The gate voltage is swept from accumulation (positive voltage) to depletion (negative voltage) in the dark. A further increase in the negative bias would result in a continual depletion of the GaN, instead of the buildup of an inversion layer, because the minority-carrier generation rate is exceedingly slow for GaN wide band gap semiconductor. Electrons initially captured in the deep-level states cannot emit to the conduction band at room temperature because the emission time constant increases exponentially with energy separation according to the Shockley-Read-Hall statistics.[17] However, if the bias is held at −6 V and the sample is illuminated to populate the inversion layer, a different *C-V* curve emerges. As photogeneration populates the inversion layer, the capacitance rises toward the equilibrium value. After the inversion layer is fully formed, the light is turned off and the sample is swept back toward accumulation. The voltage shift ΔV is caused by electrons trapped in interface states and can be used to estimate the *average* $D_{\rm it}$ across the band gap. This "hysteresis" reflects differences in charging conditions of deep-lying interface states with and without illumination. From the voltage shift ΔV, the average $D_{\rm it}$ can be estimated using the simple equation of $D_{\rm it}=C_{\rm ox}\Delta V/qE_g$,[16] where $D_{\rm it}$ is the average value of interface trap density, $C_{\rm ox}$ is the oxide capacitance, q is the electron charge, and E_g is the band gap of GaN. The average $D_{\rm it}$ of ALD Al_2O_3/GaN is about $(5-6)\times 10^{11}/\mathrm{cm}^2$ eV on 600 °C annealed films, as shown in Fig. 1(a). For an ideal deep-depletion capacitor, coming down in gate voltage from high accumulation, $d(1/C^2)/dV_g$ curve drops from close to zero to a negative point, and then rises steeply to a negative plateau around "threshold" voltage. The negative value of the plateau is directly related with the majority-carrier concentration N_e in GaN since $d(1/C^2)/dV_g=-2/q\varepsilon_s N_e$.[21] The ΔV in this letter is determined by the subtraction of two threshold voltage values from the $d(1/C^2)/dV_g$ vs V_g curves for deep depletion and after illumination. A "unique" parallel rising feature is observed on each two correlated curves in all 16 experimental data sets. The insight of device physics of this parallel feature is under further investigation.

Theoretically calculated ideal high-frequency *C-V* curves is also shown in Fig. 1(a) as dashed lines along with the experimental curves before and after light illumination. The net donor density N_d of $6.9\times 10^{17}/\mathrm{cm}^3$, which is near the experimental fitting in Fig. 1(b), and zero minority carrier is used for deep-depletion *C-V* calculation and N_d of $6.9\times 10^{17}/\mathrm{cm}^3$ and hole carrier density p of $3.0\times 10^{8}/\mathrm{cm}^3$ is used for *C-V* curve after illumination. All device parameters, such as the electron affinity of GaAs and metal gate work function, are appropriately chosen by assuming the lowest $D_{\rm it}$ in GaN located near the mid-band-gap such as Si. These two curves are analyzed using Terman technique. The estimated mid-gap $D_{\rm it}$ is around $5\times 10^{10}/\mathrm{cm}^2$ eV, which is about one order of magnitude better than the value obtained from photoassisted *C-V* method. This leads us to conclude that photoassisted *C-V* measurement is a more reliable technique to study the interface properties of GaN MOS capacitors and to use the Terman technique at room temperature for wide band gap semiconductors in general could grossly underestimate the actual $D_{\rm it}$.

We plot the deep depletion curve of ALD Al_2O_3/GaN after 600 °C RTA annealing in a N_2 ambient as $1/C^2$ versus gate bias V in Fig. 1(b). By fitting the $1/C^2$ vs V curve, the net donor density N_d is extracted to be $6.5\times 10^{17}/\mathrm{cm}^3$, which is reasonably close to the electron density of $5.0\times 10^{17}/\mathrm{cm}^3$ in the conducting channel determined by Hall measurements. The good linear fitting in the depletion region suggests the decent quality of interface and negligible fixed charge in the insulator.

Systematic photoassisted *C-V* studies on ALD Al_2O_3/GaN MOS structures are performed in this work. Figure 2(a) shows the photoassisted *C-V* curves as a function of PMA. The devices are measured sequentially after ALD growth, 600, 700, and 800 °C RTA for 30 s in a N_2 ambient. The voltage shift or "hysteresis" significantly reduces from 2–3 V to ~100 mV with increasing annealing tempera-

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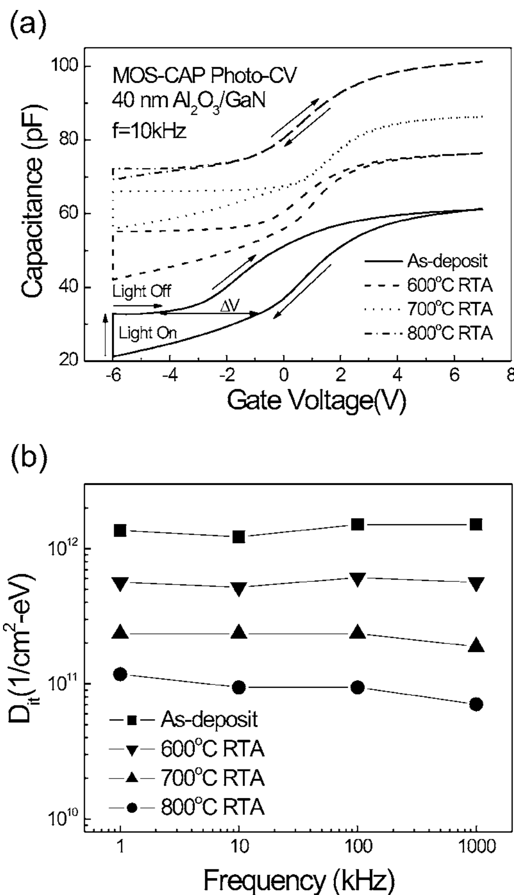

FIG. 2. (a) Photoassisted *C-V* curves as a function of PMA annealing processes. The area of the measured capacitors is $\sim 4.0 \times 10^{-4}/\text{cm}^2$. The curves are shifted vertically for clarity. The absolute values of accumulation capacitance have minor changes due to the change of dielectric constant after different PMA anneals. (b) The calculated average D_{it} vs measured ac frequency as a function of PMA annealing temperatures.

tures. The narrow or negligible hysteresis on 700 or 800 °C annealed devices suggests that the PDA or PMA is a necessary process step to achieve a low interface trap density on MOS structures. Note that no interface-state ledges on the return sweeps are observed on all photoassisted *C-V* curves. Figure 2(b) summarizes the obtained average D_{it} from photoassisted *C-V* measurements versus different measured ac frequencies as a function of the PMA processes. After 800 °C annealing, the D_{it} drops from the low $10^{12}/\text{cm}^2\,\text{eV}$ obtained from as-grown devices to $7 \times 10^{10}/\text{cm}^2\,\text{eV}$. The average D_{it} of $7 \times 10^{10}/\text{cm}^2\,\text{eV}$ is one of the best value reported on GaN MOS structures in literatures.[22,23] ALD Al_2O_3 starts to be partially crystallized above 825 °C annealing and becomes unfavorable as a gate dielectric. The ideal annealing temperature for ALD Al_2O_3/GaN should be between 700 and 800 °C. Some interdiffusion or chemical reaction could occur at the interface after 800 °C PMA, as shown as the less-deep-depletion *C-V* curve in Fig. 2(a). Note that the leakage current of all above measured Al_2O_3 films under the typical operating biases is extremely low (below 10^{-8} A/cm^2).

In summary. electrical characterization of ALD Al_2O_3/GaN interfaces are carried out by the systematic photoassisted *C-V* measurements. The average D_{it} of $7 \times 10^{10}/\text{cm}^2\,\text{eV}$ is achieved after the devices underwent 800 °C RTA annealing. The high-quality Al_2O_3/GaN interface provides the opportunity to realize high-performance inversion-type GaN MOSFETs integrated with high-*k* dielectrics in the Si CMOS platform.

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