Enhancement-mode InP *n*-channel metal-oxide-semiconductor field-effect transistors with atomic-layer-deposited Al_2O_3 dielectrics

Y. Q. Wu, Y. Xuan, T. Shen, and P. D. Ye[a)]
School of Electrical and Computer Engineering, Purdue University, West Lafayette, Indiana 47907 and Birck Nanotechnology Center, Purdue University, West Lafayette, Indiana 47907

Z. Cheng and A. Lochtefeld
AmberWave Systems Corp., 13 Garabedian Drive, Salem, New Hampshire 03079

(Received 23 February 2007; accepted 14 June 2007; published online 11 July 2007)

Enhancement-mode (E-mode) *n*-channel InP metal-oxide-semiconductor field-effect transistors (MOSFETs) with 0.75–40 μm gate length fabricated on a semi-insulating substrate with atomic-layer-deposited (ALD) Al_2O_3 as gate dielectric are demonstrated. The ALD process on III-V compound semiconductors enables the formation of high-quality gate oxides and unpinning of Fermi level on compound semiconductors. A 0.75 μm gate length E-mode *n*-channel MOSFET with an Al_2O_3 gate oxide thickness of 30 nm shows a gate leakage current less than 10 μA/mm at the highest gate bias of 8 V, a maximum drain current of 70 mA/mm, and a transconductance of 10 mS/mm. The peak effective mobility is $\sim$650 $cm^2/V\,s$ and the interface trap density of Al_2O_3/InP is estimated to be $\sim(2-3)\times10^{12}/cm^2$ eV. © *2007 American Institute of Physics*.
[DOI: 10.1063/1.2756106]

With recent announcements from Intel and IBM regarding the implementation of atomic-layer-deposited (ALD) high-*k* gate dielectrics and metal gates in high-volume manufacturing for upcoming complementary metal-oxide-semiconductor (CMOS) integrated circuits (ICs),[1] the potential for novel channel materials for future CMOS ICs is growing. By eliminating SiO_2 as the gate dielectric for the channel surface, a key advantage of Si over compound semiconductors is minimized; there is a growing hope that the ALD high-*k* dielectrics developed for Si may also be applicable to compound semiconductors. Although high-performance depletion-mode (D-mode) GaAs metal-oxide-semiconductor field-effect transistors (MOSFETs) have been demonstrated by various research groups,[2–8] the reported inversion-type enhancement-mode (E-mode) GaAs MOSFETs suffer from relatively low drain current.[9–11] Alternatively, some efforts to improve device performance were carried out to design new device structures using heterojunctions or buried channels to improve the transport quality of the carriers in the channels.[12–14] However, this approach is limited by its scalability to sub-100-nm gate length.

In this letter, we report on fabricating inversion-type E-mode *n*-channel MOSFETs on semi-insulating InP substrates using an ALD Al_2O_3 gate dielectric. Although InP is a commonly used compound semiconductor with wide applications in electronic, optoelectronic, and photonic devices, high-*k* dielectric integration on InP is largely unexplored. Compared to GaAs, InP is widely believed to be a more forgiving material with respect to Fermi-level pinning and has a higher electron saturation velocity (2×10^7 cm/s) as well. Detailed Monte Carlo simulations of deeply scaled *n*-MOS devices indicate that an InP channel could enable high-field transconductance $\sim$60% higher than either Si, Ge, or GaAs at equivalent channel length.[15] It could be a viable material for high-speed logic applications if a high-quality, thermodynamically stable high-*k* dielectric could be found. In the few reported works on InP MOSFETs since the 1980s, SiO_2 was primarily used as gate dielectric and devices suffered from significant current and threshold voltage drift due to the poor semiconductor-dielectric interface[16,17]. Although Fermi-level unpinning was achieved through application of appropriate surface treatment before SiO_2 deposition, current and effective channel mobility remained low and interface trap density was far from applicable[18–21]. By implementing ALD high-*k* dielectrics on InP, we are able to revisit this historically unsolved problem and demonstrate Fermi-level unpinning of InP surface with ALD high-*k* dielectrics.

Figure 1(a) shows the schematic cross section of the device structure of an ALD Al_2O_3/InP MOSFET fabricated on an InP semi-insulating substrate with Fe as deep level traps. After surface degreasing and $(NH_4)_2S$-based pretreatment, the wafers were transferred via room ambient to an ASM F-120 ALD reactor. A 30 nm thick Al_2O_3 layer was deposited at a substrate temperature of 300 °C, using alternately pulsed chemical precursors of $Al(CH_3)_3$ (the Al precursor) and H_2O (the oxygen precursor) in a carrier N_2 gas flow. Source and drain regions were selectively implanted with a Si dose of 1×10^{14} cm^{-2} at 140 keV through the 30 nm thick

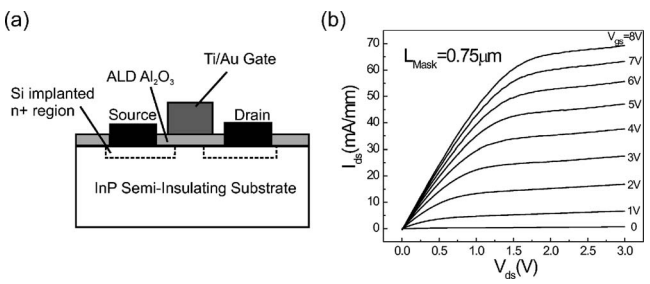

FIG. 1. (a) Cross section of an inversion-channel E-mode Al_2O_3/InP MOSFET. (b) *I-V* characteristic of a 0.75 μm mask gate length InP MOSFET with a 30 nm ALD Al_2O_3 as a gate dielectric.

a)Author to whom correspondence should be addressed; electronic mail: yep@purdue.edu

 © 2007 American Institute of Physics
Downloaded 11 Jul 2007 to 128.46.221.97. Redistribution subject to AIP license or copyright, see http://apl.aip.org/apl/copyright.jsp

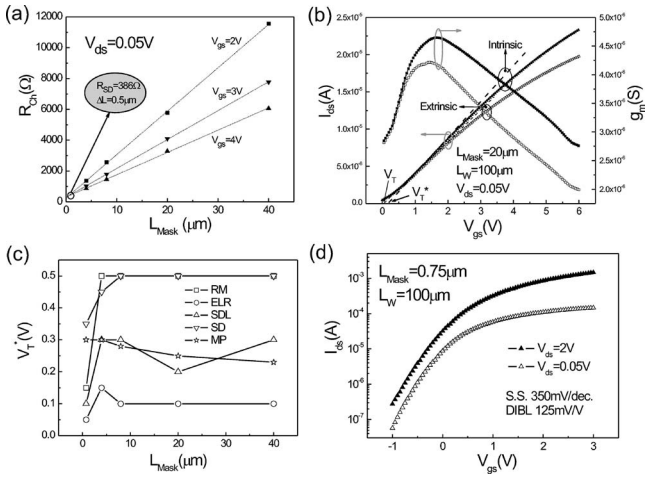

FIG. 2. (a) Measured channel resistance vs different mask gate lengths as a function of gate bias. Three dashed fitting lines are used to determine R_{SD} and ΔL. (b) Extrinsic (empty) and intrinsic (solid) drain currents and transconductance vs gate bias. The dashed lines are guide for the eyes to determine the threshold voltage of the device. (c) The threshold voltage V_{T^*} vs the gate length determined from five different methods using the intrinsic *I-V* characteristics of devices. RM refers to the ratio method; ELR refers to the extrapolation in the linear region method; SDL refers to second derivative logarithmic method; SD refers to second derivative method; MP refers to match-point method. (d) Subthreshold characteristics of a 0.75 μm device. S.S. refers to subthreshold slope and DIBL refers to drain induced barrier lowing.

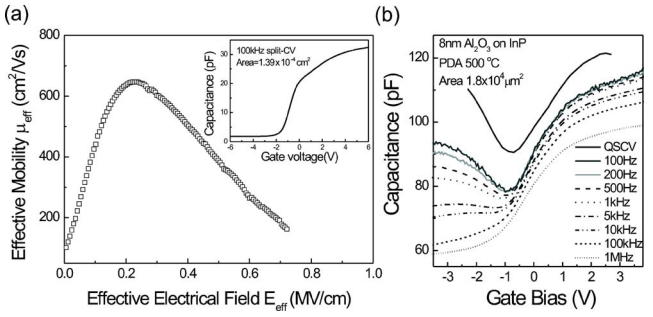

FIG. 3. (a) Effective electron mobility μ_{eff} vs effective electric field E_{eff} on InP substrate with ALD Al_2O_3 as a gate dielectric. Inset: split *C-V* to determine the total inversion charge for the mobility calculation. (b) *C-V* characteristics of 8 nm Al_2O_3/*n*-InP MOS structures at multiple frequencies from 1 MHz down to quasistatic. The data are taken at room temperature and in the dark.

Al_2O_3 layer. Implantation activation was achieved by rapid thermal annealing (RTA) at 720 °C for 10 s in a nitrogen ambient. The source and drain Ohmic contacts were made by an electron beam evaporation of a combination of AuGe/Pt/Au and a lift-off process, followed by a RTA process at 500 °C for 30 s also in a N_2 ambient. The gate electrode was defined by electron beam evaporation of Ti/Au and a lift-off process. The fabricated MOSFETs have a nominal gate length varying from 0.75 to 40 μm and a gate width of 100 μm. Transfer-length-method (TLM) structures were used to determine contact resistance of 2.5 Ω mm and sheet resistance of 230 Ω/sq. at the implanted area. Figure 1(b) shows the dc I_{ds}-V_{ds} characteristic with a gate bias from 0 to 8 V. The measured MOSFET has a designed gate length at mask level (L_{mask}) of 0.75 μm and a gate width (L_w) of 100 μm. A maximum drain current of 70 mA/mm is obtained at a gate bias of 8 V and a drain bias of 3 V. The gate leakage current is below 10 μA/mm under the same bias condition, more than four orders of magnitude smaller than the drain on current. A maximum transconductance g_m is ~10 mS/mm and an output conductance is ~3 mS/mm (V_g=8 V). The typical drain current drift is less than 10% over a 4 h test period.

Figure 2(a) shows the effective gate length (L_{eff}) and series resistance (R_{SD}) extracted by plotting channel resistance R_{ch} vs L_{mask}. R_{SD} and ΔL, which is the difference between L_{mask} and L_{eff}, are determined to be 38.6 Ω mm and 0.5 μm, respectively, by the equation below[22]

$$\frac{V_{ds}}{I_d} = R_{ch} = \frac{L_{eff}}{W\mu_{eff}C_G(V_{GS}-V_T)} = \frac{L_{mask}-\Delta L}{W\mu_{eff}C_G(V_{GS}-V_T)}. \quad (1)$$

The effective electron mobility μ_{eff} is weakly dependent on gate bias from 2 to 4 V and is taken as a constant in this calculation. R_{SD} and L_{eff} are determined as the intercept of the linear fitting of R_{ch} at different gate biases and L_{mask}, as shown in Fig. 2(a). The obtained R_{SD} is consistent with the results from the measurement by TLM technique since R_{SD} includes contact resistance, sheet resistance, accumulation resistance, and spread resistance. The ΔL is caused by the interdiffusion of source and drain implant activations and the proximity effect of photolithography process. To evaluate the output characteristics more accurately, the intrinsic transfer characteristics are calculated by substracting the series resistance R_{SD} and using effective gate length L_{eff} instead of mask gate length L_{mask} and is compared with the extrinsic one, as shown in Fig. 2(b). The intrinsic drain current and transconductance are only about 10% larger than the extrinsic ones due to the large gate length of 20 μm. Figure 2(b) also shows that the subthreshold characteristic is scarcely changed. However, the threshold voltage determined by conventional method of linear region extrapolation does show some difference, as highlighted as extrinsic threshold voltage V_T and intrinsic threshold voltage V_{T^*} in Fig. 2(b). To better extract the threshold voltage, which is an important parameter in E-mode device characterization, several different methods are used to determine V_{T^*} on various gate lengths as presented in Fig. 2(c).[23] It shows that the linear method may not be appropriate to determine threshold voltage for a non-self-aligned process. The second derivative method and ratio method give mostly the same value at the long gate length device and both show V_{T^*} roll-off behavior for the submicron gate length device. Figure 2(d) shows the transfer characteristics of the same device of Fig. 1(b), from which subthreshold slope and drain induced barrier lowing are determined to be 350 mV/decade and 125 mV/V, respectively. The subthreshold slope is relatively large due to the large gate oxide thickness or the small oxide capacitance C_{ox} and the existing interface trap capacitance C_{it}. *m* factor is defined as 60 mV/decade $(1+C_{it}/C_{ox})$. From the measured subthreshold slope, an interface trap density D_{it} of $\sim(2-3)\times10^{12}$/cm^2 eV is determined.

Effective mobility is another important parameter to evaluate the MOSFET performance. "Split-*CV*" method is used to measure the channel capacitance which can be used to calculate the total inversion charge in the channel by integrating the *C-V* curve.[24] The inset of Fig. 3(a) is 100 kHz *C-V* curve between gate and channel measured on a 40 μm gate length device from which inversion capacitance is seen

Downloaded 11 Jul 2007 to 128.46.221.97. Redistribution subject to AIP license or copyright, see http://apl.aip.org/apl/copyright.jsp

clearly. The extracted mobility has a peak value of 650 $cm^2/V\,s$ around a normal electric field of 0.22 MV/cm, as shown in Fig. 3(a). The high Fe dopants in InP substrate after high temperature annealing might affect the transport properties. Work on undoped and *p*-type epi-InP layers is ongoing.

Detailed *C-V* measurements of metal-oxide-semiconductor capacitors are also carried out to evaluate the interface quality of ALD Al_2O_3 on InP. 8 nm thick Al_2O_3 is deposited on a *n*-type InP substrate at 300 °C by ALD. 500 °C postdeposition annealing only improves *C-V* characteristics moderately for InP, as shown in Fig. 3(b), in contrast to the GaAs case[4–6]. The device starts to degrade significantly after 650 °C due to the 8 nm thin Al_2O_3, which is not thick enough as an encapsulation layer for InP high temperature annealing. We ascribe the frequency dispersion at accumulation capacitance to the relatively high D_{it} at the conduction band edge, though the extrinsic parasitic effects could also contribute to the frequency dispersion partly. The midgap D_{it} is estimated to be around $2-3\times10^{12}/cm^2\,eV$ determined by high–frequency (HF)—low-frequency (LF) methods. The value is consistent with the value determined from the *m* factor. Moderate hysteresis of 100–300 mV is exhibited in the *C-V* loops (not shown). The *C-V* characteristics in Fig. 3(b) show a clear transition from accumulation to depletion for HF *C-V* and the inversion features for LF *C-V* and quasistatic *C-V* indicating that the conventional Fermi-level pinning phenomenon[16–21] reported in the literature is overcome in this ALD Al_2O_3/InP sample. We attribute the unpinning of Fermi level to the self-cleaning ALD Al_2O_3 process which removes the native oxide on the InP surface, similar to the situation in the ALD Al_2O_3 on GaAs.[25,26] The unpinning of Fermi level by ALD Al_2O_3 process is significant, as it contributes to the realization of enhancement-mode MOSFET on InP, as demonstrated in Fig. 1(b).

In summary, an inversion-type E-mode *n*-channel InP MOSFET fabricated on a semi-insulating substrate with ALD Al_2O_3 as gate dielectric is fabricated. A maximum drain current of 70 mA/mm and a peak effective mobility of 650 $cm^2/V\,s$ are achieved. Unpinning of Fermi level in InP using ALD Al_2O_3 as the gate dielectric is demonstrated with the midgap $D_{it}\sim(2-3)\times10^{12}/cm^2\,eV$ determined by *m* factor and HF-LF methods. ALD high-*k*/InP is a promising material system for ultimate CMOS technology due to its potentially higher electron mobility and saturation velocity compared to Si.

The authors would like to thank M. A. Alam, M. Lundstrom, G. D. Wilk, W. K. Wang, and J. C. M. Hwang for the valuable discussions. This work was supported in part by NSF (Grant No. ECS-0621949).

[1] http://www.intel.com/pressroom/archive/releases/20060125comp.htm
[2] Y. C. Wang, M. Hong, J. M. Kuo, J. P. Mannaerts, J. Kwo, H. S. Tsai, J. J. Krajewski, Y. K. Chen, and A. Y. Cho, IEEE Electron Device Lett. **20**, 457 (1999).
[3] B. Yang, P. D. Ye, J. Kwo, M. R. Frei, H.-J. L. Gossmann, J. P. Mannaerts, M. Sergent, M. Hong, K. Ng, and J. Bude, J. Cryst. Growth **251**, 837 (2003).
[4] P. D. Ye, G. D. Wilk, J. Kwo, B. Yang, H.-J. L. Gossmann, M. Frei, S. N. G. Chu, J. P. Mannaerts, M. Sergent, M. Hong, K. Ng, and J. Bude, IEEE Electron Device Lett. **24**, 209 (2003).
[5] P. D. Ye, G. D. Wilk, B. Yang, J. Kwo, H.-J. L. Gossmann, S. N. G. Chu, S. Nakahara, H.-J. L. Gossmann, J. P. Mannaerts, M. Sergent, M. Hong, K. Ng, and J. Bude, Appl. Phys. Lett. **83**, 180 (2003).
[6] P. D. Ye, G. D. Wilk, B. Yang, J. Kwo, H.-J. L. Gossmann, M. Hong, K. Ng, and J. Bude, Appl. Phys. Lett. **84**, 434 (2004).
[7] X. Li, Y. Cao, D. C. Hall, P. Fay, B. Han, A. Wibowo, and N. Pan, IEEE Electron Device Lett. **25**, 772 (2004).
[8] S. J. Kang, S. J. Jo, J. C. Han, J. H. Kim, S. W. Park, and J. I. Song, Solid-State Electron. **51**, 57 (2007).
[9] Y. Xuan, H. C. Lin, P. D. Ye, and G. D. Wilk, Appl. Phys. Lett. **88**, 263518 (2006).
[10] F. Ren, M. Hong, W. S. Hobson, J. M. Kuo, J. R. Lothian, J. P. Mannaerts, J. Kwo, S. N. G. Chu, Y. K. Chen, and A. Y. Cho, Solid-State Electron. **41**, 1751 (1997).
[11] S. Oktyabrsky, V. Tokranov, M. Yakimov, R. Moore, S. Koveshnikov, W. Tsai, F. Zhu, and J. C. Lee, Mater. Sci. Eng., B **135**, 272 (2006).
[12] K. Rajagopalan, J. Abrokwah, R. Droopad, and M. Passlack, IEEE Electron Device Lett. **27**, 959 (2006).
[13] M. Passlack, R. Droopad, K. Rajagopalan, and J. Abrokwah, Conference Digest of the 28th IEEE Compound Semiconductor IC Symposium, 2006 (unpublished), p. 250.
[14] Y. Sun, S. J. Koester, E. W. Kiewra, K. E. Fogel, D. K. Sadana, D. J. Webb, J. Fompeyrine, J.-P. Locquet, M. Sousa, and R. Germann, Conference Digest of the Device Research Conference, 2006 (unpublished), p. 49.
[15] M. V. Fischetti and S. E. Laux, IEEE Trans. Electron Devices **38**, 650 (1991).
[16] D. L. Lile and M. J. Taylor, J. Appl. Phys. **54**, 260 (1983).
[17] D. L. Lile, Solid-State Electron. **21**, 1199 (1978).
[18] D. L. Lile, D. A. Collins, L. G. Meiners, and L. Messick, Electron. Lett. **14**, 657 (1978).
[19] T. Kawakami and M. Okamura, Electron. Lett. **15**, 502 (1979).
[20] Y. Shinoda and T. Kobayashi, Solid-State Electron. **25**, 1119 (1982).
[21] W. F. Tseng, M. L. Bark, H. B. Dietrich, A. Christou, R. L. Henry, W. A. Schmidt, and N. S. Saks, IEEE Electron Device Lett. **2**, 299 (1981).
[22] Y. Taur, IEEE Trans. Electron Devices **47**, 160 (2000).
[23] A. Ortiz-Conde, F. J. G. Sanchez, J. J. Liou, A. Cerdeira, M. Estrada, and Y. Yue, Microelectron. Reliab. **42**, 583 (2002).
[24] C. G. Sodini, T. W. Ekstedt, and J. L. Moll, Solid-State Electron. **25**, 833 (1982).
[25] M. M. Frank, G. D. Wilk, D. Starodub, T. Gustafsson, E. Garfunkel, Y. J. Chabal, J. Grazul, and D. A. Muller, Appl. Phys. Lett. **86**, 152904 (2005).
[26] M. L. Huang, Y. C. Chang, C. H. Chang, Y. J. Lee, P. Chang, J. Kwo, T. B. Wu, and M. Hong, Appl. Phys. Lett. **87**, 252104 (2005).

Downloaded 11 Jul 2007 to 128.46.221.97. Redistribution subject to AIP license or copyright, see http://apl.aip.org/apl/copyright.jsp