Enhancement-mode GaAs metal-oxide-semiconductor high-electron-mobility transistors with atomic layer deposited Al$_2$O$_3$ as gate dielectric

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Enhancement-mode GaAs metal-oxide-semiconductor high-electron-mobility transistors (MOS-HEMTs) with *ex situ* atomic-layer-deposited Al$_2$O$_3$ as gate dielectrics are studied. Maximum drain currents of 211 and 263 mA/mm are obtained for 1 μm gate-length Al$_2$O$_3$ MOS-HEMTs with 3 and 6 nm thick gate oxide, respectively. *C-V* characteristic shows negligible hysteresis and frequency dispersion. The gate leakage current density of the MOS-HEMTs is 3–5 orders of magnitude lower than the conventional HEMTs under similar bias conditions. The drain current on-off ratio of MOS-HEMTs is $\sim 3 \times 10^3$ with a subthreshold swing of 90 mV/decade. A maximum cutoff frequency (f_T) of 27.3 GHz and maximum oscillation frequency (f_{max}) of 39.9 GHz and an effective channel mobility of 4250 cm^2/V s are measured for the 1 μm gate-length Al$_2$O$_3$ MOS-HEMT with 6 nm gate oxide. Hooge's constant measured by low frequency noise spectral density characterization is 3.7×10^{-5} for the same device. © *2007 American Institute of Physics.* [DOI: 10.1063/1.2814052]

Unlike normally on depletion-mode (D-mode) transistors, normally off enhancement-mode (E-mode) devices exhibit low static power consumption and constitute the backbone of today's Si digital circuitry. Normally off, E-mode GaAs metal-semiconductor field-effect transistors (MESFETs) and GaAs high-electron-mobility transistors (HEMTs) have been demonstrated by various research groups.[1–4] However, in GaAs MESFETs and HEMTs, the Schottky-contact gate formation suffers from high leakage current, which limits the input dynamic range, increases the noise figure, and prevents the large scale integration of these transistors. In order to restrain the gate leakage current, insulating layers were introduced between metal gates and compound semiconductors through different techniques such as *in situ* molecular beam expitaxy (MBE) Ga$_2$O$_3$(Gd$_2$O$_3$) (Refs. 5–7) or *ex situ* atomic-layer-deposited (ALD) high-k dielectrics.[8–13]

In this letter, we report E-mode GaAs metal-oxide-semiconductor (MOS) HEMTs using *ex situ* ALD Al$_2$O$_3$ as gate dielectric. The high electron-mobility channel is still at AlGaAs/InGaAs heterojunction like HEMT, though high-k dielectric is introduced to significantly reduce the gate leakage current. Al$_2$O$_3$ has a high bandgap ($\sim$9 eV), a high breakdown electric field (5–30 MV/cm),[14] high thermal stability (up to at least 850 °C), and a good interface quality on GaAs.[15] The disadvantage of Al$_2$O$_3$ is its relatively low k value (8.6–10), compared to HfO$_2$ (20–26).[16]

Figure 1(a) shows the cross section of the ALD high-k GaAs MOS-HEMT structure. Using MBE, a 5 nm undoped Al$_{0.20}$Ga$_{0.80}$As, 12 nm undoped In$_{0.20}$Ga$_{0.80}$As and 23 nm undoped Al$_{0.20}$Ga$_{0.80}$As (4×10^{12} cm^2 Si δ-doping layer located 3 nm above InGaAs), 1.5 nm n-doped 1×10^{18} cm^{-3} AlAs etch stop layer, and 60 nm n-doped 5×10^{18} cm^{-3} GaAs top layer have been sequentially grown on a GaAs buffer layer and 4 in. semi-insulating GaAs substrate. Device isolation is achieved by oxygen implantation. Gate recess is performed

by wet etching using succinic acid and hydrogen peroxide solution at PH value equal to 4.2. The AlAs etch stop layer could be easily removed by hydrochloric acid solution (HCl:H$_2$O=1:1). After recess, the wafers are treated by ammonia-based surface treatment[15] and are subsequently transferred to an ASM F-120 ALD reactor for Al$_2$O$_3$ growth followed by a 600 °C postdeposition annealing. The drain and source Ohmic contacts are formed by electron-beam evaporation of Au/Ge/Au/Ni/Au metal layers and lift-off process. The metallization annealing is done in rapid thermal annealing at 400 °C, nitrogen ambient for 30 s. Gate oxide etch-back process is performed using diluted buffered oxide etch followed by the formation of electron-beam evaporated high work-function Pt/Au metal gate electrodes.[7] The purpose of the gate oxide etch back is to remove the impurities at the surface of ALD dielectrics such as residual arsenic oxide (As$_2$O$_5$) (Ref. 17) and contaminants from photoresist which could otherwise degrade the metal-oxide interface. The source-gate and drain-gate spacings are 3 and 6 μm, respectively. E-mode HEMTs with gate oxide completely etched away are also fabricated for comparison.

We first focus on a GaAs MOS-HEMT with 3 nm Al$_2$O$_3$ as gate dielectric. Figure 1(b) shows well-behaved dc I_{ds}-V_{ds} characteristic with a gate bias from 0 to 3.5 V in steps of +0.5 V. The measured MOS-HEMT has a gate length L_g of
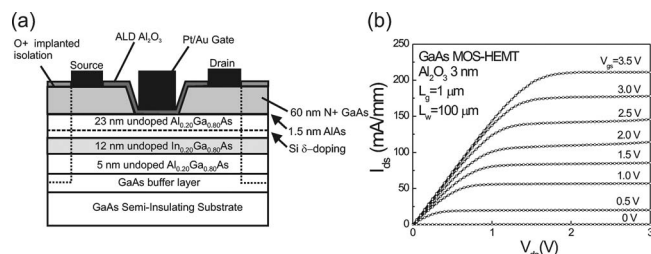

FIG. 1. (a) A cross section of an E-mode Al$_2$O$_3$/GaAs MOS-HEMT and (b) *I-V* characteristic of a 1 μm gate-length GaAs MOS-HEMT with a 3 nm ALD Al$_2$O$_3$ as a gate dielectric.

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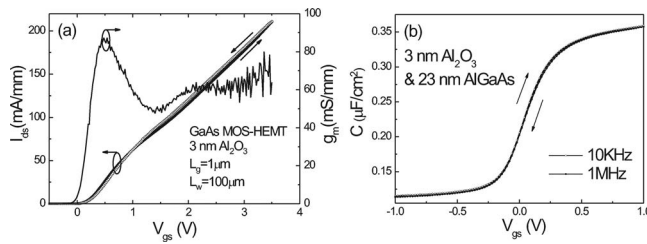
FIG. 2. (a) Drain current vs gate bias in both forward (filled circles) and reverse (empty circles) sweep directions. The solid line is extrinsic transconductance vs gate bias at $V_{ds}=3$ V. (b) Bidirectional 10 KHz and 1 MHz gate capacitance vs gate voltage with both source and drain grounded.

1.0 μm and gate width L_w of 100 μm. A maximum drain current of 211 mA/mm is obtained at a gate bias of 3.5 V and a drain bias of 3 V. Figure 2(a) illustrates the drain current as a function of the gate bias in both forward and reverse sweep directions in the saturation region. The I_{ds} vs V_{gs} shows negligible hysteresis. The extrinsic peak transconductance G_m is $\sim$90 mS/mm. The intrinsic peak G_m is $\sim$116 mS/mm by considering the access sheet resistance of 1.5 Ω mm at the source side and the contact resistance of 1.0 Ω mm measured from transmission line method. Threshold voltage (V_T) of 0.21 V is extracted from the drain current versus gate voltage data by linear extrapolation technique at the peak transconductance gate bias and 0.3 V drain bias.

Figure 2(b) shows 10 KHz and 1 MHz bidirectional C-V measurements on the same device of Figs. 1(b) and 2(a). Four traces are completely overlapped with near zero hysteresis and frequency dispersion. The accumulation capacitance value is reasonably consistent with the theoretical value for 3 nm Al_2O_3 and 23 nm AlGaAs. These excellent C-V characteristics and negligible hysteresis in I-V characteristics demonstrate that the high quality of Al_2O_3/AlGaAs interface is achieved. More studies are needed to understand what and how the potential traps at Al_2O_3/AlGaAs interface could affect I-V and C-V characteristics on MOS-HEMT structures.

For MOS-HEMTs with 6-nm-thick Al_2O_3 gate dielectric, the shift in V_T compared to the device with 3 nm gate dielectric is about 0.02 V (quasi-E mode[7]) while the maximum drain current, extrinsic peak G_m, and intrinsic peak G_m are improved to 263, 165, and 275 mS/mm, respectively.

As shown in Fig. 3(a), the good MOS interface quality is further verified by comparing the subthreshold characteristic of MOS-HEMTs of two oxide thicknesses and a similarly designed HEMT. The subthreshold swing of all three devices is $\sim$90 mV/decade. The introduced Al_2O_3/AlGaAs interface does not degrade the device on-off performance. From the m factor, defined as 60 mV/decade $(1+C_{it}/C_{ox})$, the interface
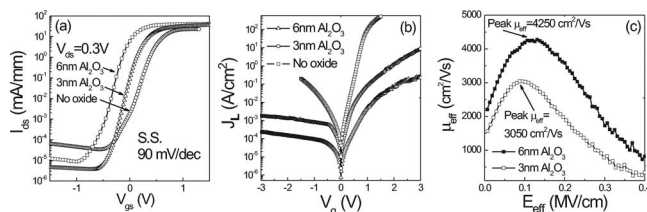

FIG. 3. (a) Subthreshold characteristics of three devices with 3 nm Al_2O_3, 6 nm Al_2O_3 and without oxide at $V_{ds}=0.3$ V. (b) Gate leakage characteristics of the same three devices with both source and drain grounded. (c) Effective mobility vs effective field measured from 20 μm gate-length devices at $V_{ds}=0.3$ V.

trap density (D_{it}) is estimated to be $\sim$1$\times$10^{12}/cm^2 eV. Here, C_{ox} is the serial capacitance of Al_2O_3 and AlGaAs layers and C_{it} is the existing interface trap capacitance. The gate leakage characteristic of the same three devices is also presented in Fig. 3(b). By inserting a 3–6 nm thin oxide layer, gate leakage current is significantly reduced by 3–5 orders of magnitude depending on different gate bias conditions. The ultrathin dielectric can also prevent the downgrading of subthreshold swing on HEMT due to higher gate leakage, as shown in Fig. 3(a). The I_{on}/I_{off} ratio is 3$\times$10^3 at $V_{gs}=3$ V (on), $V_{gs}=0$ V (off), and $V_{ds}=3$ V. The channel effective mobility of the MOS-HEMTs is deduced from I-V of the transistors with $L_g=20$ μm and the accumulation capacitance measured in Fig. 2(b). Peak effective mobility values of 3050 cm^2/V s (3 nm oxide) and 4250 cm^2/V s (6 nm oxide) are obtained in Fig. 3(c). These effective mobility values are among the highest reported for GaAs devices.[7,11] The high effective mobility is beneficial from high low-field electron mobility of InGaAs and modulation-doping heterostructures, while the maximum drain current is limited by saturation velocity when the gate length approaches 5–10 μm and $V_{ds}=3$ V. There is no significant degradation of effective mobility from Hall mobility due to the low D_{it} at the Al_2O_3/AlGaAs interface and well-controlled device fabrication process.[11] The 6 nm oxide MOS-HEMT exhibits higher transconductance and channel mobility due to its lower threshold voltage.

The S-parameters of both device and probe pads are measured under different bias conditions up to 40 GHz and de-embedding is done according to the three step deembedding technique introduced by Vandamme *et al.*[18] The maximum cutoff frequency (f_T) and maximum oscillation frequency (f_{max}) of the MOS-HEMTs are determined by varying the gate bias condition. Under 3 V drain bias and 0.7 V gate bias, maximum f_T and f_{max} for the 3 nm Al_2O_3 MOS-HEMT are 10.9 and 13.8 GHz, respectively. For the 6 nm Al_2O_3 MOS-HEMT under the same biasing conditions, f_T and f_{max} are improved to 27.3 and 39.9 GHz, respectively. Note that the higher f_T and f_{max} of the 6 nm Al_2O_3 MOSHEMT reflect the larger transconductance value of the device.

Low frequency noise measurement is an additional approach to study MOS interface properties. To further evaluate the interface quality of the present GaAs MOS-HEMTs, the low frequency noise ($1/f$) spectral density of the drain in the linear operating regime is measured and the value of Hooge's constant α_H is extracted. The α_H value for 3 nm Al_2O_3 MOS-HEMT is about 3.7$\times$10^{-5}, which is slightly higher than 6.0$\times$10^{-6} measured from HEMTs and much superior to the value of 1.0$\times$10^{-3} obtained from HfO_2/Si MOSFETs.[19] Note that the commercial GaAs MESFETs have α_H values of 5.6–7.6$\times$10^{-5} (Ref. 20).

In summary, we have demonstrated E-mode GaAs MOS-HEMTs with *ex situ* ALD Al_2O_3 as gate dielectric. The E-mode operation is realized by implementation of gate recess and high work-function gate metal to shift the V_T,[7] being different from the traditional inversion-type E-mode devices. The high-mobility electrons are constrained in semiconductor heterojunctions or quantum wells instead of oxide-semiconductor interfaces. Due to the need of thick AlGaAs layer to confine electrons, the devices are hard to scale down to 100 nm for ultimate CMOS applications. However, these devices may find a wide range of applications in the

traditional compound semiconductor fields such as wireless electronics or optoelectronics. Similar device performance is also demonstrated by using ALD HfO_2 or HfO_2/Al_2O_3 nanolaminates as gate dielectrics.

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