Concurrent Characterization of GaN MOSHEMT Gate Leakage via Electrical and Thermoreflectance Measurements

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(Dated: 22 November 2023)

In this work, we report the first concurrent use of electrical and thermal characterization, via thermoreflectance, to analyze Time Dependent Dielectric Breakdown in GaN MOSHEMTs. Electrically stressing the devices until a failure occurs, then evaluating them via thermoreflectance, revealed a geometric dependence of the failure mode. All soft breakdowns occurred at the mesa edge where the electric field strength was at its strongest, and tunneling current density was at its highest. This breakdown phenomenon at the mesa edge has been seen previously in GaN HEMTs employing a mesa architecture. Possible approaches to mitigate these failures in MOSHEMTs are proposed.

Keywords: GaN MOSHEMT, GaN MISHEMT, time dependent dielectric breakdown

I. INTRODUCTION

Power electronics that convert alternating to direct current play a critical role in electrical infrastructure; from personal transportation to grid-level battery storage. The current state-of-the-art technology in power electronics is the gallium nitride (GaN) high electron mobility transistor (HEMTs). GaN HEMTs' larger bandgap material and higher operating voltage allow more efficient operation than metal-oxide-semiconductor field effect transistors (MOSFETs), but do come with the drawback of higher gate leakage currents. GaN MOSHEMTs are an attractive successor to GaN HEMTs. The addition of the oxide reduces the gate leakage current, but also introduces new failure modes centered around the gate oxide. The reliability of the gate oxide and understanding how its rate of degradation is influenced by field[1–4], temperature[1,4,5] and device architecture is imperative before GaN MOSHEMTs can be widely adopted.

GaN HEMT and MOSHEMT failure mechanisms currently being researched include Time Dependent Dielectric Breakdown (TDDB)[3,6–9], Positive[10–12] and Negative[13] Bias Temperature Instability (BTI), and Inverse Piezoelectric Effect (IPE)[14,15]. The failure mode of interest in this work is the Time Dependent Dielectric Breakdown of the gate oxide. TDDB refers to a process whereby a dielectric under a constant stress, will break down with increasing time. TDDB can occur in both enhancement (E-mode) and depletion mode (D-mode) GaN MOSHEMTs. E-mode devices feature a recessed gate[16–19] that locally displaces part of the dielectric stack responsible for inducing the polarization that causes the 2DEG to form. D-mode devices feature non-recessed gates[20–22] where the 2DEG is continuous between source and gate with no gate voltage applied. The devices characterized in this work are D-mode GaN MOSHEMTs.

In the early days of CMOS manufacturing, oxides were thick and operating voltages were high. When a percolation path formed through an oxide, it would lead to a sudden increase in gate leakage current by many orders of magnitude. This formation of an ohmic shunt between the gate and channel would render the transistor failed/broken. This is referred to as hard breakdown.

As CMOS manufacturing technology improved and gate oxides were made thinner to increase device speed, it was discovered that thin oxides don't immediately undergo catastrophic failure as thicker oxides tend to do. Over time, electrons tunneling through the oxide stochastically generate internal defects, causing a gradual uniform increase in the gate leakage current called stress-induced leakage current (SILC). The mechanism of SILC was determined to be the increase in trap-assisted tunneling[23,24] via additional defects created by electrons tunneling through the oxide. Therefore, SILC measurements are an effective way to measure bulk trap density[25].

When the localized defect density reaches a critical value, a percolation path forms and a localized increase in current occurs. The gate operating voltage is not sufficiently high to cause a catastrophic failure, but instead a localized high conductance path through the oxide is formed, referred to as soft breakdown[8,26,27]. Imaging of these localized leakage pathways has been successfully performed previously using methods such as thermoreflectance for Si[28] and InGaAs[29] devices. In this work, we report the first concurrent use of electrical and thermal characterization, via thermoreflectance, to analyze TDDB in GaN MOSHEMTs using an amorphous Al_2O_3 gate oxide. This concurrent characterization captures any structural or location based data that would be unavailable with a purely electrical characterization.

The most important difference between amorphous Al_2O_3 (am-AlO) and crystalline Al_2O_3 is the bandgap. The bandgap strongly affects the breakdown voltage, making it vital that the am-AlO used in GaN MOSHEMTs is of the highest quality; as crystalline Al_2O_3 has a bandgap of 8.7eV[30], sapphire is approximately 10eV[31], and am-AlO can range from 3.2eV to 7.3eV depending on the fabrication process[30,32–35]

II. METHODS

Our process flow for testing and characterization is outlined in Figure 1, and will be discussed in further detail throughout

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this section. Initial device fabrication was followed by determination of the stress bias to be used for CV stress. Next, individual devices were characterized to determine if they were of sufficient quality to warrant stress tests. Devices that passed this test, were stressed using stress-recovery cycles until they underwent soft breakdown. During this process, they were checked for breakdown after each stress cycle. After electrical stress and characterization was completed, a subset of devices underwent additional stress while being monitored using thermoreflectance (TR) thermal imaging microscopy. Thermoreflectance imaging is a non-contact method that can map the temperature distribution of reflecting surfaces with submicron spatial resolution[36–41]. Here TR imaging was used to optically detect localized heating in the MOSHEMT gate metal and determine how it relates to the power dissipated in the percolation path.

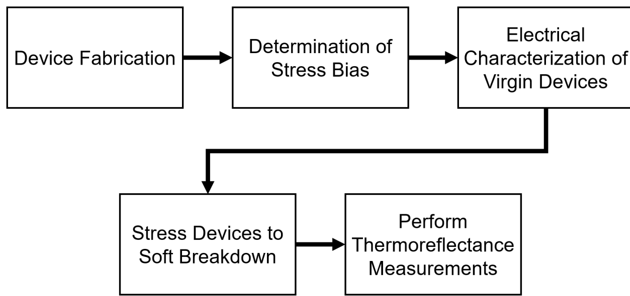

FIG. 1. Outline of Fabrication and Characterization Process for GaN MOSHEMTs. After fabrication, a series of electrical measurements is performed, followed by thermoreflectance imaging to obtain multiple sources of information about device failure.

The characterization and analysis was performed on prototype laboratory devices, with all tested devices co-located on the same sample. The architecture of the device under test (DUT), shown in Figure 2b, is a depletion mode GaN MOSHEMT with an amorphous 5 nm Al_2O_3 gate oxide applied via atomic layer deposition (ALD). The dimensions that vary between fabricated devices are channel length, ranging from 6.8 to 35.8 µm, and channel width at 10 or 20 µm. Four devices have a gate-to-source distance of 1.25 µm and gate length of 3.35 µm. Remaining devices have a gate-to-source distance of 1.5 µm and gate length of 4.4 µm. Subtracting the gate-to-source distance and gate length from the channel length gives the gate-to-drain distance. An optical micrograph of a representative device is provided in Figure 2a. Further information related to device fabrication can be found in Zhou et al.[42,43].

Measurements were taken using tungsten probes from Micromanipulator, mounted on a Micromanipulator 6000 probe station in a dark box on top of a vibration isolation table, connected to a Keithley 4200SCS Semiconductor Parameter Analyzer. Our experiments were performed in the dark at room temperature. Substrate temperature was not monitored or actively controlled.

Prior to performing TDDB testing, a group of four devices was tested to determine the appropriate stress bias. With the drain and source grounded, the gate bias was swept from 0

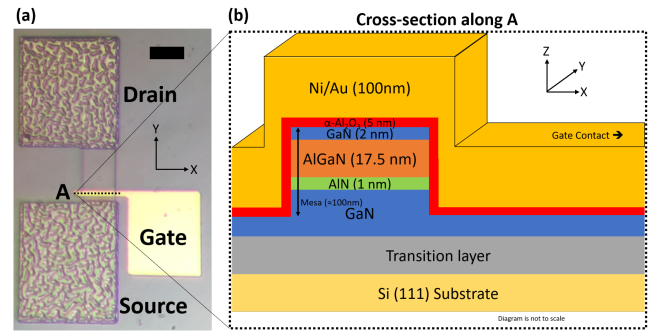

FIG. 2. a) Optical image of sample device. Reference line in figure is 20 µm long. b) Cross-section along line 'A' from (a) shows device mesa layering as well as conformal gate oxide and gate electrode.

to +5V while measuring gate current. Hard breakdown was found to occur, for all devices, at approximately +4.5V; see Figure 3. Devices were then stressed by cycling the gate voltage from 0V to +4V and back to 0V to determine at what voltage oxide defect density no longer influenced gate leakage current; this was found to be +3.4V. This voltage was chosen as the stress bias to keep the resulting gate leakage currents relatively constant as additional defects were generated in the oxide. Additionally, the gate oxide was characterized at both forward and reverse bias conditions for comparison to other GaN MOSHEMTs; example I-V curve shown in Figure 4. In reverse bias, the 2DEG is depleted and measured gate leakage current is low enough that it is not discernable from noise. This is consistent with the behavior seen in other high quality GaN MISHEMT devices[3,42,44,45].

Our experiments were performed in the V_{DS} = 0V state; with DC bias applied to the gate and the source and drain remaining grounded at all times. Prior to degradation, the gate voltage was swept from -0.5 to +3.4V while measuring gate current, to determine if the virgin device gate oxide was al-

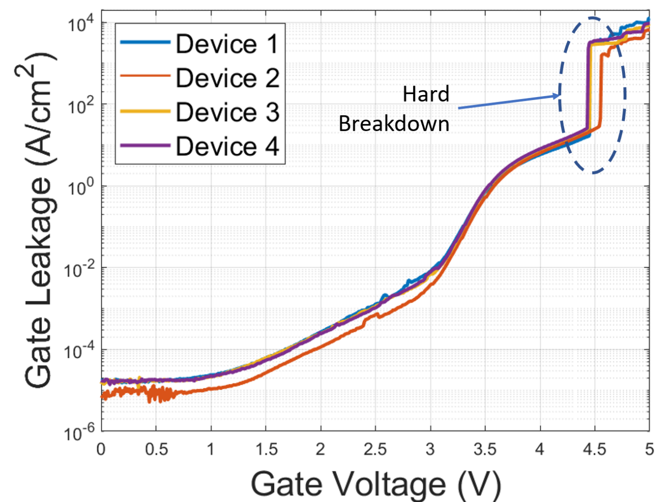

FIG. 3. I-V plots of four virgin devices that were stressed beyond hard breakdown to determine desired stress bias

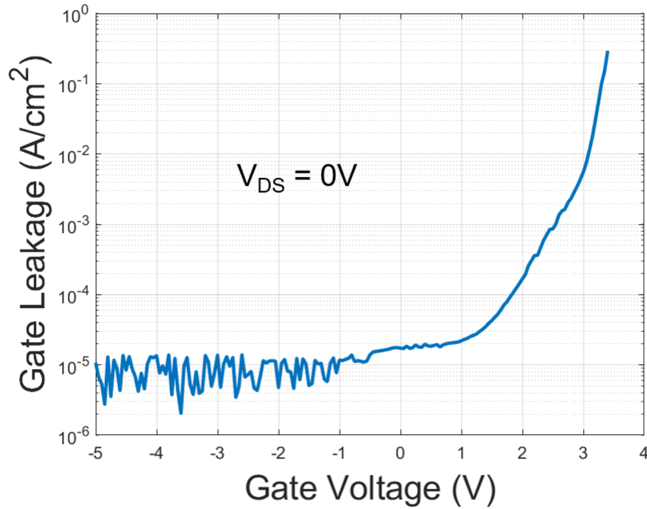

FIG. 4. I-V curve of representative device testing the gate terminal in forward and reverse bias conditions.

ready in the soft breakdown regime; attributed to fabrication defects. Once it was determined that a device was not in soft breakdown, stress testing began.

Testing soft breakdown of each device, 27 in total, consisted of one or more test cycles performed repeatedly until a stop condition was reached. A test cycle includes a stress-recovery degradation period and a post degradation sweep. Degradation consists of biasing the gate to +3.4V for 30 seconds, then 0V for 15 seconds. Immediately following degradation, a post degradation sweep identical to the initial device sweep was performed; typically lasting 2.5 seconds. Evaluation sweeps were determined to have a negligible effect on device degradation due to the minimal time spent at elevated voltages. Test cycles were repeated until a step change in the gate leakage current, measured at V_G = +3.4V, was observed.

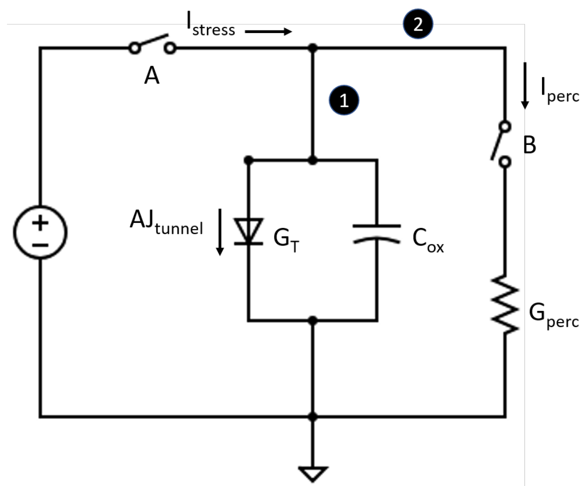

FIG. 5. Circuit equivalent of model used to characterize soft breakdown via two conditions: Stress bias applied before a breakdown event (Switch A closed and Switch B open) and breakdown event while stress bias applied (Switches A and B closed)

The theoretical model for soft breakdown of the gate oxide is based on the SiO_2/Si percolation model by Alam et al.[8], using a constant voltage stress, as shown in Figure 5. Figure 5 contains a voltage source and two possible paths for current to flow. For a virgin device that has not undergone soft breakdown, Switch 'B' is open because no percolation path exists. Stress testing begins by closing Switch 'A' and current flows through Path 1 which 1) charges the capacitor created by the gate/oxide/2DEG and 2) causes tunneling current to flow from the gate electrode to the channel with a conductance of G_T. With no percolation path having formed yet, stress current equals tunneling current. When a percolation path forms through the oxide, Switch 'B' closes and stress current now flows through Path 1 and Path 2. Stress current is now the sum of tunneling current and percolation path current; Equation (1). Percolation path current is approximately two orders of magnitude larger than tunneling current and is a function of voltage and the percolation path conductance, Equation (2),

$$I_{stress} = AJ_{tunnel} + I_{perc} \tag{1}$$

$$I_{perc} = G_0 V^{\delta}, \tag{2}$$

where A is the area of the gate and J_{tunnel} is tunneling current density. The power law fitting parameters, G_0 and δ, for each device can be found using the following equations:

$$\delta = \frac{\ln\left(\frac{I_1}{I_2}\right)}{\ln\left(\frac{V_1}{V_2}\right)} \qquad G_0 = \frac{I_{perc}}{V^{\delta}}, \tag{3}$$

where I_1 and I_2 are currents measured at gate bias points +0.5V and +3.4V. The voltages of +0.5V and +3.4V, V_1 and V_2 respectively, were chosen in order to avoid noise at low currents near 0V and prevent stressing of devices during I-V data collection. Prior literature has focused on calculating values of δ to determine the level of nonlinearity of the breakdown in specific devices, so subsequent analysis will focus on this value.

Following CV stress tests, a subset of seven devices were imaged using thermoreflectance (TR) microscopy to inspect for localized heating due to percolation path current passing through the gate dielectric. I-V data for each device was taken before and after TR imaging. A thermoreflectance measurement is based on the temperature dependence of a material's reflectance. Because the magnitude of material thermoreflectance is very small for most materials, on the order of one part in 10,000 for each degree Kelvin, measurements with good temperature resolution require averaging. Our imaging method uses lock-in amplification. The device under test was modulated by a low duty-cycle voltage pulse signal with repetition rates in the kilohertz range. Resulting modulation of device reflectance over the microscope's full field of view was recorded by a camera and averaged for several minutes.

Thermoreflectance magnitude varies for different materials and for different wavelengths of incident illumination. Our study imaged the top gold surface of the MOSHEMT gate. For incident illumination of 530 nm, the thermoreflectance response of the gold gate was experimentally determined to be

$3.1(3) \times 10^{-4}\,\mathrm{K}^{-1}$. Averaging for ten minutes produced images with noise floor of 0.09 K. The TR data was overlaid with the optical image of a microscope to give the final image. Diffraction limited spatial resolution in the TR image was calculated to be 640 nm using a 0.7 numerical aperture, 100X objective, and 530 nm incident illumination. Spatial resolution of the images was an important metric in this study, as the size and localization of hotspots due to stress induced gate leakage are not known. Other methods such as light emission microscopy[46,47] have been used previously to determine oxide breakdown location, via emission of IR radiation, but diffraction limited spatial resolution is typically greater than one micron using IR based methods. TR imaging can achieve an order of magnitude better spatial resolution using visible wavelength illumination.

The TR setup used to collect images is a hand-built setup. The process for gathering TR data began with establishing good probe contact at the device source, drain, and gate. Then a manual I-V measurement was taken by keeping the source and drain grounded, and sweeping the gate bias from -0.5V to +3.4V. Thermal images were then collected using 500 μsec pulses with a 20% duty cycle, at the desired gate bias, and an averaging time of ten minutes. The gate bias was increased for successive images from 0V to +3.4V. Once all images were collected, a post-imaging manual I-V measurement was performed in the same manner as before. The setup has a spatial resolution of 800 nm and a temperature resolution of 10 mK. Spatial resolution is diffraction limited, with the numerical aperture equal to 0.7, and incident illumination of 530 nm. The minimum measurable temperature is 90 mK above equilibrium; the noise floor.

III. RESULTS AND ANALYSIS

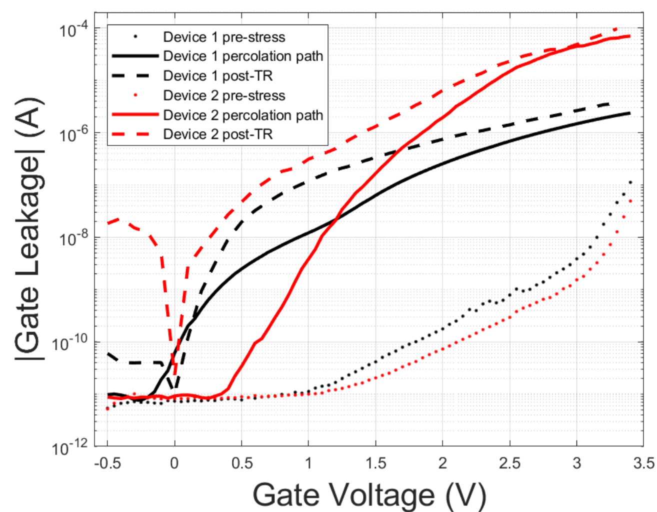

FIG. 6. I-V curves for two representative devices at three different stages of the experiment: 1) pre-stress 2) post-soft breakdown and 3) post-thermoreflectance. The Device 1 percolation path has a δ of 3.58 and the Device 2 percolation path has a δ of 7.72.

Prior to stress testing, all virgin devices yield similar I-V characteristics to those observed during stress bias determination; see Figures 3 and 6. This behavior includes no detectable change in gate current from -0.5V to +0.5V, then a region of exponential growth up to approximately +3V, and a final steeper region from +3V to +3.4V. I-V data immediately prior to soft breakdown was subtracted from post-breakdown I-V data to capture the I-V characteristic of the percolation path itself; see Figure 6. Some devices show a percolation path current minimum at a non-zero value. This is due to current values near the noise floor being subtracted from one another and has no physical significance; hence $V_1 = +0.5$V. Applying Equation 3 to the percolation path I-V data at +0.5V and +3.4V, gives min/mean/max δ values of 3.5/4.8/8.1.

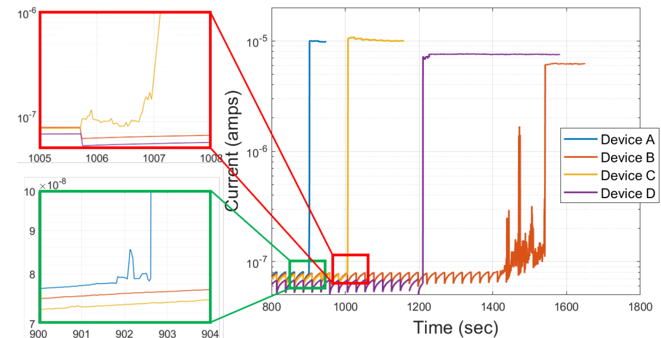

FIG. 7. Evolution of gate leakage current of four representative devices. Devices A, B, and D all undergo progressive breakdown (PBD), ranging from a few seconds to a few minutes, before a percolation path is formed. Device C on the other hand, shows no signs of progressive breakdown on any time scale.

Data regarding the amount of stress each device underwent prior to soft breakdown was also collected. Figure 7 displays the evolution of gate leakage current of four devices which are representative of the different breakdown behaviors seen across all 27 devices. All four devices shown have similar pre-breakdown gate leakage currents at the stress voltage, show a step change in current after formation of a percolation path, and then stabilize at a higher leakage current. The difference in current between pre-breakdown and post-breakdown current is the current from the percolation path; which as mentioned earlier is approximately two orders of magnitude larger than the tunneling current. Where the devices differ is the behavior immediately prior to breakdown. The unpredictable variations in leakage current prior to soft breakdown seen in most devices are referred to as progressive breakdown (PBD)[6]. The duration of PBD prior to soft breakdown ranges from one second for Device C to 2.5 minutes for Device B. There were a few notable exceptions that featured no PBD, such as Device D.

Figure 8 shows a Weibull plot of fluence for most devices. Fluence was used instead of time since the gate leakage currents are not completely identical and using fluence accounts for this variability. The β value is slightly less than one meaning the devices are wearing out consistently as time increases. The following variables were then examined for any correlations: 1) fluence to soft breakdown (fluence) 2) time to soft

breakdown (t_{SB}) 3) time to first breakdown (t_{1BD}) 4) duration of progressive breakdown (DPB) and 5) δ values. Fluence was highly correlated with time to soft breakdown (93%) which is expected since the only variation between the two is devices that have large variations in leakage current. Time to soft breakdown and time to first breakdown had an even higher correlation (98%), consistent with Warnock et al.[3], suggesting a common mechanism for the events. No correlation was found between δ, or DPB, and the breakdown events.

Following soft breakdown testing, thermoreflectance imaging was performed on seven devices, with min/mean/max δ values of 3.6/5.9/7.8, and resulting thermal images are shown in Figure 9. Six of the seven device images contain hotspots located at the mesa edge opposite the gate contact pad; near the gate finger. These localized temperature increases, ranging from 0.5 to 1.5 K, occur at powers as low as 45 µW. After thermoreflectance imaging, I-V data was taken again and δ values were recalculated with min/mean/max values of 2.8/3.5/4.0.

The single pixel sized hot spots visible in the channel region, Figure 9, are believed to be measurement noise for a few reasons. First, the channel hot spots' temperatures do not seem to vary with applied power. If they were self-heating hot spots, they would follow Joule's law and vary linearly with power; such as the temperature at the gate. Second, the spatial distribution of the channel hot spots appears random, or Poisson, which is consistent with shot noise in CCD imaging measurements. Real, or shunt, self-heating is usually focused at one primary shunt location, as we see at the gate edge. Third, the thermoreflectance amplitude of the channel hot spots appear to be the same for all the hot spots in the channel. This again is consistent with shot noise but less common with self-heating due to shunts, where most of the power is typically dissipated at a single shunt location. That said, we cannot rule out the possibility that these tiny hot spots are real self-heating localities.

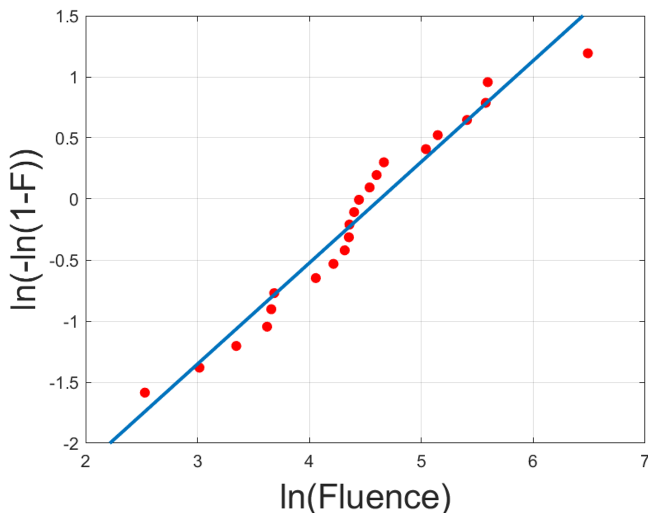

FIG. 8. Weibull distribution of device data. F is the fraction of devices that have achieved soft breakdown.

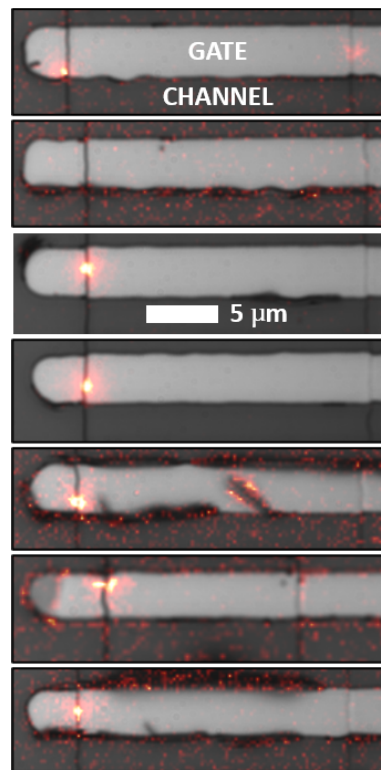

FIG. 9. Images of each device taken during final thermoreflectance measurement. Hot spots due to localized heating at the percolation path are visible on all but one device.

IV. DISCUSSION

Literature values of δ for soft breakdown in SiO_2/Si MOS capacitors are ≈ 3 (4.2 nm oxide)[8,48], with hard breakdown values of ≈ 2 (purely ohmic path)[8]. Immediately following soft breakdown, the δ values were much larger than 3, but approached 3 as device stressing continued; most likely due to enhanced defect generation at the soft breakdown location from localized high current. This initial degree of high non-linearity could be due to a combination of factors. First, is the differences in device architecture between our GaN MOSHEMTs and the SiO_2/Si MOS capacitors. The GaN MOSHEMTs utilized herein are depletion-type (normally ON) unlike the MOS capacitors and have different carrier dynamics and material stackups. Second, the mesa architecture of the GaN MOSHEMTs results in field concentration at the mesa edge where the 2DEG is closest to the gate electrode. This field concentration, which will be discussed shortly, is not present in the planar architecture of the SiO_2/Si MOS capacitors.

The decrease in δ values, and associated non-linearity of the percolation path, during thermoreflectance measurements is a result of the additional stress imposed by the TR measurement process itself. Since the percolation path is present after soft breakdown, and considered highly localized, a worthwhile comparison of fluence from stress testing and TR measurements is not viable. Instead, total charge transferred from

channel to gate is compared. For Device 2 from Figure 6, stress testing applied a total stress of 6.06×10^{-4} C while TR measurement stress totaled 2.26×10^{-2} C. The additional stress induced on the device is also evident by the joule heating detected during the TR measurements themselves. This additional stress increases the defect density in the percolation path, increasing its conductivity.

Thermoreflectance images reveal that all hotspots that occurred during stress testing, occur at the mesa edge near the gate finger. The suspected reason for hot spot formation preferentially occurring at the gate finger, instead of the contact side of the mesa, is due to using e-beam evaporation which is not a conformal deposition method. The line-of-sight nature of e-beam evaporation causes shadowing which in this case may have caused a small gap between the gate electrode and the gate oxide on the contact side; reducing the field strength on that side of the mesa. This characteristic of e-beam evaporation should not appear in future devices that feature the solutions discussed later in this work. SEM imaging of the gate finger near the mesa edge after TR hotspot imaging, showed no degradation when compared with virgin devices. These hotspots are the locations where percolation paths form and coincide with the high lateral electric field through the gate oxide. The lateral electric field strength, $E_{lateral}$, is 6.8 MV/cm and the vertical electric field strength, $E_{vertical}$, is 1.3 MV/cm; from 2DEG to gate electrode at +3.4V. Spillover of electrons moving vertically through the stack may buildup at the bottom of the oxide, increasing $E_{vertical}$.

Leakage from the channel to the gate laterally through the sidewall of the mesa, known as *sidewall leakage*, is an undesirable by-product of the mesa architecture and was originally discovered in InAlAs/InGaAs HFETs[49] and resulted in increased subthreshold and forward gate leakage currents while reducing the device breakdown voltage. Later, Mojaver et al.[50] discovered and characterized the same behavior in AlGaN/GaN HFETs looking specifically at the reverse gate-current. Three solutions have been found to limit sidewall leakage in mesa architectures: 1) selective sidewall recessing[51] 2) RoundHEMT[52] and 3) oxide spacers[53].

For InAlAs/InGaAs heterostructures, selective sidewall recessing is able to eliminate sidewall leakage. The recessing step is performed immediately after mesa isolation, by dipping the wafer in a solution that etches the exposed channel material and leaves the remainder of the structure unaffected. When the gate electrode is deposited via lift-off, an air gap remains between the channel and gate, insulating the channel and preventing sidewall leakage.

Another solution for sidewall leakage, originally proposed by Marso et al., is the RoundHEMT architecture. It doesn't rely on etch selectivity, so is agnostic to the material system. RoundHEMT, as the name implies, completely surrounds the drain contact with the gate contact in a more or less planar architecture. This is a change of the overall architecture and not a solution for the mesa architecture itself.

For AlGaN/GaN material systems selective sidewall recessing is not possible due to the higher chemical stability of GaN compared to InGaAs; so oxide spacers are used. This solution deposits a layer of tetraethyl orthosilicate (TEOS) oxide after mesa isolation. The oxide deposition is conformal and when through-etched, it leaves oxide spacers along the mesa sidewalls. When the gate electrode is deposited, the oxide spacers provide additional separation and insulation between the gate and 2DEG. This solution to sidewall leakage is the most favorable as it is applicable to the AlGaN/GaN material system and doesn't change the entire architecture of the devices, as RoundHEMT would.

V. CONCLUSION

We have examined gate oxide soft breakdown in mesa-style GaN MOSHEMTs via I-V plots and thermoreflectance imaging. We found that when the device gate is subjected to a constant voltage stress, in forward bias, soft breakdown is most likely to occur at the mesa edge where the electric field strength is strongest; concentrated where the distance between the 2DEG and gate electrode is smallest. A solution is proposed, oxide spacers, that is compatible with the material system and standard CMOS fabrication processes.

Future work will consist of 1) integrating the solution, outlined herein, to high field strength localized at the mesa edge 2) determination of the best overall gate insulator by integrating the electrical and thermal characterization so the imaging may be done *in situ* and 3) further characterization of the traps generated in the gate oxide.

The areas where using multiple concurrent device characterization methods has the most potential for impact are device reliability testing and quality control. Electrical characterization measurements are based on averages and spatial resolution can only be achieved if a specialized structure is used[54]. The electrical data, based on averages, then has to be analyzed according to a model to give useful information. Using thermoreflectance concurrently with electrical tests, gives spatial data on device behavior allowing production level devices to be evaluated without having to interrogate the raw data.

ACKNOWLEDGMENTS

We acknowledge support from the Department of Energy (grant DE-EE0004946), the National Science Foundation (grants EEC1454315-CAREER, EEC-1227110, and CBET-1855882), and the Office of Naval Research (grants N000014-15-1-2833 and N00014-19-S-B001). We also thank Muhammad Ashraf Alam for valuable discussions, and our research group for assistance with our experiments.

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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