# GaAs MOSFET With Oxide Gate Dielectric Grown by Atomic Layer Deposition

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***Abstract*—For the first time, a III-V compound semiconductor MOSFET with the gate dielectric grown by atomic layer deposition (ALD) is demonstrated. The novel application of the ALD process on III-V compound semiconductors affords tremendous functionality and opportunity by enabling the formation of high-quality gate oxides and passivation layers on III-V compound semiconductor devices. A 0.65-$\mu$m gate-length depletion-mode n-channel GaAs MOSFET with an $Al_2O_3$ gate oxide thickness of 160 Å shows a gate leakage current density less than $10^{-4}$ A/cm$^2$ and a maximum transconductance of 130 mS/mm, with negligible drain current drift and hysteresis. A short-circuit current-gain cut-off frequency $f_T$ of 14.0 GHz and a maximum oscillation frequency $f_{max}$ of 25.2 GHz have been achieved from a 0.65-$\mu$m gate-length device.**

***Index Terms*—Atomic layer deposition, depletion mode, GaAs MOSFET.**

## I. Introduction

CMOS integrated-circuit technology dominates the Si-based microelectronics industry. The key for the aggressive yet successful scaling of Si CMOS technology is the outstanding material properties of $SiO_2$ and the $SiO_2$/Si interface. The benefits of a GaAs-based MOSFET are well known, based on the success of Si technology. This motivation has attracted great interest for decades [1]–[9]. Gallium arsenide (GaAs)-based devices potentially have great advantages over silicon (Si)-based devices for both high-speed and high-power applications, in part from an electron mobility in GaAs that is $\sim 5\times$ greater than that in Si, and from the availability of semi-insulating GaAs substrates. In contrast to GaAs MESFETs and HEMTs, both of which exhibit a severe limitation on forward gate bias of a few tenths of a volt (arising from the nature of Schottky barrier heights), GaAs MOSFETs feature a much larger logic swing, which provides much greater flexibility in digital IC design.

The main obstacle to GaAs-based MOSFET devices is the lack of high-quality, thermodynamically stable insulators on GaAs that can match the device criteria as $SiO_2$ on Si, e.g., a mid-bandgap interface-trap density $(D_{it})$ of $\sim 10^{10}$/cm$^2$-eV. Many approaches [10]–[13] have been applied to grow a gate oxide on GaAs, such as thermal, anodic, and plasma methods or direct deposition of thermodynamically stable oxide films on GaAs. These approaches have had limited success, however, due to a high and unacceptable $D_{it}$ value. Recently, *in situ* deposition of $Ga_2O_3$ and $Ga_2O_3(Gd_2O_3)$ dielectric films on the GaAs surface in an ultrahigh-vacuum multichamber molecular beam epitaxy (MBE) system has been shown to provide a high-quality interface with a low $D_{it}$ [14]–[17]. Promising results have been demonstrated in both inversion-channel and depletion-mode GaAs MOSFETs using this technique [18]–[20].

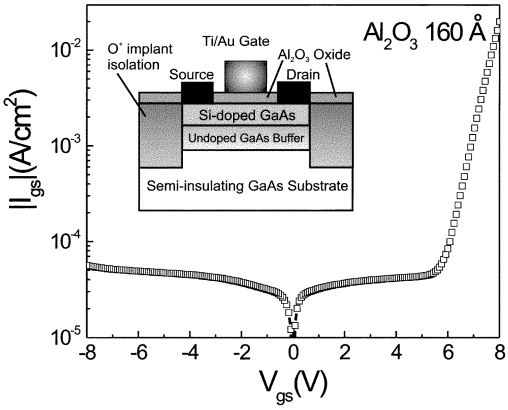


Fig. 1. Two-terminal gate $I$–$V$ characteristics of an $Al_2O_3$/GaAs MOSFET. Source and drain are grounded together. Inset: Schematic view of a depletion-mode n-channel GaAs MOSFET with ALD-grown $Al_2O_3$ as gate dielectric.

In this letter, we report for the first time a MOSFET on a III-V substrate with an $Al_2O_3$ gate dielectric deposited by atomic layer deposition (ALD). $Al_2O_3$ is a highly desirable gate dielectric from both a physical and electrical characteristics standpoint: $Al_2O_3$ has a high bandgap ($\sim$9 eV), a high breakdown field (5–10 MV/cm), and high thermal stability (up to at least 1000 °C) and remains amorphous under typical processing conditions. Furthermore, $Al_2O_3$ is easily wet-etched yet is robust against interfacial reactions and moisture absorption (i.e., nonhygroscopic). The $Al_2O_3$ gate oxide is grown by ALD, which is a variant of CVD, and has recently shown promise for use in high-k gate dielectrics for Si CMOS [21]. ALD is an *ex situ*, robust manufacturing process that is already commonly used throughout the Si industry. This process does not require ultrahigh-vacuum conditions for wafer transfer between semiconductor epi-layer growth and oxide layer deposition and may find wide applications in microelectronics manufacturing.

## II. Device Structure and Process

The device structure of the fabricated depletion-mode n-channel $Al_2O_3$/GaAs MOSFET is shown in the inset of Fig. 1. A 1500-Å undoped GaAs buffer layer and a 700-Å

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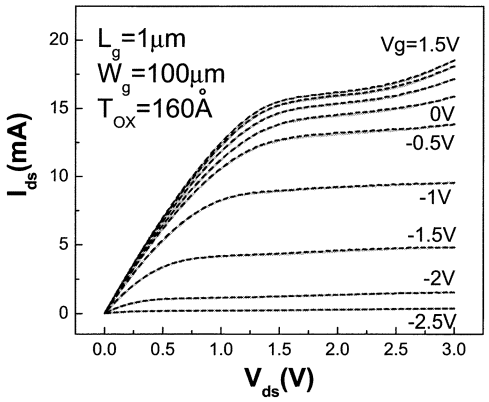


Fig. 2. Drain current versus drain bias in both forward (dashed black line) and reverse (solid gray line) sweep directions as a function of gate bias. The $I$–$V$ characteristics show negligible hysteresis in drain current.

Si-doped GaAs layer ($4 \times 10^{17}/\text{cm}^3$) were sequentially grown by MBE on a (100)-oriented semi-insulating 2-in GaAs substrate. After the semiconductor epilayer growth, the wafer was transferred *ex situ* to an ASM Pulsar2000™ ALD module. A 160-Å-thick $Al_2O_3$ oxide layer was deposited at a substrate temperature of 300 °C, using alternately pulsed chemical precursors of $Al(CH_3)_3$ (the Al precursor) and $H_2O$ (the oxygen precursor) in a carrier $N_2$ gas flow. Each precursor undergoes a self-limiting reaction at the surface, and the $Al_2O_3$ film is thereby grown with excellent thickness and uniformity precision. A post-deposition anneal was done at 600 °C for 60 s in an oxygen ambient. Device isolation was achieved by oxygen implantation. Activation annealing was performed at 450 °C in a helium gas ambient. Using a wet etch in diluted HF, the oxide on the source and drain regions was removed while the gate area was protected by photoresist. Ohmic contacts were formed by e-beam deposition of Au/Ge/Au/Ni/Au and a lift-off process, followed by a 425 °C anneal in a nitrogen ambient. Finally, conventional Ti/Au metals were e-beam evaporated, followed by liftoff to form the gate electrodes. The source-to-gate and the drain-to-gate spacings are ∼0.75 $\mu$m. The sheet resistance and contact resistance is 1.3 kΩsq. and 1.5 Ω · mm. The gate lengths of the measured devices are 0.65, 0.85, 1, 2, and 4 $\mu$m. The process requires four levels of lithography (alignment, isolation, ohmic, and gate), all done using a contact printer.

## III. Electrical Results and Discussions

Fig. 1 demonstrates the low gate leakage of these devices in the gate $I$–$V$ characteristics of a MOSFET with an $Al_2O_3$ gate oxide thickness of 160 Å. The gate length and width of the device are 0.65 $\mu$m and 100 $\mu$m, respectively. For gate operation between a bias ($V_g$) of +4 V to −4 V, the gate leakage current is less than 100 pA, corresponding to $<10^{-4}$ A/cm$^2$. Based on the data in Fig. 1, these MOSFET devices clearly exhibit extremely low gate leakage currents over a 14-V gate bias range, which is more than three orders of magnitude lower than for MESFETs under similar bias. The forward breakdown voltage is ∼8 V for a 160-Å-thick $Al_2O_3$ layer, which corresponds to a breakdown electric field larger than 5 MV/cm. This verifies the high quality of the ALD-grown oxide even after the full transistor process.

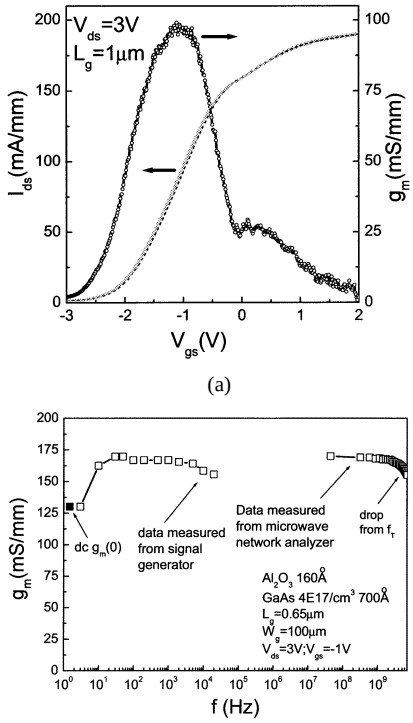


Fig. 3. (a) Drain current versus gate bias in both forward (dashed black line) and reverse (solid gray line) sweep directions. Dotted line is transconductance versus gate bias at $V_{ds} = 3$ V. (b) Peak transconductance $g_m$ versus frequency from dc to several gigahertz. The $g_m$ is essentially constant for frequencies above 20 Hz, indicating that efficient charge modulation of the channel can be achieved over the entire useful frequency range of the device.

We ascribe the asymmetric gate $I$–$V$ characteristics to different carrier transport mechanisms and barrier heights in the different bias polarities. The current is larger when the semiconductor is biased to inject electrons compared with when the metal is biased to inject electrons.

The DC $I$–$V$ characteristics of a MOSFET show a clean pinchoff at a gate voltage of −2.5 V (see Fig. 2) with a gate length of 1 $\mu$m and gate width of 100 $\mu$m. Device operation is achieved for positive $V_{gs}$ bias voltages, and no substantial $I$–$V$ hysteresis is observed in the drain current drift in both the forward and reverse sweep directions. This indicates that no significant mobile bulk oxide charge is present and that density of slow interface traps is low. The small $g_m$ and $I_{ds}$ values for $V_{gs} > 0$ V are mainly limited by the surface mobility of the GaAs layer and/or higher $D_{\text{it}}$ near the conduction-band edge. In order to separate these two factors, more detailed capacitance and Hall measurements as a function of gate bias are underway. Ongoing experiments with an inserted $In_{0.2}Ga_{0.8}As$ channel show significant improvement in both $g_m$ and $I_{ds}$ performance for $V_{gs} > 0$ V, which can be attributed to the higher surface mobility of the $In_{0.2}Ga_{0.8}As$ layer.

Fig. 3(a) illustrates the drain current as a function of gate bias in both the forward and reverse sweep directions in the saturation region. The device shows negligible hysteresis. The slope of the drain current shows that the peak extrinsic transconductance $(g_m)$ of the 1-$\mu$m gate length device is 100 mS/mm. The peak $g_m$ can be improved from ∼90 mS/mm at a 4-$\mu$m gate length to ∼130 mS/mm at 0.65-$\mu$m gate length. Fig. 3(b) shows the

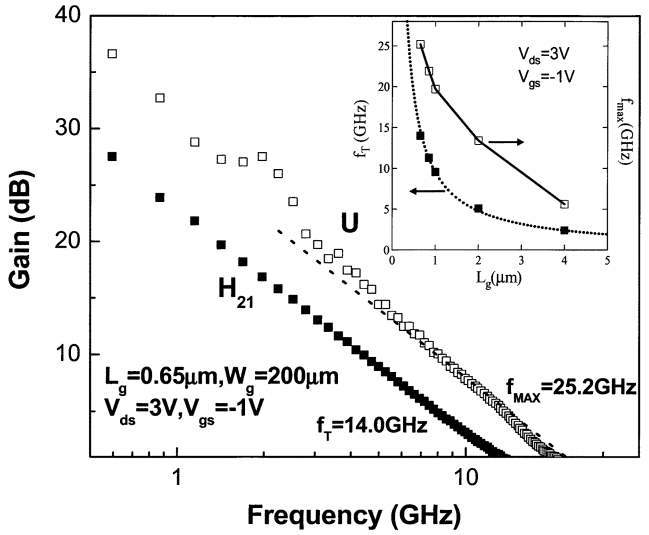


Fig. 4. RF characteristics of $Al_2O_3$/GaAs MOSFETs with gate length and width of 0.65 and 100 $\mu$m, respectively. RF tester includes two identical devices with total gate length of 200 $\mu$m. Inset: $f_T$ and $f_{\max}$ for different gate lengths. The dashed line illustrates $f_T = v_{\rm sat}/2\pi L_g$.

peak $g_m$ as a function of frequency, measured from dc to several gigahertz, under typical operating conditions ($V_{ds} = 3$ V, $V_{gs} = -1$ V). It can be seen that the $g_m$ remains essentially constant for frequencies above 20 Hz, indicating that efficient charge modulation in the channel can be achieved over the entire useful frequency range of the device. Furthermore, note that there is about a 20% decrease in $g_m$ from 20 Hz down to dc. A model calculation of this change in $g_m$ gives an upper limit for $D_{\rm it}$ of $5 \times 10^{11}$ to $10^{12}/{\rm cm}^2$-eV.

From S-parameter measurements, the short-circuit current-gain cut-off frequency $(f_T)$ and the maximum oscillation frequency $(f_{\max})$ are determined by biasing the devices at $V_{ds} = 3$ V and $V_{gs} = -1$ V. Under these conditions, the 0.65-$\mu$m gate length device shows $f_T = 14$ GHz and $f_{\max} = 25$ GHz. These values are obtained by extrapolating the short-circuit current gain $(H_{21})$ and the unilateral power gain (U) curves, respectively, using $-20$ dB/decade slopes, as shown in Fig. 4. The inset of Fig. 4 illustrates the $f_T$ and $f_{\max}$ as a function of gate length. As the trend shows, $f_T$ and $f_{\max}$ can be significantly improved by reducing the gate length. The observed $f_T$ versus gate length is quite close to the theoretical relation of $f_T = v_{\rm sat}/2\pi L_g$, where $v_{\rm sat}$ is $\sim 6 \times 10^6$ cm/s.

The long-term drain-current drift behavior of the $Al_2O_3$/GaAs MOSFET is also studied when the devices are biased at a stress condition of $V_{ds} = 4$ V and $V_{gs} = 2$ V. The long-term drain-current drift is less than 3% for a stress period of $\sim$12 h. The result is comparable with the best data reported previously [19], indicating that the ALD-grown $Al_2O_3$ film and $Al_2O_3$/GaAs interface are of very high quality.

## IV. Conclusions

We have demonstrated the first ALD-grown insulated gate MOSFET on III-V substrates, using $Al_2O_3$ gate dielectric for n-channel depletion-mode GaAs devices. The 0.65-$\mu$m gate-length device exhibits an extrinsic transconductance of 130 mS/mm, an $f_T$ of 14 GHz, and an $f_{\max}$ of 25 GHz, with negligible $I$–$V$ hysteresis and a gate leakage current density less than $10^{-4}$ A/cm$^2$. The stability under stress indicates that the ALD-grown $Al_2O_3$ film and the $Al_2O_3$/GaAs interface are of high quality. These results provide new opportunities to explore many other alternative dielectrics for use as gate oxides and as effective passivation layers on III-V compound semiconductor devices.

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