GaSb Inversion-Mode PMOSFETs With Atomic-Layer-Deposited Al_2O_3 as Gate Dielectric

Min Xu, Runsheng Wang, *Student Member, IEEE*, and Peide D. Ye, *Senior Member, IEEE*

***Abstract*—GaSb inversion-mode PMOSFETs with atomic-layer-deposited (ALD) Al_2O_3 as gate dielectric are demonstrated. A 0.75-μm-gate-length device has a maximum drain current of 70 mA/mm, a transconductance of 26 mS/mm, and a hole inversion mobility of 200 $cm^2/V \cdot s$. The OFF-state performance is improved by reducing the ALD growth temperature from 300 °C to 200 °C. The measured interface trap distribution shows a low interface trap density of $2 \times 10^{12}/cm^2 \cdot eV$ near the valence band edge. However, it increases to $1 - 4 \times 10^{13}/cm^2 \cdot eV$ near the conduction band edge, leading to a drain current on–off ratio of 265 and a subthreshold swing of ~600 mV/decade. GaSb, similar to Ge, is a promising channel material for PMOSFETs due to its high bulk hole mobility, high density of states at the valence band edge, and, most importantly, its unique interface trap distribution and trap neutral level alignment.**

***Index Terms*—Atomic layer deposition, GaSb, high-*k*, MOSFET.**

I. Introduction

COMPLEMENTARY metal–oxide–semiconductor (CMOS) devices based on Si have been scaled close to their physical limit. To further increase the device performance, III–V semiconductor materials have attracted interest because of their higher electron mobility and saturation velocity. Although significant progress has been made on high-k/III–V NMOSFETs [1]–[3] and Schottky-gate p-channel quantum well transistors [4], [5], there is less work on III–V PMOSFETs [6]. In this letter, we address the fundamental advantages of using GaSb as the p-channel material in a potential full III–V CMOS technology [7], [8]. The validity of this approach is supported by the experimental results on atomic-layer-deposited (ALD) Al_2O_3/GaSb PMOSFETs.

GaSb has a bandgap of 0.73 eV and is near lattice matched to InAs. The hole mobility of GaSb is $\sim 1000\ cm^2/V \cdot s$, which is much higher than most other III–V materials [9]. However, the drain current (I_{DS}) in an inversion-mode MOSFET is not only determined by the mobility and saturation velocity but also by the inversion charge density. The effective density of states in the valence band (N_V) for GaSb is as high as $1.8 \times 10^{19}/cm^3$ [10], which is also favorable for realizing high-performance GaSb PMOSFETs. The trap neutral level (E_0) position and interface trap distribution play a significant role in the device performance if the oxide/semiconductor interface is nonideal. According to the defect-induced gap-state model developed by Hasegawa and Ohno [11], the empirical model by the authors [12], and the defective interface model by Robertson [13], the E_0 for GaSb should be located around 0.1 eV above the valence band edge (E_V). This particular property makes it easy to realize strong hole inversion.

Manuscript received March 6, 2011; revised April 4, 2011; accepted April 8, 2011. Date of publication May 16, 2011; date of current version June 29, 2011. This work was supported by SRC Cross-Disciplinary Semiconductor Research Program. The work of M. Xu was supported in part by The Network for Computational Nanotechnology. The review of this letter was arranged by Editor M. Passlack.

The authors are with the School of Electrical and Computer Engineering and the Birck Nanotechnology Center, Purdue University, West Lafayette, IN 47907 USA (e-mail: yep@purdue.edu).

Color versions of one or more of the figures in this letter are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/LED.2011.2143689

II. Device Fabrication

Two-inch n-type GaSb (100) substrates with a doping concentration of $5.5 \times 10^{17}\ cm^{-3}$ were used for MOSFET fabrication. After degreasing by acetone, methanol, and isopropanol, 30-nm Al_2O_3 was deposited at 300 °C in an ASM F-120 ALD chamber as an encapsulation layer using trimethyl aluminum and water as precursors. Source and drain regions were selectively implanted with a Si dose of $2 \times 10^{14}\ cm^{-2}$ at 50 keV through the 30-nm Al_2O_3 encapsulation layer [14]. Dopant activation was achieved by a 30-s rapid thermal anneal (RTA) at 650 °C (Process-I samples) or at 600 °C (Process-II and Process-III samples). The encapsulation layer was then removed by buffered oxide etch. The surface was then treated with $HCl:H_2O = 1:1$ for 30 s to etch away the native oxide and subsequently treated with NH_4OH for 60 s to remove elemental Sb. Following those treatments, 8-nm Al_2O_3 gate dielectrics were regrown by ALD at 300 °C (Process-I and Process-II samples) or 200 °C (Process-III samples). After 600 °C postdeposition anneal (PDA) for 30 s in N_2 ambient, the source and drain ohmic contacts were made by electron beam evaporation of a combination of Pt/Ti/Pt/Au. The gate electrode was defined by electron beam evaporation of Ni/Au. Also, an n-type GaSb substrate with a doping concentration of $5.5 \times 10^{17}\ cm^{-3}$ and a p-type GaSb substrate with a doping concentration of $1.1 \times 10^{18}\ cm^{-3}$ were used for MOSCAPs with 8-nm Al_2O_3 films grown at 300 °C and a 600 °C PDA.

III. Results and Discussion

Fig. 1(a) shows the schematic cross section of a GaSb inversion-mode PMOSFET with the gate aligned in the $\langle 110 \rangle$ direction. Transfer-length-method structures are used to study the implantation/activation. Due to the relatively high substrate doping concentration $(5.5 \times 10^{17}\ cm^{-3})$, a high Si implantation dose $(2 \times 10^{14}\ cm^{-2})$ was used, requiring a high activation temperature to activate the dopants and recover lattice damage.

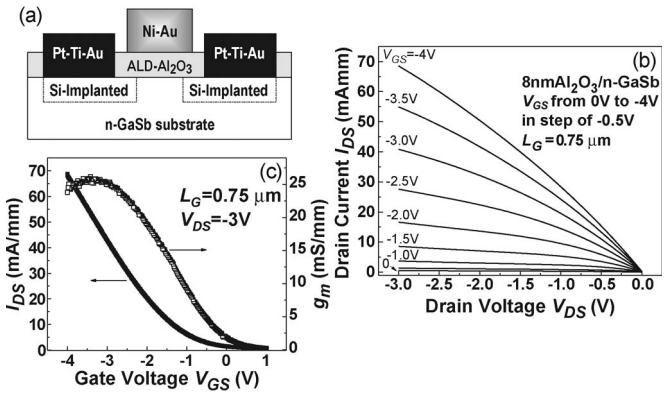

Fig. 1. (a) Schematic cross section of an inversion-mode GaSb PMOSFET with ALD Al_2O_3 as gate dielectric. (b) DC output characteristic of a 0.75-μm-gate-length device fabricated by Process I at $V_{\rm DS} = -3$ V and $V_{\rm GS} = -4$ V, showing the drain current potential at the current interface quality and dielectric strength. (c) DC transfer characteristics of the same device at $V_{\rm DS} = -3$ V.

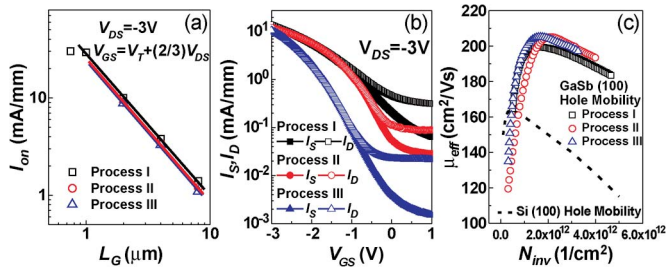

Fig. 2. (a) Comparison of scaling behavior of drain currents versus gate length L_G on three different processed samples at $V_{\rm DS} = -3$ V and $V_{\rm GS} = V_T + (2/3) \cdot V_{\rm DS}$. (b) (Empty signs) Drain currents and (solid signs) source currents versus gate bias $V_{\rm GS}$ on three different processed samples at $V_{\rm DS} = -3$ V. (c) Effective mobility ($\mu_{\rm eff}$) versus inversion hole charge density ($N_{\rm inv}$). $\mu_{\rm eff}$ is extracted from split C–V method with all three processes. The Si(100) universal hole mobility is also included for comparison.

The sheet resistance is 390 Ω/sq. for 650 °C activation and 480 Ω/sq. for 600 °C activation, respectively. The source/drain contact resistance (R_S or R_D) is 6.85 $\Omega \cdot$ mm for 650 °C and 15.1 $\Omega \cdot$ mm for 600 °C activation, respectively, determined from PMOSFETs with different gate lengths. Fig. 1(b) shows the dc output characteristic of a 0.75-μm-gate-length GaSb PMOSFET with Process I. A maximum $I_{\rm DS}$ of 70 mA/mm is obtained at a gate bias of -4 V and a drain bias of -3 V. From the device transfer characteristic, a maximum transconductance g_m of $\sim$26 mS/mm is obtained. Note that the $I_{\rm DS}$ and g_m achieved here are much larger than those from the previous works on inversion-mode GaAs PMOSFETs [15], [16]. The $I_{\rm DS}$ is larger than the value reported on GaAs p-channel MOS-HFET ($I_{\rm DS} \sim 50$ mA/mm and $g_m \sim 50$ mS/mm with $L_G = 0.6$ μm) by Passlack *et al.* [6], while the g_m is lower mainly due to the large source/drain contact resistance and the interface traps described as follows. The gate leakage current is below 1×10^{-3} A/cm^2 at -4.0 V gate bias, which is more than six orders of magnitude smaller than the drain on-current.

Fig. 2(a) summarizes all measured drain currents $I_{\rm DS}$ for three different processed samples versus L_G at $V_{\rm DS} = -3.0$ V and $V_{\rm GS} = V_T + (2/3) \cdot V_{\rm DS}$. The drain on-current ($I_{\rm ON}$) is linearly inversely proportional to L_G, as expected, and starts to saturate at submicrometer gate length. The $I_{\rm ON}$ for Process I is slightly larger than those for Process II and Process III at the same L_G due to a higher RTA temperature, thus better ohmic contacts. By the linear extrapolation at $V_{\rm DS} = -0.05$ V, the V_T values of 2-μm-gate-length devices are determined to be -0.5 V for Process I, -0.75 V for Process II, and -1.7 V for Process III. The threshold voltage (V_T) for Process III is shifted more negative due to low-temperature ALD dielectric formation, which leads to the reduction of the negative fixed charges in the dielectric [17]. Fig. 2(b) compares the transfer characteristics of 2-μm-gate-length devices for three different processes at $V_{\rm DS} = -3$ V. The leakage floor of I_D at $V_{\rm GS} > 0$ is mainly determined by the reverse-biased pn-junction leakage current $I_{\rm SUB}$ [1]. The leakage floor of I_S at $V_{\rm GS} > 0$ is mainly due to the high $D_{\rm it}$ in the bandgap (Process I or II) which impedes further modulation of the channel charges at OFF state. The low values of I_D and I_S at $V_{\rm GS} > 0$ for Process III indicate the improvement in both junction leakage and the interface quality. From Fig. 2(b), the values of $I_{\rm on}/I_{\rm off}$ are determined to be 24 and 100 for Process I, 107 and 289 for Process II, and 265 and 454 for Process III from I_D and I_S, respectively. $I_{\rm on}/I_{\rm off}$ is chosen as $I_{\rm on}$ ($V_{\rm DS} = -3$ V, $V_{\rm GS} = V_T + 2/3V_{\rm DS}$)/$I_{\rm off}$($V_{\rm DS} = -3$ V, $V_{\rm GS} = V_T - 1/3V_{\rm DS}$) with V_T determined by linear extrapolation at $V_{\rm DS} = -0.05$ V. The subthreshold swing of the device in Fig. 2(b) for Process III at $V_{\rm DS} = -0.05$ V is $\sim$600 mV/decade due to the high $D_{\rm it}$ in the bandgap. Combined with the split C–V measurement, the extracted peak hole mobility is $\sim$ 200 cm^2/V $\cdot$ s with all three processes, as shown in Fig. 2(c).

Fig. 3(a) shows the temperature-dependent C–V measurements in accumulation [18] on an Al_2O_3/p-GaSb MOSCAP. The frequencies range from 5 to 464 kHz with temperature from 300 K down to 35 K. The very small frequency dispersion at all temperatures in the accumulation capacitance indicates true accumulation and good interface properties near the valence band edge. The room-temperature minority carrier (electron) or trap response at positive bias is suppressed at 77 K or 35 K. Note that, even at temperature as low as 35 K, the accumulation capacitance does not decrease significantly, in great contrast to GaAs [18]. This results from the high N_V for GaSb. This allows the channel to get sufficiently high hole density with less E_F movement.

Fig. 3(b) shows the $D_{\rm it}$ distribution across the whole GaSb bandgap. The $D_{\rm it}$ value near E_V is $\sim 2 \times 10^{12}$/cm$^2 \cdot$ eV determined by the measured low-f and high-f C–V method shown in Fig. 3(a). The temperature-dependent conductance method is also employed to quantitatively map the $D_{\rm it}$ distribution inside the bandgap and near E_C for majority carriers in n-type GaSb MOSCAPs. It is found that the $D_{\rm it}$ for GaSb, similar to Ge without good passivation, increases rapidly to $1 - 4 \times 10^{13}$/cm$^2 \cdot$ eV in the bandgap and $1 - 2 \times 10^{13}$/cm$^2 \cdot$ eV near E_C. Better $D_{\rm it}$ inside the bandgap for Process III is also consistent with the better OFF-state performance of PMOSFETs with Process III, as shown in Fig. 2(b). The determined $D_{\rm it}$ distribution at the Al_2O_3/GaSb interface clearly explains why strong inversion and reasonable drain current can be obtained on GaSb PMOSFETs. GaSb has a similar band alignment to the trap neutral level E_0 as Ge [12], [13], [19]. The previously demonstrated GaSb PMOSFET and $D_{\rm it}$ distribution further

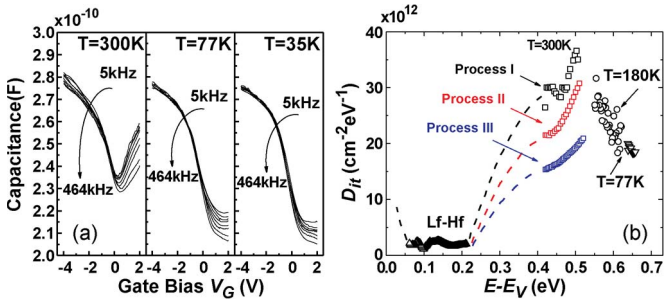

Fig. 3. (a) C–V plots of Au/ Ni/8-nm-Al_2O_3/p-GaSb at 300 K, 77 K, and 35 K. The excellent frequency-dispersion behavior at accumulation capacitance at all temperatures indicates true hole accumulation and a good interface near the valence band. The capacitor area is 3.14×10^4 μm^2 with a dielectric constant of ~8 for Al_2O_3. (b) Interface trap distribution near the conduction band is obtained from temperature-dependent conductance method on n-MOSCAPs at 300 K, 180 K, and 77 K, and that near the valence band is obtained from low-f–high-f C–V measurement on p-MOSCAPs at 35 K. The D_{it} distribution is similar to that on Ge without good surface passivation. The hole capture cross section in GaSb from 10^{-18} to $10^{-14}/cm^2$, depending on the energy level [20], is chosen to determine the D_{it} distribution. The dashed lines are guides to the eye. The square signs are obtained from conductance method performed at 300 K with the black signs for Process I, the red signs for Process II, and the blue signs for Process III. The black circle signs and down triangle signs are obtained from Process-I samples performed at 180 K and 77 K, respectively. Process I with a higher activation temperature of 650 °C results in a larger D_{it} since GaSb has a melting point of 712 °C and is easier to lose Sb at a higher processing temperature [10].

confirms the validity of the models proposed in [11]–[13]. However, the OFF-state performance suffers from the large D_{it} in the bandgap. To turn the device off, E_F has to move away from the valence band, and the large amount of acceptor-type interface traps starts to become negatively charged and prevents E_F to move freely further to turn off the channel. Improved dielectric process with better passivation and optimized device fabrication are needed to reduce the D_{it} and further improve the ON- and OFF-state performances of GaSb PMOSFETs.

IV. Conclusion

In summary, we have demonstrated GaSb inversion-mode PMOSFETs with ALD Al_2O_3 as gate dielectric. For a device with a gate length of 0.75 μm, a maximum drive current of 70 mA/mm, a transconductance of 26 mS/mm, and a hole inversion mobility of ~ 200 $cm^2/V \cdot s$ are achieved. However, the OFF state is limited by a high D_{it} in the bandgap with a drain current on–off ratio of 265 and a subthreshold swing of ~600 mV/decade. The D_{it} distribution at Al_2O_3/GaSb is quantitatively measured, which accurately explains the ON- and OFF-state performances of GaSb MOSFETs.

References

[1] Y. Xuan, Y. Q. Wu, and P. D. Ye, "High-performance inversion-type enhancement-mode InGaAs MOSFET with maximum drain current exceeding 1 A/mm," *IEEE Electron Devices Lett.*, vol. 29, no. 4, pp. 294–296, Apr. 2008.

[2] M. Radosavljevic, B. Chu-Kung, S. Corcoran, G. Dewey, M. K. Hudait, J. M. Fastenau, J. Kavalieros, W. K. Liu, D. Lubyshev, M. Metz, K. Millard, N. Mukherjee, W. Rachmady, U. Shah, and R. Chau, "Advanced high- κ gate dielectric for high-performance short-channel $In_{0.7}Ga_{0.3}As$ quantum well field effect transistors on silicon substrate for low power logic applications," in *IEDM Tech. Dig.*, Dec. 2009, pp. 319–322.

[3] R. J. W. Hill, D. A. J. Moran, X. Li, H. P. Zhou, D. Macintyre, S. Thoms, A. Asenov, P. Zurcher, K. Rajagopalan, J. Abrokwah, R. Droopad, M. Passlack, and I. G. Thayne, "Enhancement-mode GaAs MOSFETs with an $In_{0.3}Ga_{0.7}As$ channel, a mobility of over 5000 $cm^2/V \cdot s$, and transconductance of over 475 $\mu S/\mu m$," *IEEE Electron Device Lett.*, vol. 28, no. 12, pp. 1080–1082, Dec. 2007.

[4] M. Radosavljevic, T. Ashley, A. Andreev, S. D. Coomber, G. Dewey, M. T. Emeny, M. Fearn, D. G. Hayes, K. P. Hilton, M. K. Hudait, R. Jefferies, T. Martin, R. Pillarisetty, W. Rachmady, T. Rakshit, S. J. Smith, M. J. Uren, D. J. Wallis, P. J. Wilding, and R. Chau, "High-performance 40 nm gate length InSb P-channel compressively strained quantum well field effect transistors for low-power ($Vcc = 0.5$ V) logic applications," in *IEDM Tech. Dig.*, Dec. 2008, pp. 727–730.

[5] A. Nainani, S. Raghuanathan, D. Witte, M. Kobayashi, T. Irisawa, T. Krishnamohan, and K. Saraswat, "Engineering of strained III–V heterostructures for high hole mobility," in *IEDM Tech. Dig.*, Dec. 2009, pp. 857–860.

[6] M. Passlack, J. K. Abrokwah, R. Droopad, Z. Y. Yu, C. Overgaard, S. I. Yi, M. Hale, J. Sexton, and A. C. Kummel, "Self-aligned GaAs p-channel enhancement mode MOS heterostructure field-effect transistor," *IEEE Electron Device Lett.*, vol. 23, no. 9, pp. 508–510, Sep. 2002.

[7] A. Nainani, T. Irisawa, Z. Yuan, Y. Sun, T. Krishnamohan, M. Reason, B. R. Bennett, J. B. Boos, M. G. Ancona, Y. Nishi, and K. C. Saraswat, "Development of high- k dielectric for antimonides and a sub 350 °C III–V pMOSFET outperformance germanium," in *IEDM Tech. Dig.*, Dec. 2010, pp. 138–141.

[8] A. Ali, H. Madan, R. Misra, E. Hwang, A. Agrawal, I. Ramirez, P. Schiffer, T. N. Jackson, J. B. Boos, B. R. Bennett, I. Geppert, M. Eizenberg, and S. Datta, "Advanced composite high-k gate stack for mixed anion arsenide-antimonide quantum well transistors," in *IEDM Tech. Dig.*, Dec. 2010, pp. 134–137.

[9] S. K. Haywood, A. B. Henriques, N. J. Mason, R. J. Nicholas, and P. J. Walker, "Growth of GaSb by MOVPE," *Semicon. Sci. Technol.*, vol. 3, no. 4, pp. 315–320, Apr. 1988.

[10] [Online]. Available: http://www.ioffe.ru/SVA/NSM/Semicond/GaSb/bandstr.html

[11] H. Hasegawa and H. Ohno, "Unified disorder induced gap state model for insulator–semiconductor and metal–semiconductor interfaces," *J. Vac. Sci. Technol. B.*, vol. 4, no. 4, pp. 1130–1138, Jul. 1986.

[12] P. D. Ye, Y. Xuan, Y. Q. Wu, and M. Xu, "Atomic-layer deposited high-k/III–V metal–oxide–semiconductor devices and correlated empirical model," in *Fundamentals of III–V Semiconductor MOSFETs*, S. Oktyabrisky and P. D. Ye, Eds. New York: Springer-Verlag, Feb. 2010.

[13] J. Robertson, "Model of interface states at III–V oxide interfaces," *Appl. Phys. Lett.*, vol. 94, no. 15, pp. 152 104-1–152 104-3, Apr. 2009.

[14] A. G. Milnes, X. Li, A. Y. Polyakov, N. B. Smirnov, A. V. Govorkov, O. M. Borodina, I. V. Tunitskaya, E. A. Kozhukhova, and A. G. Mil'vidskaya, "Ion implantation effects in GaSb," *Mater. Sci. Eng, B*, vol. 27, no. 2/3, pp. 129–136, Nov. 1994.

[15] I. Ok, H. Kim, M. Zhang, T. Lee, F. Zhu, L. Yu, S. Koveshnikov, W. Tsai, V. Tokranov, M. Yakimov, S. Oktyabrsky, and J. C. Lee, "Self-aligned n- and p-channel GaAs MOSFETs on undoped and P-type substrates using HfO_2 and silicon interface passivation layer," in *IEDM Tech. Dig.*, Dec. 2006, pp. 1–4.

[16] M. Xu, Y. Q. Wu, O. Koybasi, T. Shen, and P. D. Ye, "Metal–oxide–semiconductor field-effect transistors on GaAs (111)A surface with atomic-layer-deposited Al_2O_3 as gate dielectrics," *Appl. Phys. Lett.*, vol. 94, no. 21, pp. 212 104-1–212 104-3, May 2009.

[17] J. Buckley, B. De Salvo, D. Deleruyelle, M. Gely, G. Nicotra, S. Lombardo, J. F. Damlencourt, Ph. Hollonger, F. Martin, and S. Deleonibus, "Reduction of fixed charges in atomic layer deposited Al_2O_3 dielectrics," *Microelectron. Eng.*, vol. 80, pp. 210–213, Jun. 2005.

[18] M. Xu, K. Xu, R. Contreras, M. Milojevic, T. Shen, O. Koybasi, Y. Q. Wu, R. M. Wallace, and P. D. Ye, "New insight into Fermi-level unpinning on GaAs: Impact of different surface orientations," in *IEDM Tech. Dig.*, Dec. 2009, pp. 865–868.

[19] A. Dimoulas, P. Tsipas, and A. Sotiropoulos, "Fermi-level pinning and charge neutrality level in germanium," *Appl. Phys. Lett.*, vol. 89, no. 25, pp. 252 110-1–252 110-3, Dec. 2006.

[20] K. Nakashima, "ICTS measurements of interface properties in GaSb MOS structure," *Jpn. J. Appl. Phys.*, vol. 26, no. 2, pp. 308–309, Feb. 1987.