Submicrometer Inversion-Type Enhancement-Mode InGaAs MOSFET With Atomic-Layer-Deposited Al_2O_3 as Gate Dielectric

Y. Xuan, *Member, IEEE*, Y. Q. Wu, *Student Member, IEEE*, H. C. Lin, T. Shen, and Peide D. Ye, *Senior Member, IEEE*

***Abstract*—High-performance inversion-type enhancement-mode n-channel $In_{0.53}Ga_{0.47}As$ MOSFETs with atomic-layer-deposited (ALD) Al_2O_3 as gate dielectric are demonstrated. The ALD process on III–V compound semiconductors enables the formation of high-quality gate oxides and unpinning of Fermi level on compound semiconductors in general. A 0.5-μm gate-length MOSFET with an Al_2O_3 gate oxide thickness of 8 nm shows a gate leakage current less than 10^{-4} A/cm^2 at 3-V gate bias, a threshold voltage of 0.25 V, a maximum drain current of 367 mA/mm, and a transconductance of 130 mS/mm at drain voltage of 2 V. The midgap interface trap density of regrown Al_2O_3 on $In_{0.53}Ga_{0.47}As$ is $\sim$1.4 $\times$ 10^{12}/cm$^2 \cdot$ eV which is determined by low- and high-frequency capacitance–voltage method. The peak effective mobility is $\sim$1100 cm^2/V $\cdot$ s from dc measurement, $\sim$2200 cm^2/V $\cdot$ s after interface trap correction, and with about a factor of two to three higher than Si universal mobility in the range of 0.5–1.0-MV/cm effective electric field.**

***Index Terms*—Atomic layer deposition (ALD), compound semiconductor, enhancement mode (E-mode), inversion, MOSFETs.**

I. Introduction

IN THE PAST four decades, great efforts have been made to produce "perfect" insulators for III–V MOSFETs. The literature testifies to the extent of this enormous effort [1]–[6], including some promising results from *in situ* molecular-beam-epitaxy (MBE) grown $Ga_2O_3(Gd_2O_3)$ [7]–[11]. However, this letter is mainly focused on *ex situ* atomic-layer-deposited (ALD) high-κ dielectrics on III–V [12]–[17], since the Si industry is already familiar with the ALD Hf-based dielectrics for front-end processes. The transition from ALD high-κ on Si to high-κ on III–V compound semiconductors must be easier.

Although high-performance depletion-mode GaAs MOSFETs have been previously demonstrated [10], [12]–[14], the reported inversion-type enhancement-mode (E-mode) GaAs MOSFETs suffer from low drain currents [18]–[20]. In this letter, we report high-performance inversion-type E-mode $In_{0.53}Ga_{0.47}As$ MOSFETs using ALD Al_2O_3 as gate dielectric. The maximum drain current of 367 mA/mm and extrinsic transconductance of 130 mS/mm for a 0.5-μm gate-length MOSFET are achieved, which has a significant improvement over the previously reported inversion-type E-mode $In_{0.20}Ga_{0.80}As$ MOSFETs [19]. Al_2O_3 has a high bandgap ($\sim$9 eV), a high breakdown electric field (5–30 MV/cm), a high permittivity (8.6–10), and a high thermal stability (up to at least 1000 °C), and it remains amorphous under typical processing conditions. Compared to the conventional methods to form thin Al_2O_3 films, i.e., by sputtering, electron beam evaporation, chemical vapor deposition, or oxidation of pure Al films, ALD Al_2O_3 is of much higher quality. [21] The disadvantage for Al_2O_3 is its relative low-κ value compared to other high-κ materials. However, the similar ALD process of HfO_2, HfAlO, or other high-κ dielectrics could be applied to this device structure and significantly reduce the equivalent oxide thickness down to 1–2 nm.

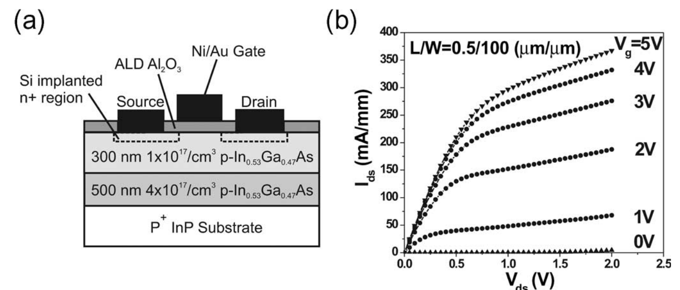

Fig. 1. (a) Cross section of the inversion-type E-mode Al_2O_3/InGaAs MOSFET. (b) Current–voltage (I–V) characteristic of a 0.5-μm mask gate length InGaAs MOSFET with an 8-nm ALD Al_2O_3 as a gate dielectric.

II. Device Structure and Fabrication

Fig. 1(a) shows the cross-sectional schematic of the device structure of an ALD $Al_2O_3/In_{0.53}Ga_{0.47}As$ MOSFET. A 500-nm p-doped 4×10^{17}-cm^{-3} buffer layer and a 300-nm p-doped 1×10^{17}-cm^{-3} $In_{0.53}Ga_{0.47}As$ channel layer were sequentially grown by MBE on a 2-in InP p+ substrate. After surface degreasing and ammonia-based native oxide etching, the wafers were transferred via room ambient to an ASM

Manuscript received May 17, 2007; revised August 1, 2007. This work was supported in part by the National Science Foundation (NSF) Grant ECS-0621949 and in part by the SRC MARCO MSD Focus Center. The review of this letter was arranged by Editor J. del Alamo.

Y. Xuan, Y. Q. Wu, H. C. Lin, and P. D. Ye are with the School of Electrical and Computer Engineering and Birck Nanotechnology Center, Purdue University, West Lafayette, IN 47907 USA (e-mail: yep@purdue.edu).

T. Shen is with the Physics Department, Purdue University, West Lafayette, IN 47907 USA.

Digital Object Identifier 10.1109/LED.2007.906436

0741-3106/$25.00 © 2007 IEEE

F-120 ALD reactor. A 30-nm thick Al_2O_3 layer was deposited at a substrate temperature of 300 °C as an encapsulation layer.

For device fabrication, source and drain regions were selectively implanted with a Si dose of 1×10^{14} cm^{-2} at 30 keV and 1×10^{14} cm^{-2} at 80 keV through the 30-nm-thick Al_2O_3 layer. Implantation activation was achieved by rapid thermal anneal (RTA) at 650 °C–850 °C for 10 s in a nitrogen ambient. An 8-nm Al_2O_3 film was regrown by ALD after removing the encapsulation layer by buffered-oxide-etch (BOE) solution ($BOE : H_2O = 1 : 5$ for 2 min) and soaking in ammonia sulfide for 10 min for surface preparation. After 600-°C PDA in N_2 ambient, the source and drain ohmic contacts were made by an electron beam evaporation of a combination of AuGe/Ni/Au and a lift-off process, followed by an RTA process at 400 °C for 30 s also in a N_2 ambient. The gate electrode was defined by the electron beam evaporation of Ni/Au and the lift-off process. The fabricated MOSFETs have a nominal gate length varying from 0.50 to 40 μm and a gate width of 100 μm. An HP4284 LCR meter was used for the capacitance measurement, and a Keithley 4200 was used for the MOSFET output characteristics.

III. Results and Discussion

Fig. 1(b) shows the dc I_{ds}–V_{ds} characteristics with a gate bias from 0 to 5 V in steps of +1 V. The measured MOSFET has a mask-designed gate length L_{mask} of 0.50 μm and a gate width of 100 μm. L_{mask} is defined by source–drain implantation mask. A maximum drain current of 367 mA/mm is obtained at a gate bias of 5 V and a drain bias of 2 V. The device performance has a significant leap in drain current, compared to our previous results on $In_{0.20}Ga_{0.80}As$ MOSFETs [19]. We ascribe this improvement to the fact that $In_{0.53}Ga_{0.47}As$ is the more forgiving material with respect to the Fermi-level pinning and has a narrower bandgap which makes the realization of electron inversion easier.

The gate leakage current is below 10^{-4} A/cm^2 at 3-V gate bias and around 0.3 A/cm^2 at 5-V gate bias, which is still more than five orders of magnitude smaller than the drain ON-current. The source–drain leakage current is another issue for narrow bandgap semiconductor devices that is caused mainly by drain-induced-barrier-lowing (DIBL) effect and impact ionization. The source–drain leakage current at zero gate bias is $\sim$1 μA from virgin devices and increases to tens of microamperes after multiple measurements or heat cycles at $V_{ds} = 2$ V. It is significantly reduced to less than 5 μA at $V_{ds} = 1$ V even after stress. ON/OFF ratio of $\sim 4 \times 10^3$ is achieved at $V_{gs} = 5$ V (ON) and $V_{gs} = 0$ V (OFF), and $V_{ds} = 1.0$ V on these devices.

Since the fabrication process used is not a self-aligned process, accurate determination of the effective gate length and series resistance is important in evaluating the intrinsic device performance and the potential for further optimization. The inset of Fig. 2(b) shows the effective gate length (L_{eff}) and the series resistance (R_{SD}) extracted by plotting R_{Ch} versus L_{mask}. Here, R_{Ch} is the measured channel resistance. R_{SD} and ΔL are determined to be 15 Ω and

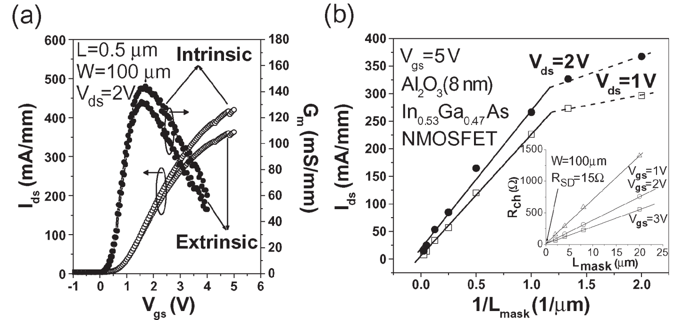

Fig. 2. (a) Extrinsic and intrinsic drain current and transconductance versus gate bias. (b) Drain current at $V_{gs} = 5$ V and $V_{ds} = 2$ V or $V_{ds} = 1$ V versus $1/L_{mask}$. The solid and dashed lines are guided by eyes. Inset: Measured channel resistance versus different mask gate length as a function of gate bias. Three solid fitting lines are used to determine the source and drain contact resistance and ΔL. Here, ΔL is near zero.

< 0.05 μm, respectively. ΔL, which is the difference between L_{mask} and L_{eff}, is negligible in this letter so that $L_{mask} \approx L_{eff} \approx L$.

The maximum extrinsic transconductance G_m is $\sim$130 mS/mm, and the ON-resistance is only 2 $\Omega \cdot$ mm at $V_g = 5$ V. The extrinsic G_m could be further improved by reducing the thickness of the dielectric and improving the quality of the interface. To evaluate the output characteristics more accurately, the intrinsic transfer characteristics are calculated by substracting the half of R_{SD} and are compared with the extrinsic ones in Fig. 2(a). The resulting intrinsic maximum drain current and transconductance for 0.5-μm device are 425 mA/mm and 145 mS/mm, respectively. By the conventional linear region extrapolation method or second derivative method, the extrinsic threshold voltage is determined around 0.25 V. The subthreshold slope and the DIBL for this particular device are 260 mV/decade and 150 mV/V, respectively.

Fig. 2(b) summarizes all measured drain current I_{ds} versus $1/L_{mask}$ under $V_{gs} = 5$ V and $V_{ds} = 2$ V or $V_{ds} = 1$ V. The drain current or transconductance is linearly and inversely proportional to L_{mask}, as expected, and starts to saturate at $L_{mask} = 0.75$ μm. For a simple linear extrapolation, we expect to have the maximum drain current of 510 mA/mm for 0.25-μm device and 930 mA/mm for 0.1 μm, not considering parasitic resistance and short-channel effect. The large subthreshold slope or m-factor indicates that D_{it} of $Al_2O_3/In_{0.53}Ga_{0.47}As$ is still significant compared to SiO_2/Si interface. With the optimization of surface preparation and high-κ dielectric formation process, the drain current and the G_m could increase at least a factor of two to three further [9].

Detailed capacitance–voltage (C–V) measurements of MOS capacitors, fabricated on the same device wafers, are also carried out to evaluate the interface quality of ALD Al_2O_3 on $In_{0.53}Ga_{0.47}As$, as shown in Fig. 3(a). The high-frequency (HF) C–V at 10 kHz shows a clear transition from accumulation to depletion for a typical p-type MOS capacitor. The inversion features of low-frequency (LF) C–V from 1 kHz down to 300 Hz indicate that the conventional Fermi-level pinning phenomenon on III–V is overcome in this ALD-$Al_2O_3/In_{0.53}Ga_{0.47}As$ interface. We ascribe the small (3% per decade) frequency dispersion at accumulation capacitance to the relative high D_{it} at the

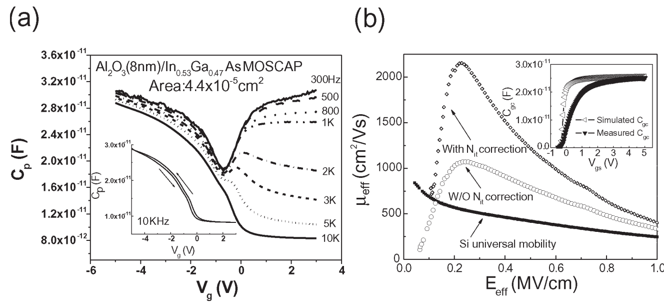

Fig. 3. (a) C–V characteristics of the 8-nm Al_2O_3/InGaAs MOS structures at multiple frequencies from 10 kHz down to 300 Hz. The data are taken at room temperature and in dark. The inset shows 100-mV hysteresis observed in bidirectional C–V measurement at 10 kHz. (b) Effective electron mobility μ_{eff} versus effective electric field E_{eff} measured on the ALD $Al_2O_3/In_{0.53}Ga_{0.47}As$ E-mode MOSFETs. The filled square line is the Si universal mobility for electrons [22]. The empty circle line is calculated by the dc split C–V method without an interface trap (N_{it}) correction. The empty diamond line is with an N_{it} correction after the method developed by Zhu *et al.* [24]. The inset shows the measured split C–V from a 40 × 100 μm^2 device at 100 kHz and a simulated curve with EOT = 5.3 nm for the mobility extraction.

valence band edge, although the extrinsic parasitic effects could also contribute to it. The midgap D_{it} is estimated to be around $1.4 \times 10^{12}/cm^2 \cdot eV$ which is determined by the HF–LF method. Moderate hysteresis of ∼100 mV exhibits in the C–V loops, as shown in the inset of Fig. 3(a).

Effective mobility is another important parameter to evaluate the MOSFET performance. DC "split C–V" method is used to measure the channel capacitance of a 40-μm gate-length device which can be used to calculate the total inversion charge in the channel by integrating the C–V curve. The effective mobility μ_{eff} has a peak value of 1100 $cm^2/V \cdot s$ around a normal electric field E_{eff} of 0.25 MV/cm and twice higher μ_{eff} than the Si universal mobility [22] at E_{eff} of 0.50 MV/cm, as shown in Fig. 3(b). It is slightly higher than the mobility value from strain silicon. [23] The peak μ_{eff} increases to 2200 $cm^2/V \cdot s$ after the correction of overestimated inversion charge by the dc split C–V due to the interface traps [24]. More sophisticated measurement by pulse I–V and pulse C–V is ongoing. A better mobility performance is expected to be achievable by further optimizing the dielectric formation and the device fabrication process.

IV. Conclusion

In summary, we have demonstrated the high-performance inversion-type E-mode $In_{0.53}Ga_{0.47}As$ MOSFETs using ALD high-κ gate dielectrics. These results suggest that $In_{0.53}Ga_{0.47}As$ could be an ideal channel material, which has higher electron effective mobility, low surface recombination velocity to have enough inversion charge, and wide enough bandgap for ultimate CMOS applications with low drain voltage.

Acknowledgment

The authors would like to thank M. A. Alam, M. Lundstrom, J. Woodall, G. D. Wilk, Z. Cheng, A. Lochtefeld, R. M. Wallace, and A. Kummel for the valuable discussions.

References

[1] T. Mimura and M. Fukuta, "Status of the GaAs metal–oxide–semiconductor technology," *IEEE Trans. Electron Devices*, vol. ED-27, no. 6, pp. 1147–1155, Jun. 1980. and references therein.

[2] C. W. Wilmsen, *Physics and Chemistry of III–V Compound Semiconductor Interfaces*. New York: Plenum, 1985. and references therein.

[3] B. J. Skromme, C. J. Sandroff, E. Yablonovitch, and T. Gmitter, "Effects of passivating ionic films on the photoluminescence properties of GaAs," *Appl. Phys. Lett.*, vol. 51, no. 24, pp. 2022–2024, Dec. 1987.

[4] G. G. Fountain, R. A. Rudder, S. V. Hattangady, R. J. Markunas, and J. A. Hutchby, "Demonstration of an n-channel inversion mode GaAs MISFET," in *IEDM Tech. Dig.*, Dec. 1989, pp. 887–889.

[5] S. Tiwari, S. L. Wright, and J. Batey, "Unpinned GaAs MOS capacitors and transistors," *IEEE Electron Devices Lett.*, vol. 9, no. 9, pp. 488–490, Sep. 1988.

[6] Y. H. Jeong, K. H. Choi, and S. K. Jo, "Sulfide treated GaAs MISFETs with gate insulator of photo-CVD grown P_3N_5 film," *IEEE Electron Devices Lett.*, vol. 15, no. 7, pp. 251–253, Jul. 1994.

[7] M. Passlack, M. Hong, J. P. Mannaerts, R. L. Opila, S. N. G. Chu, N. Moriya, F. Ren, and J. R. Kwo, "Low D_{it}, thermodynamically stable Ga_2O_3-GaAs interfaces: Fabrication, characterization, and modeling," *IEEE Trans. Electron Devices*, vol. 44, no. 2, pp. 214–225, Feb. 1997.

[8] M. Hong, J. Kwo, A. R. Korton, J. P. Mannaerts, and A. M. Sergent, "Epitaxial cubic Gd_2O_3 as a dielectric for GaAs passivation," *Science*, vol. 283, no. 5409, pp. 1897–1900, Mar. 1999.

[9] F. Ren, J. M. Kuo, M. Hong, W. S. Hobson, J. R. Lothian, J. Lin, H. S. Tsai, J. P. Mannaerts, J. Kwo, S. N. G. Chu, Y. K. Chen, and A. Y. Cho, "$Ga_2O_3(Gd_2O_3)$/InGaAs enhancement-mode n-channel MOSFETs," *IEEE Electron Devices Lett.*, vol. 19, no. 8, pp. 309–311, Aug. 1998.

[10] Y. C. Wang, M. Hong, J. M. Kuo, J. P. Mannaerts, J. Kwo, H. S. Tsai, J. J. Krajewski, Y. K. Chen, and A. Y. Cho, "Demonstration of submicron depletion-mode GaAs MOSFETs with negligible drain current drift and hysteresis," *IEEE Electron Devices Lett.*, vol. 20, no. 9, pp. 457–459, Sep. 1999.

[11] K. Rajagopalan, R. Droopad, J. Abrokwah, P. Zurcher, P. Fejes, and M. Passlack, "1-μm enhancement mode GaAs N-channel MOSFETs with transconductance exceeding 250 mS/mm," *IEEE Electron Devices Lett.*, vol. 28, no. 2, pp. 100–102, Feb. 2007.

[12] P. D. Ye, G. D. Wilk, J. Kwo, B. Yang, H.-J. L. Gossmann, M. Frei, S. N. G. Chu, J. P. Mannaerts, M. Sergent, M. Hong, K. Ng, and J. Bude, "GaAs MOSFET with oxide gate dielectric grown by atomic layer deposition," *IEEE Electron Device Lett.*, vol. 24, no. 4, pp. 209–211, Apr. 2003.

[13] P. D. Ye, G. D. Wilk, B. Yang, J. Kwo, H.-J. L. Gossmann, S. N. G. Chu, S. Nakahara, H.-J. L. Gossmann, J. P. Mannaerts, M. Sergent, M. Hong, K. Ng, and J. Bude, "GaAs MOSFET with nm-thin dielectric grown by atomic layer deposition," *Appl. Phys. Lett.*, vol. 83, no. 1, pp. 180–182, Jul. 2003.

[14] P. D. Ye, G. D. Wilk, B. Yang, J. Kwo, H.-J. L. Gossmann, M. Hong, K. Ng, and J. Bude, "Depletion-mode InGaAs MOSFET with oxide gate dielectric grown by atomic-layer deposition," *Appl. Phys. Lett.*, vol. 84, no. 3, pp. 434–436, Jan. 2004.

[15] I. Ok, H. Kim, M. Zhang, T. Lee, F. Zhu, L. Yu, S. Koveshnikov, W. Tsai, V. Tokranov, M. Yakimov, S. Oktyabrsky, and J. C. Lee, "Self-aligned n- and p-channel GaAs MOSFETs on undoped and P-type substrates using HfO_2 and silicon interface passivation layer," in *IEDM Tech. Dig.*, Dec. 2006, pp. 829–832.

[16] F. Gao, S. J. Lee, R. Li, S. J. Whang, S. Balakumar, D. Z. Chi, C. C. Kean, S. Vicknesh, C. H. Tung, and D.-L. Kwong, "GaAs p- and n-MOS devices integrated with novel passivation (plasma nitrdation and AlN-surface passivation) techniques and ALD-HfO_2/TaN gate stack," in *IEDM Tech. Dig.*, Dec. 2006, pp. 833–836.

[17] Y. Sun, S. J. Koester, E. W. Kiewra, K. E. Fogel, D. K. Sadana, D. J. Webb, J. Fompeyrine, J.-P. Locquet, M. Sousa, and R. Germann, "Buried-channel $In_{0.70}Ga_{0.30}As/In_{0.52}Al_{0.48}As$ MOS capacitors and transistors with HfO_2 gate dielectrics," in *Proc. 64th Device Res. Conf. Dig.*, Jun. 2006, pp. 49–50.

[18] F. Ren, M. Hong, W. S. Hobson, J. M. Kuo, J. R. Lothian, J. P. Mannaerts, J. Kwo, S. N. G. Chu, Y. K. Chen, and A. Y. Cho, "Demonstration of enhancement-mode p- and n-channel GaAs MOSFETs with $Ga_2O_3(Gd_2O_3)$ as gate oxide," *Solid State Electron.*, vol. 41, no. 11, pp. 1751–1753, Nov. 1997.

[19] Y. Xuan, H. C. Lin, P. D. Ye, and G. D. Wilk, “Capacitance–voltage studies on enhancement-mode InGaAs metal–oxide–semiconductor field-effect-transistor using atomic-layer-deposited dielectric,” *Appl. Phys. Lett.*, vol. 88, no. 26, pp. 263 518–263 520, Jun. 2006.

[20] S. Oktyabrsky, V. Tokranov, M. Yakimov, R. Moore, S. Koveshnikov, W. Tsai, F. Zhu, and J. C. Lee, “High-κ gate stack on GaAs and InGaAs using *in situ* passivation with amorphous silicon,” *Mater. Sci. Eng. B*, vol. 135, no. 3, pp. 272–274, Dec. 2006.

[21] H. C. Lin, P. D. Ye, and G. D. Wilk, “Leakage current and breakdown electric-field studies on ultrathin atomic-layer-deposited Al_2O_3 on GaAs,” *Appl. Phys. Lett.*, vol. 87, no. 18, pp. 182 904–182 906, Oct. 2005.

[22] S. Takagi, A. Toriumi, M. Iwase, and H. Tango, “On the universality of inversion layer mobility in Si MOSFETs: Part I—Effects of substrate impurity concentration,” *IEEE Trans. Electron Devices*, vol. 41, no. 12, pp. 2357–2362, Dec. 1994.

[23] T. Mizuno, N. Sugiyama, T. Tezuka, T. Numata, and S. Takagi, “High-performance strained-SOI CMOS devices using thin film SiGe-on-Insulator technology,” *IEEE Trans. Electron Devices*, vol. 50, no. 4, pp. 988–994, Apr. 2003.

[24] W. Zhu, J. P. Han, and T. P. Ma, “Mobility measurement and degradation mechanisms of MOSFETs made with ultrathin high-κ dielectrics,” *IEEE Trans. Electron Devices*, vol. 51, no. 1, pp. 98–105, Jan. 2004.