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Formation and characterization of nanometer scale metal-oxide-semiconductor structures on GaAs using low-temperature atomic layer deposition

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Atomic layer deposition (ALD) grown Al_2O_3 has excellent bulk and interface properties on III-V compound semiconductors and is used as gate dielectric for GaAs and GaN metal-oxide-semiconductor field-effect transistors (MOSFETs). The low-temperature (LT) ALD technology enables us to fabricate 100 nm MOS structures on GaAs, defined by nanoimprint lithography. The electrical characterization of these nanostructured dielectrics demonstrates that the bulk oxide films and the oxide-GaAs interfaces are of high quality even in nanometer scale. The submicron gate length GaAs MOSFET formed by LT-ALD and lift-off process shows well-behaved transistor characteristics. This GaAs MOSFET process is ready to scale the gate length below 100 nm for ultra-high-speed or THz transistor applications. *© 2005 American Institute of Physics*. [DOI: 10.1063/1.1954902]

The search for alternative gate dielectrics has gained considerable attention recently because technology roadmaps predict the need for a sub-20 Å Si-oxide gate dielectric for sub-0.1 μm Si complementary metal-oxide-semiconductor field-effect transistors (MOSFETs) and suggests the atomic layer deposition (ALD) for high-*k* gate oxides and diffusion barriers for back-end interconnects.[1] ALD is an ultra-thin-film deposition technique based on sequences of self-limiting surface reactions enabling thickness control on atomic scale. ALD finds its applications not only in dielectrics for electronic devices, but also in other frontier research fields; for microelectromechanical systems devices,[2] photonic crystal devices,[3] and carbon nanotube transistors.[4,5] We have applied ALD to grow high-*k* gate dielectrics on III-V compound semiconductors with high-mobility channels and demonstrated GaAs and GaN MOSFETs with excellent device performance.[6–9] The ultimate ultra-high-speed MOSFETs or THz MOSFETs should include the following three features: (1) high-*k* dielectrics (2) high mobility carrier channels, and (3) ultrashort gate lengths below 100 nm.

In this letter, we demonstrate an approach to fabricate nanometer scale metal-oxide-semiconductor structures on GaAs using newly developed low-temperature ALD growth. The nanometer features are defined by nanoimprint lithography.[10] It verifies the feasibility to fabricate a high-mobility GaAs MOSFET with a high-*k* dielectric and with a gate length of 100 nm or below. A direct relevant work has been reported very recently by Biercuk *et al.*,[11] which demonstrates the feasibility to physically form a nanometer scale gate oxide layer on Si. In conventional Si technology, the gate oxide layer and the polysilicon layer are deposited subsequently on the whole wafer. The gate is defined by lithography and dry etching process. The gate oxide remains nearly intact through the whole process, protected mainly by the thick polysilicon layer. In contrast, conventional GaAs technology, for example, GaAs metal-semiconductor field-effect transistors (MESFETs) and high-electron-mobility transistors (HEMTs), uses the so called lift-off process to form the metallic gate at the final stage of the whole wafer process. Our GaAs MOSFET process uses mainly the conventional GaAs technology except that we deposit the gate oxide layers on the whole GaAs wafers before the device fabrication. The gate oxide exposes to the whole device process, which could lead to the degradation of the oxide quality and oxide-semiconductor interface. It would be of great interest to explore a novel process on GaAs, which forms the gate oxide dielectric together with the metal gate at the final stage of the wafer process, eliminating the sources for oxide degradation. The standard growth temperature for conventional plasma-enhanced chemical vapor deposition or ALD is around 300 °C, which is too high for any kind of photoresist. The low-temperature (LT) ALD process developed here enables us to deposit oxides at the temperature of 25–150 °C, which makes the resist lift-off process possible after ALD growth. To selectively deposit dielectrics on GaAs using resist patterns is not only demonstrated for the features ~1 μm defined by photolithography, but also features below 100 nm defined by nanoimprinting lithography. We characterize the electrical properties of these nanometer scale LT-ALD gate oxide layers on GaAs by *I-V* and *C-V* measurements. It shows low gate leakage current density, high breakdown electrical field, and good quality of interfaces of LT-ALD films on GaAs at nanometer scale.

The starting material was 2 in. Si-doped GaAs wafers. A nanoimprint process was applied to form 100 nm wide periodic resist lines on the whole 2 in. wafers. To do so, the GaAs wafer was first spin coated with a thin imprint resist

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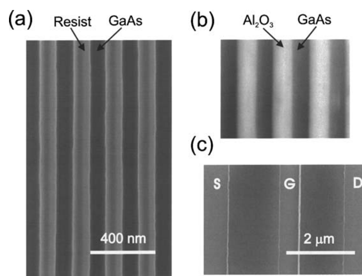

FIG. 1. Scanning electron micrographs of (a) the resist strips with a period of 200 nm, a width of 100 nm, and a height of 100 nm homogeneously across the entire 2 in. *n*-type GaAs wafer generated by nanoimprint lithography; (b) a periodic Al_2O_3 dielectric pattern, transferred from a periodic resist pattern, after LT-ALD and lift-off process; and (c) a 0.65 μm MOS gate of a GaAs MOSFET formed by photolithography, LT-ALD, and lift-off process.

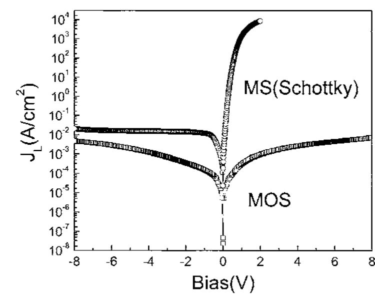

FIG. 2. Measured *I-V* characteristic for both a MOS capacitor (empty squares) and a metal-semiconductor (MS) Schottky diode (empty circles).

layer with thickness of 180 nm. After spin coating, the wafer was baked at 80 °C for 1 h to dry out solvent in the resist layer. The resist used was NP-69, a thermoplastic imprint resist with glass transition temperature of 60 °C. In the nanoimprint process, a 4-in.-diameter 200 nm period SiO_2-on-Si grating mold was used.[12] The nanoimprint process was conducted at temperature of 100 °C and pressure of 100 psi using parallel plate imprint machine. As shown in Fig. 1(a), the patterned resist grating on the GaAs wafer has a period, width, and depth of 200, 100, and 120 nm, respectively. O_2 plasma dry etching was then applied to clean up the resist residues remaining in the gap of the resist strips. Another type of resist patterns was formed by Shipley photoresist 1811 and photolithography with the smallest feature of ~0.5 μm. The Shipley photoresist hardens once the temperature reaches 140–150 °C. After forming the resist patterns on GaAs surface, the wafer was cleaved into different pieces and transferred to an ASM Pulsar2000™ ALD module to grow ALD films. A 160 Å Al_2O_3 oxide layer was deposited at different substrate temperatures of 25, 50, 100, and 150 °C. All deposited Al_2O_3 films in this letter are amorphous, which is favorable for gate dielectrics. Following the growth step, the lift-off procedure was carried out by immersing samples in acetone at 60 °C for a few hours. Ultrasonic pulses were used to dislodge remaining sections of resist. The ALD process is a conformal deposition and has good step coverage in general. This ALD characteristic makes the lift-off process much more difficult compared to lift-off the deposited metal films. This problem can be eventually solved by applying nonconformal dielectric formation technique, for example, ALD using supersonic molecular-beam techniques.[13] A better lift-off procedure was carried out by immersing samples in Shipley SVC 175 resist stripper at 110 °C for 10 min. This lift-off procedure succeeds for Shipley photoresist with ALD growth temperature of up to 150 °C and nanoimprint resist with growth temperature of 25 and 50 °C. The resist pattern fabricated by the nanoimprint process in this work starts to soften once the temperature is higher than 60 °C (i.e., T_g) and eventually becomes a viscous glass state at higher temperature. However, this critical temperature can be increased if we use different imprint resists, such as polymethylmethacrylate, which has a much higher T_g of 105 °C.[10] Figure 1(b) is the scanning electron microscopic image of periodic Al_2O_3 strips on GaAs surface after room temperature ALD growth and lift-off. The edge roughness of these patterned oxide gates is less than 5 nm, which could be limited by lithography, but not by ALD growth or lift-off. Figure 1(c) shows Al_2O_3 field-effect transistor patterns defined by photolithography and ALD grown at the temperature of 100 °C. The 0.65 μm length gate is well defined, showing the edge roughness less than 100 nm. A similar lift-off result is also accomplished if a thin Ti/Au (100 Å/1000 Å) metal film is deposited directly on ALD film to form a MOS gate.

First, we focus on the intrinsic properties of the nanopatterned LT-ALD oxide. It is possible to physically generate 100-nm-wide Al_2O_3 strips, as shown in Fig. 1(b). However, it is very challenging to directly contact such a small feature for electrical property measurement. An alternative approach is to deposit 200-nm-thick Au metal disks on nanopatterned samples directly after LT-ALD growth, as depicted in the inset of Fig. 3. Here, the height of photoresist is approximately 120 nm, which is one order of magnitude larger than the thickness of LT-ALD Al_2O_3. The leakage current through the resist strips is negligible. The leakage current measured from this kind of metal-insulator-semiconductor capacitor is the average leakage current between the metal gate and the GaAs substrate through 100-nm-wide oxide films located in between resist strips. The active dielectric area is just about half of the capacitor disk area. The open squares in Fig. 2 show the measured leakage current density for the MOS capacitors with 16 nm thick LT-grown ALD Al_2O_3. The growth temperature is as low as 25 °C. The open circles are the leakage current density for a reference sample where the metal disk was deposited directly on the clean GaAs surface, forming a Schottky contact. The leakage current of the MOS structure is generally lower than that of Schottky contact. In particular, under positive gate bias, the leakage current of the MOS structure is six to seven orders of magnitude lower than that of the Schottky contact. The breakdown electric field strength for this LT-ALD Al_2O_3 is also ~5 MV/cm, a value similar to the standard ALD Al_2O_3. It demonstrates the high quality of bulk ALD oxide even grown at room temperature and with 100 nm features.

Figure 3 shows the *C-V* characteristics measured at 100 kHz on a 200 μm diameter gate capacitor, which contains nanopatterned dielectrics grown by LT-ALD, as illustrated in the inset. This approach avoids the technical challenge to measure a very small capacitance (smaller than 1 pF) of an individual dielectric with a width of 100 nm. The capacitance contribution from the metal on the resist strips is very small compared to the capacitance part of the metal sitting directly on the dielectrics in between the resist strips. The well-behaved high-frequency *C-V* characteristic shows the clear accumulation and depletion at positive and negative biases. $C_{ox}=\varepsilon_o\varepsilon_{ox}A/d_{ox}$, where ε_o is vacuum permittivity; *A*

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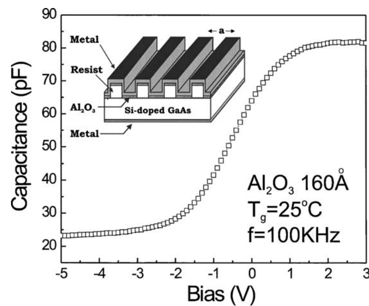

FIG. 3. Measured *C-V* characteristic for a MOS capacitor with a 16 nm LT-ALD Al_2O_3 on *n*-type (100) GaAs with a nanoimprinted resist pattern. Inset: Sketch of a one-dimensional resist grating on top of GaAs surface with 16 nm LT-ALD Al_2O_3 and electron-beam deposited Au layers. Another thin Au film is deposited on the back side of the sample. The period *a* of the resist grating is 200 nm. The width of the resist strips is 100 nm.

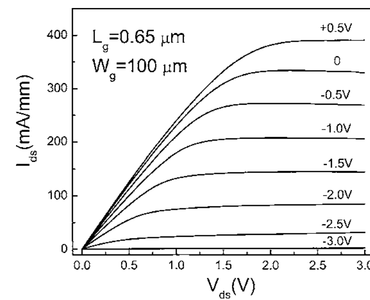

FIG. 4. Drain current vs drain bias as a function of gate bias of a GaAs MOSFET. The gate length is 0.65 μm. The MOS gate is formed by a 16 nm Al_2O_3 grown at 100 °C and electron-beam deposited Ti/Au and lift-off process.

is the active capacitor area, which is about half the area of a 200 μm disk; d_{ox} is the oxide thickness which is 16 nm here; and C_{ox} is the measured capacitance at the accumulation region. The calculated permittivity of room temperature grown ALD Al_2O_3 is 9.4, which is near 10, the permittivity value of ALD Al_2O_3 grown at 300 °C. The lower permittivity value indicates that the quality of LT-ALD films is slightly different from that of the standard 300 °C grown films. The quality of the oxide-semiconductor interface is the most critical part to realize functional GaAs MOSFETs. By analyzing the *C-V* curves, the midgap interface trap D_{it} of LT-ALD Al_2O_3 on GaAs is $\sim 10^{12}/cm^2$ eV. It is approximately one order of magnitude higher than the value reported on 300 °C grown ALD Al_2O_3 on GaAs.[6] The higher D_{it} could be due to the GaAs surface damage induced by the nanoimprint process or due to the LT-ALD process. More work is needed to distinguish these two different physical origins.

The previously reported process is to form the dielectric by ALD at 300 °C immediately after molecular beam epitaxy (MBE) or metalorganic chemical vapor deposition epilayer growth. The device fabrication process degrades the quality of the gate oxide and increases the gate leakage current. The process reported here is to deposit the gate dielectric and metal gate using one photoresist mask as the final device process step. The room temperature or LT-ALD growth enables the photoresist patterns to remain intact after dielectric growth and makes it possible to deposit the dielectric and lift-off to form the final MOS structure just as simply as the commonly used metal deposition and lift-off process. This novel process opens the possibility to fabricate GaAs MOSFETs using the standard GaAs MESFET or GaAs HEMT manufacture lines with minimum change of the existing process. A submicron gate length GaAs MOSFET was fabricated using this novel LT-ALD and lift-off process. A 1500 Å undoped GaAs buffer layer and a 1000 Å Si-doped GaAs layer $(4 \times 10^{17}/cm^3)$ were sequentially grown by MBE on a semi-insulating GaAs substrate. Device isolation was achieved by oxygen implantation. Ohmic contacts serving as sources, and drains were formed by electron-beam deposition of Au/Ge/Au/Ni/Au and a lift-off process, followed by a 435 °C anneal in a forming gas ambient. After photolithography defining the gate, the wafer or the sample was transferred to an ALD module to deposit Al_2O_3 at the temperature of 25–100 °C and an electron-beam deposition chamber to deposit Ti/Au metal film. The lift-off process requires warm resist stripper and/or ultrasound to form the gate electrodes. Depending on the growth temperature, the resist thickness, the resist undercut shapes, and the gate feature size, special approaches might be needed to have a clean lift-off. Figure 4 shows the measured drain current versus drain voltage (I_{ds} versus V_{ds}) characteristics of a GaAs MOSFET whose gate was formed by 100 °C ALD oxide growth and a lift-off process. The gate voltage is varied from −1.5 to +1.0 V with 0.25 V step. The extrinsic peak transconductance g_m is ~125 mS/mm, which is similar to the devices with ALD oxide grown at 25 °C or 50 °C. Si MOSFETs with the gate length of 60 nm were already demonstrated on 4 in. wafer using nanoimprint at all lithography levels.[14] There is no physical limitation using this LT-ALD and lift-off process to fabricate a GaAs MOSFET with a 100 nm gate length, which can be either defined by nanoimprint lithography or by another advanced lithography, for example, electron-beam lithography.

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