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High-performance GaAs metal-insulator-semiconductor field-effect transistors enabled by self-assembled nanodielectrics

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High-performance GaAs metal-insulator-semiconductor field-effect-transistors (MISFETs) fabricated with very thin *self-assembled organic nanodielectrics (SANDs)*, deposited from solution at room temperature, are demonstrated. A submicron gate-length depletion-mode *n*-channel GaAs MISFET with SAND thicknesses ranging from 5.5 to 16.5 nm exhibit a gate leakage current density $<10^{-5}$ A/cm^2 at a gate bias smaller than 3 V, a maximum drain current of 370 mA/mm at a forward gate bias of 2 V, and a maximum intrinsic transconductance of 170 mS/mm. The importance of appropriate GaAs surface chemistry treatments on SAND/GaAs interface properties is also presented. Application of SANDs to III-V compound semiconductors affords more opportunities to manipulate the complex III-V surface chemistry with broad materials options. © *2006 American Institute of Physics*. [DOI: 10.1063/1.2358202]

Heterogeneous integration of novel dielectrics and novel channel materials has recently gained increasing attention as a necessity to further drive Si complementary metal-oxide-semiconductor (CMOS) integration, functional density, speed and power dissipation, and to extend CMOS front-end fabrication to and beyond the 22 nm node. Using III-V compound semiconductors as conduction channels, to replace traditional Si or strained Si, is currently an active research frontier due to the excellent electrical properties of III-V compound semiconductors and the existence of a viable III-V industry for more than 30 years. The principal obstacle to III-V compound semiconductors rivaling or exceeding the properties of Si electronics has been the lack of high-quality, thermodynamically stable insulators on GaAs (or on III-V materials in general) that equal the outstanding properties of SiO_2 on Si, e.g., a mid-band gap interface-trap density (D_{it}) of $\sim 10^{10}/\mathrm{cm}^2$ eV. For more than four decades, the research community has searched for suitable III-V compound semiconductor gate dielectrics or passivation layers. The literature testifies to the extent of this effort,[1,2] with representative, currently active approaches including sulfur passivation,[3] silicon interface control layers (Si ICLs)[4–6], *in situ* molecular beam epitaxy (MBE) growth of $Ga_2O_3(Gd_2O_3)$,[7] *ex situ* atomic layer deposition (ALD) growth of Al_2O_3 and HfO_2,[8–10] wet oxidation of InAlP,[11] jet vapor deposition[12] of Si_3N_4, and ALD or PVD of HfO_2+Si ICL.[13,14]

In this letter, we report a completely different approach–GaAs metal-insulator-semiconductor field-effect-transistors (MISFETs) exhibiting excellent performance can be fabricated under mild conditions using simple equipment and very thin biomembrane-like *self-assembled nanodielectrics (SANDs)* as the insulating layer. Primarily developed for enhancing the response of organic thin-film transistors (OTFTs), self-assembled organic gate dielectrics can be deposited at room temperature via layer-by-layer solution phase techniques using organosilane precursors.[15,16] This yields smooth, nanostructurally well-defined, strongly adherent, thermally stable, virtually pinhole-free, organosiloxane thin films exhibiting excellent insulating properties (leakage current densities as low as 10^{-9} A/cm^2 with native SiO_2 on Si), a large single Stb layer (Fig. 1) capacitance (up to ~ 0.025 pF/μm^2) and dielectric constant (k) of ~ 16, enabling OTFT function at very low operating voltages.[15,16] These dielectrics exhibit good uniformity over areas as large as ~ 150 cm^2, are insoluble in common solvents, can be patterned using standard microelectronic etching methodologies, and adhere to/are compatible with a wide range of substrates. The work reported in this letter unambiguously demonstrates facile integration of SANDs with III-V compound semiconductors.

For the present GaAs MISFET devices (Fig. 1) we employed a 700–900 Å Si-doped ($4\times10^{17}/\mathrm{cm}^3$) GaAs layer as the channel and a 1500 Å C-doped ($5\times10^{16}/\mathrm{cm}^3$) GaAs buffer layer on a P+ GaAs substrate grown by metalorganic chemical vapor deposition (MOCVD). Device isolation was achieved by oxygen implantation. Activation annealing was performed at the same time as ohmic contact formation. Ohmic contacts were formed by e-beam deposition of Au/Ge/Au/Ni/Au structures and a lift-off process, followed by 400 °C annealing in an N_2 ambient. Prior to SAND deposition, hydrophilic or hydrophobic GaAs surfaces were prepared using NH_4OH or HCl pretreatments, respectively. The SAND growth process (see Fig. 1) was as follows: 5 mM **Alk** reagent in dry toluene at 0 °C in N_2 for 1 h; 34 mM **Cap** reagent in dry pentane at 25 °C in N_2 for 25 min; 10 mM **Stb** reagent in dry tetrahydrofuran at 60 °C in N_2 for 15 min, followed by hydrolysis with acetone-H_2O solution to yield a 5.5-nm-thick type III SAND film (Fig. 1). Finally, conventional Ti/Au structures were deposited by e-beam evaporation, followed by lift-off to form the gate electrodes.

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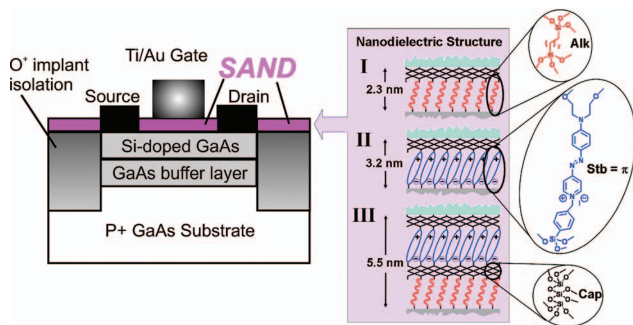

FIG. 1. (Color) Schematic view of a depletion-mode *n*-channel GaAs MISFET (left) with a self-assembled nanodielectric (right) as the insulating layer. The SAND layers were sequentially deposited from solutions of precursors **Alk**, **Stb**, and **Cap**. (type III)$_n$ SANDs [n=1 (5.5 nm thick), 3 (16.5 nm thick)] are used for GaAs MISFET fabrication.

The source-to-gate and the drain-to-gate spacings are $\sim 1\ \mu$m. The sheet resistance and contact resistance are $1.5-2.5\ \mathrm{k}\Omega/\mathrm{sq.}$ (depending on the thickness of *n* channels) and $1.5\ \Omega$ mm, respectively, measured using a transmission length method (TLM). The gate lengths of the measured devices are 0.5 and 1 μm. The process requires four levels of lithography (alignment, isolation, ohmic and gate), all done using a contact printer.

Figures 2(a) and 2(b) illustrate 500 Hz–1 MHz *C-V* measurements on MIS capacitors fabricated with type III SAND layers (Fig. 1) as the insulator in parallel with the MISFETs. The results demonstrate the importance of the GaAs surface pretreatment (NH_4OH vs HCl) on the SAND/GaAs interface quality. Larger frequency dependent flatband shifts, frequency dispersions at accumulation capacitances, and hysteresis are observed for HCl-pretreated devices as shown in Fig. 2(b). Conversely, the NH_4OH pretreatment producing a hydroxylated GaAs surface results in high-quality SAND layers as demonstrated by the *C-V* measurements. Hydroxylated GaAs surfaces favor SAND chemisorption, hence passivation, since the Alk Si–Cl groups react with the GaAs surface OH groups to form strong, covalent bonds (see Fig. 1). More detailed studies of this process are in progress. The typical hysteresis observed in these devices as shown in Fig. 2(a) is less than 80 mV, corresponding to a *slow* trap density of about $2\times 10^{11}/\mathrm{cm}^2\,\mathrm{eV}$. Consequently, all of the MISFET *I-V* characteristics were measured on NH_4OH treated devices. The dielectric constant of the currently employed SAND is $\sim 3-4$ as obtained from *C-V* measurements. Systematic studies with different SAND variants having higher *k* values, different III-V surfaces, such as *n*-type or *p*-type GaAs, InGaAs, and GaN, different pre-

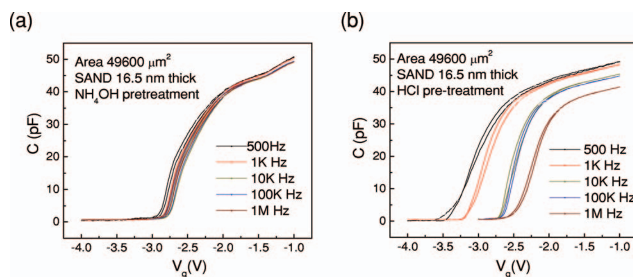

FIG. 2. (Color) (a) *C-V* measurements on a NH_4OH pretreated GaAs MISFET showing small hysteresis and frequency dispersion. (b) *C-V* measurements on HCl pretreated GaAs MISFET showing significant frequency dispersion on the flatband voltage and accumulation capacitance.

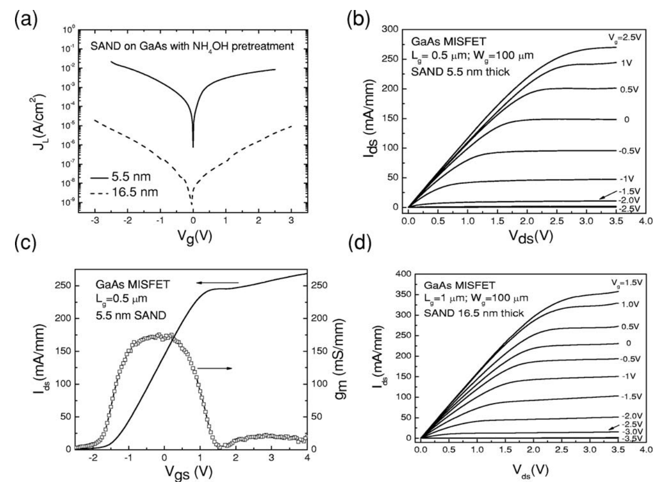

FIG. 3. (a) Leakage current density $J_L(\mathrm{A/cm^2})$ vs gate bias $V_g(V)$ for GaAs MISFETS having different SAND film thicknesses. (b) Drain current vs drain bias as a function of gate bias for a 0.5 μm gate length GaAs MISFET fabricated with a 5.5 nm SAND. (c) Drain current vs gate bias (solid line) and intrinsic transconductance vs gate bias (empty squares) at V_{ds}=3.5 V. (d) Drain current versus drain bias as a function of gate bias for 1 μm GaAs MISFET with 16.5 nm SAND.

deposition surface treatments and different device structures are currently in progress.

Figure 3(a) shows the gate leakage current density (J_L) versus gate bias (V_g) for SANDs deposited on hydroxylated GaAs with film thicknesses ranging from 5.5 nm [type III] to 16.5 nm [(Type III)$_3$]. The 16.5-nm-thick SAND is realized by three successive depositions of a 5.5-nm-thick type III SAND film (Fig. 1). The corresponding gate leakage current of a MISFET having a 1 μm gate length and a 100 μm gate width is very small, 10 pA–10 nA, which is at least six orders of magnitude smaller than the drain current. The dielectric strength of this organic film is as high as 6 MV/cm, comparable to conventional inorganic gate dielectrics such as SiO_2, Si_3N_4 or HfO_2. The small SAND leakage currents and large breakdown strengths are attributed to the heavily three-dimensional cross-linked structures, containing dense arrays of strong Si–O bonds and polarizable π-electron spacers.[15,16] Figure 3(b) shows the *I-V* characteristics for a 0.5 μm-gate-length GaAs MISFET with a 5.5-nm-thick type III SAND film. The 800-Å-thick MOCVD GaAs channel layer leads to a maximum drain current of 280 mA/mm with a pinch-off voltage of -2.5 V. A parasitic resistance of 4 Ω mm is obtained from the resistance of the mobility region in Fig. 3(b). The same number can also be calculated from the measured sheet resistance of 2.5 kΩ/sq. and contact resistance of 1.5 Ω mm from the TLM measurement, using a gate-source spacing of 1 μm. The maximum intrinsic transconductance, g_m, is $\sim$170 mS/mm for L_g=0.5 μm as shown in Fig. 3(c). Such large transconductance values indicate that the interface trap densities are remarkably low. The *I-V* characteristics for a 1 μm-gate-length GaAs MISFET with a 16.5-nm-thick SAND are shown in Fig. 3(d). The maximum drain current density at a forward gate bias of 2.0 V is increased to $\sim$370 mA/mm by employing a 900-Å-thick MOCVD GaAs *n*-channel layer. The device is still cleanly pinched off at a gate bias of -3.5 V, although the insulator layer is 16.5 nm thick. The maximum intrinsic transconductance is $\sim$125 mS/mm by correcting for the parasite resistance of 3 Ω mm. Note that this result does not

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scale with dielectric thickness due to depletion-mode operation, interface trap density, and incomplete electron velocity saturation. The estimated electron mobility from the maximum transconductances measured on 20-μm-long channel devices is $\sim$1875 $cm^2/V\ s$, which is about a factor of 4–5 larger than the mobility in Si-based devices. The relatively large differences in drain current vs channel layer physical thickness, i.e., 370 vs 280 mA/mm for 900 vs 800 Å, is due to some depletion from C-doped $(5\times10^{16}/cm^3)$ *p*-type buffer layer on a P+ GaAs substrate.

In conclusion, we have demonstrated the implementation of SAND nanodielectrics for fabrication of GaAs MISFETs exhibiting excellent transistor characteristics. These results suggest more opportunities for manipulating the complex GaAs surface chemistry with unprecedented materials options and using organic dielectrics for high-performance III-V semiconductor devices. The SAND process is flexible, low-cost, and far simpler to implement than previously reported MBE or ALD dielectric deposition processes.

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