First Experimental Demonstration of Ge CMOS Circuits

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Abstract

We report the first experimental demonstration of Ge CMOS circuits, based on a novel recessed channel and S/D technique. Aggressively scaled non-Si CMOS logic devices with channel lengths (L_{ch}) from 500 to 20 nm, channel thicknesses (T_{ch}) of 25 and 15 nm, EOTs of 4.5 and 3 nm and a small width ratio (W_n:W_p=1.2) are realized on a Ge-on-insulator (GeOI) substrate. The CMOS inverters have high voltage gain of up to 36 V/V, which is the best value among all of the non-Si CMOS results by the standard top-down approach. Scalability studies on Ge CMOS inverters down to 20 nm are carried out for the first time. NAND and NOR logic gates are also investigated.

Introduction

With the continuous device scaling and integration density increasing, Si CMOS technology is approaching its physical limit. High mobility channel materials such as Ge [1-5] and III-V [6-7] are intensively studied. However, most of works are limited to the single MOSFET level. There are only several reports discussing non-Si CMOS logic [8-17].

Recently, we reported a breakthrough in high-performance accumulation-mode Ge nFETs by the recessed channel and S/D [18]. Taking advantage of the doping density gradient along the depth axis, the recess process realizes both heavily doped S/D and lightly doped channel. Thanks to the fully-depleted (FD) ultra-thin-body (UTB) recessed channel, low resistivity recessed S/D contact, well-engineered threshold voltage (V_{TH}) and balanced electron and hole mobilities in Ge, nFETs and pFETs with near symmetrical performance and good voltage transition are achieved in the CMOS inverters with a wide range of supply voltage (V_{DD}), from 1.6 to 0.2 V.

Experiment

Fig. 1 shows the Ge CMOS inverter schematic, highlighting the recessed channel and S/D structures employed in the devices. Fig. 2 briefly summarizes the key fabrication processes. The experiment started with a GeOI wafer with 180 nm lightly n-doped (100) Ge and 400 nm SiO_2 on (100) Si from Soitec™ as shown in Fig. 3(a). After a standard clean, the device isolation was carried out by SF_6 inductively coupled plasma (ICP) dry etching. After the mesa etching, the samples were selectively implanted with P (5×10^{15}/cm^2 at 30 keV) and BF_2 (4×10^{15}/cm^2 at 30 keV) for nFETs and pFETs, respectively, both of which were then activated by a *common* rapid thermal anneal (RTA) at 500 °C for 1 min in N_2 ambient. After that, an optimized *common* SF_6 ICP dry etching with a high aspect ratio was used to form the recessed channel, as shown in the testing structures in Fig. 3(b). Fig. 3(c-d) show the recessed channels in real fabricated devices with T_{ch} of 15 and 25 nm determined by different etching time and adopted in different samples. After smoothing the channel interface by a surface wet clean using cyclic 2% HF rinsing, 1 nm Al_2O_3 was first deposited by ALD at 250 °C and then a post-deposition oxidation (PO) was performed by RTA at 500 °C for 30 s in pure O_2 ambient to grow GeO_x passivating the Al_2O_3/Ge interface. Next, the *common* ALD gate dielectric of 5 or 8 nm Al_2O_3 was deposited at 300 °C for different samples. The overall EOT is calculated to be 3 or 4.5 nm, considering both the Al_2O_3 and the GeO_x. After a post deposition anneal (PDA) at 500 °C for 1 min in forming gas ambient and etching away the oxide in the S/D area, an extra BCl_3/Ar ICP dry etching was used to remove the top Ge layer as the recessed S/D etching. Note that this is one of the key processes in this experiment and the recessed S/D dry etching is carefully calibrated to precisely control the etch rate and etched profile. The etching rate is around 15 nm/min. Fig. 4(a) shows the test recessed S/D structure, indicating that about 20 nm of top Ge was removed. 100 nm Ni was then deposited as the *common* S/D metal contacts, followed by a *common* ohmic anneal by RTA at 250 °C for 30 s in N_2 ambient. The metal gate was formed by 40/60 nm Ti/Au for pFETs and 40/60 nm Ni/Au for nFETs. Finally, devices were connected for CMOS logic gates.

The ratio of nFETs to pFETs gate width is carefully designed to be 1.2:1 (1 μm : 0.85 μm) for balanced performance. Three samples: A (T_{ch} = 15 nm, EOT = 4.5 nm), B (T_{ch} = 25 nm, EOT = 4.5 nm) and C (T_{ch} = 25 nm, EOT = 3 nm) are thoroughly investigated and presented.

Results and Discussion

Fig 4(b) shows the TLM structure under SEM and square Ni metal contacts are placed on isolated conductive Ge with different gaps between each other. Low resistivity Ohmic contacts are realized on both nFETs and pFETs by using common Ni recessed S/D, which greatly simplifies the process complexity compared to using multiple metal layers respectively for n- and p-type contacts. The contact resistances (R_c) are extracted to be 0.45 and 0.37 Ω·mm for Ge n- and p-contacts and 88 and 135 Ω/□ for the sheet resistance (R_{sh}), as shown in Fig. 4(c). The small standard deviations of measured results shown in the inserted figures verify the good uniformity of the recessed S/D contacts. The contact quality could be further improved by optimizing the etching depth of recessed S/D. Fig. 5 explains the basic principles in the recessed channel and S/D structures. Due to the near-Gaussian distribution profile of the doping ions in Ge [18-19], the ion concentration first increases then decreases rapidly along the depth axis into the body. The recess processes, combined with the doping density gradient, result in the realization of a heavily doped S/D region and a lightly doped channel region. Higher doping level in S/D region reduces Schottky barrier width at the metal-semiconductor interface, thus improves the contact resistance [17]. Meanwhile, lower doping level in channel region increases the maximum depletion width, thus enhances the gate control and realizes the enhancement-mode operation in the devices. It also reduces the Coulomb scattering generated by ionized dopants, thus improves the carrier mobilites for both electrons and holes.

Fig. 6(a) depicts the top-down view of the smallest L_{ch} CMOS inverter under SEM and the dark region is SiO_2 in the area with top conductive Ge layer removed during the device isolation. The gate areas of the nFET and pFET in the same inverter shown in Fig. 6(a) are enlarged in Fig. 6(b-c) and the L_{ch} of both devices are 20 nm. Fig. 6(d) gives the bird's eye view of a CMOS inverter. Fig. 7 shows the transfer curves of the nFET and the pFET inside a 50 nm L_{ch} inverter in *sample A* at $|V_{ds}|$ = 0.05, 0.5 and 1 V. With a T_{ch} of 15 nm and an optimized gate stack, both of the two devices show good I_{ON}/I_{OFF} ratios > 1×10^5 and balanced threshold voltages ($|V_{TH}| \sim 0.5$ V). For comparison, transfer curves of a longer channel (L_{ch} = 90 nm) device in *sample B* with a T_{ch} of 25 nm are given in Fig. 8. The short channel effects (SCEs) are greatly suppressed as proved by reduced DIBLs and further improved I_{ON}/I_{OFF} ratios. Fig. 9 presents the I_d-V_{ds} curves of the same two nFETs and pFETs in Fig. 7-8 with $|V_{gs}|$ from 0 V to 3 V in 0.2 V steps, showing near-symmetrical output characteristics.

Fig. 10 shows the voltage transfer curves of the same two inverters shown in Fig. 7-8 with a V_{DD} from 1.6 V to 0.2 V. Longer channel inverter shows a better voltage transition. Further increasing L_{ch} (400 nm), together with reduced EOT (3 nm) in *sample C* yields much steeper V_{OUT} versus V_{IN} curves as shown in Fig. 11. Fig. 12 compares the voltage gains of the same two inverters in Fig. 10 and the 90 nm L_{ch} inverter in sample B has larger voltage gain, proving that better gate electrostatics control leads to steeper voltage transition. Fig. 13 gives the voltage gains of the same long channel inverter in Fig. 11. A High peak voltage gain of 36 V/V is obtained at a V_{DD} of 1.2 V. Fig. 14 shows the peak voltage gain scaling metrics of the three samples at V_{DD} = 1 V. Thinner and longer channel results in an improved voltage gain, indicating a better gate electrostatic control.

Noise margin (NM) is the maximum departure from the ideal logical level that places the gate at a small-signal voltage gain of unity, quantifying the robustness of a gate with respect to the input signal interference. Fig. 15 compares the noise margins of the same two inverters in Fig. 10 in butterfly transfer curves at a V_{DD} of 1.2 V. Fig. 16 shows the NM of the same long channel inverter in Fig. 11 at V_{DD} = 1.2 V, showing a larger NM_H (NM for high input) of 0.5 V and NM_L (NM for low input) of 0.38 V. Both of the noise margins as a function of V_{DD} are depicted in Fig. 17. While the absolute values of NM increase with higher V_{DD}, the ratios to V_{DD} fluctuate around 40%. Scaling metrics of noise margin (NM_L+NM_H) at V_{DD} of 1 V for the three samples are given in Fig. 18. NMs decrease with smaller L_{ch}, due to stronger short channel effects, indicating worse immunity to noises in input signal. Larger NMs are obtained by enhancing the gate electrostatic control through thinning T_{ch} from 4.5 nm to 3 nm and reducing EOT from 4.5 nm to 3 nm.

Transition width (TW) as a function of V_{DD} for the same long channel inverter in Fig. 11 is shown in Fig. 19. TW is defined by the difference between low and high V_{IN} corresponding to a voltage gain of 1. It describes the range of V_{IN} needed to switch the inverter between "1" and "0" states and smaller TW means better voltage transition at certain V_{DD}. The absolute value of TW increases with higher V_{DD}, while the percentage value to V_{DD} decreases and tends to saturate. Fig. 20 provides the L_{ch} dependence of TW for the three samples at V_{DD} = 1 V. Similar to the case of peak voltage gain and noise margin, smaller EOT, thinner and longer channels provide lower TW.

Fig. 21 compares the transient current (I_{DD}) of the three inverters in Fig. 10-11. I_{DD} is the current flowing through the inverter during switching from "1" to "0" states and it partially determines the speed of CMOS logic gates. Shorter channel device has significant large I_{DD} and the I_{DD} increases from 0.12 μA to 7.4 μA with V_{ds} rising from 0.2 V to 1.2 V. Fig. 22 summarizes the scaling trend of the switching current (max I_{DD}) of the three samples at V_{DD} = 1 V. The switching current increases with decreasing L_{ch}. Moreover, by employing larger T_{ch} and smaller EOT, the I_{DD} increases as expected.

Fig. 23 shows the output signals of a 100 nm L_{ch} CMOS inverter in response to input square-wave signals with different frequencies. The output signal still maintains good square-wave shape at 1 kHz. Fig. 24(a) and (b) show the top-down view of a fabricated NAND logic gate under SEM and its circuit diagram. Fig. 25 provides the output signal of a 100 nm L_{ch} NAND gate with two input signals at a supply voltage of 1.2 V. Four combinations of input states "1 1", "0 1", "1 0" and "0 0" are used and the output signal shows sharp transitions. Fig. 26(a) and (b) show the top-down view of a fabricated NOR logic gate under SEM and its circuit diagram. The output signal of a 100 nm L_{ch} NOR gate is provided in Fig. 27 and same testing conditions are applied as used in the NAND gate.

Table 1 compares all of the non-Si CMOS results reported in literature with this work. We have realized the smallest VLSI-related non-Si CMOS inverters fabricated by the top-down approach. A record high peak voltage gain at low V_{DD} (36 V/V at 1.2 V) is obtained on a 400 nm L_{ch} Ge CMOS inverter.

Conclusion

We experimentally demonstrate the first Ge CMOS circuits by a novel recessed channel and S/D technique. Inverters with high voltage gains up to 36 V/V and L_{ch} down to 20 nm are realized. The first scalability study on Ge CMOS inverters is carried out. NAND and NOR logic gates are also investigated in the time domain. This study provides strong evidences of Ge as a promising candidate to replace Si in future's low power and high speed CMOS logic applications.

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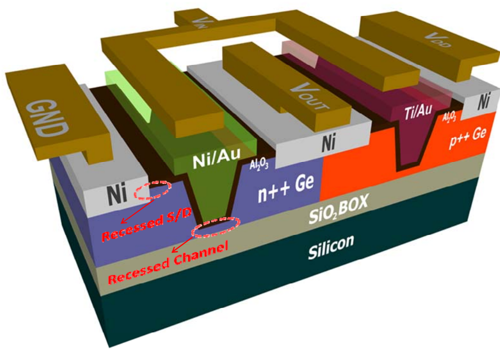

Fig. 1 Device schematic of a Ge recessed channel and S/D CMOS inverter. The recessed channel and S/D structures are highlighted for better illustration.

- Mesa Isolation (SF_6 ICP Dry Etch)
- N-Implantation (P 5×10^{15} 30 keV)
- P-Implantation (BF_2 4×10^{15} 30 keV)
- Common Dopant Activation (500 °C 1min in N_2)
- Common Channel Formation (SF_6 ICP Dry Etch)
  - Process I (T_{ch}=15nm) Process II (T_{ch}=25nm)
- Surface Wet Clean (HF Cyclic Rinse)
- Common Gate Oxide Formation
  - 1st ALD (250°C 1nm Al_2O_3)
  - Oxidation (500°C 30s in O_2)
  - 2nd ALD for Gate Dielectric
    - *Sample A* (300°C 8nm Al_2O_3) With T_{ch}=15nm
    - *Sample B* (300°C 8nm Al_2O_3) With T_{ch}=25nm
    - *Sample C* (300°C 5nm Al_2O_3) With T_{ch}=25nm
  - PDA (500°C 1min in N_2/H_2)
- Common S/D Contacts Formation
  - Local Oxide Etch (BCl_3/Ar ICP Dry Etch)
  - Top Ge Etch (BCl_3/Ar ICP Dry Etch)
  - Metal Deposition (Ni)
  - Ohmic Anneal (250°C 30s in N_2)
- Gate Metal Deposition
  - pFETs (Ti/Au) nFETs (Ni/Au)
- Device Interconnection

Fig. 2 Fabrication process flow of the Ge CMOS in this experiment. Three samples with different conditions are fabricated.

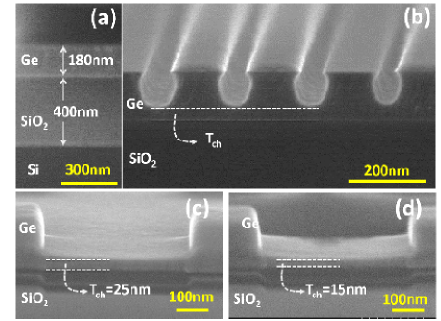

Fig. 3 (a) Cross section of a GeOI substrate. (b) Testing recessed channel structures. (c) The 25 nm T_{ch} channel in *sample B and C*. (d) The 15 nm T_{ch} channel in *sample A*.

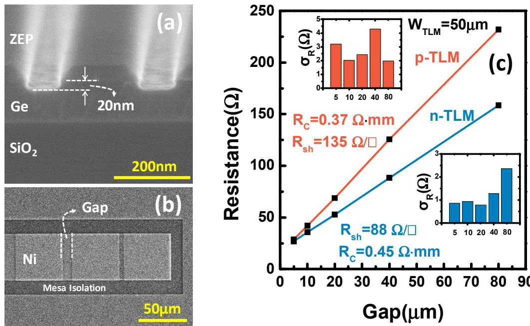

Fig. 4 (a) Testing recessed S/D structures with 20 nm top Ge layer removed. (b) TLM structure under SEM. (c) TLM data for both Ge n-contact and p-contact. Inserted figures show the standard deviation based on 10 measured devices.

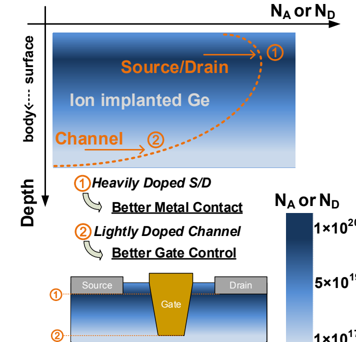

Fig. 5 Basic idea in the recessed S/D and channel. Doping density gradient in the implanted Ge helps to obtain heavily doped S/D and lightly doped channels.

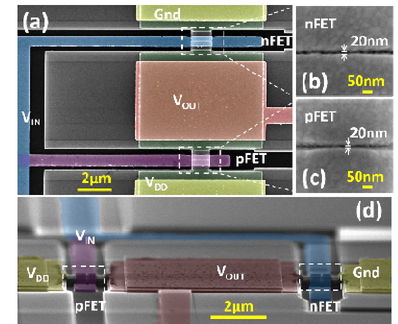

Fig. 6 (a) Top-down view of a fabricated Ge CMOS inverter with the smallest channel length. (b-c) zoom-in images of the gate area in the CMOS inverter in (a), the channel length is 20 nm. (d) Bird's eye view of a CMOS inverter under SEM.

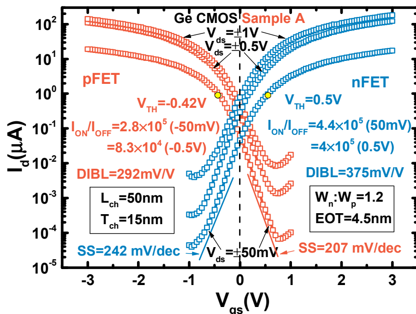

Fig. 7 Transfer curves of the nFET and pFET in a 50 nm L_{ch} CMOS inverter in *sample A*. With the ultra-thin channel, both of devices show good ON and OFF state.

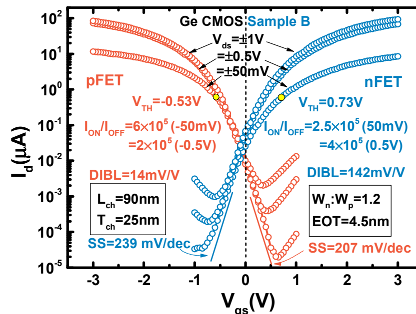

Fig. 8 Transfer curves of the nFET and pFET in a 90 nm L_{ch} CMOS inverter in *sample B*. Because of the longer channel, the SCE is further suppressed.

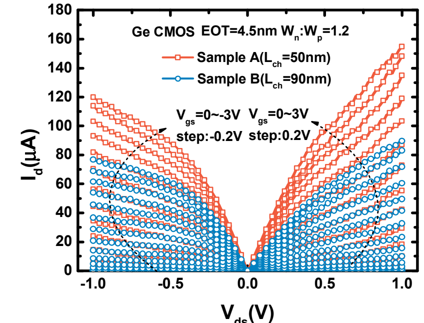

Fig. 9 Output characteristics of the same four devices shown in Fig. 7-8 with a V_{gs} sweeping from 0 V to 3 V for nFETs and 0 V to -3 V for pFETs.

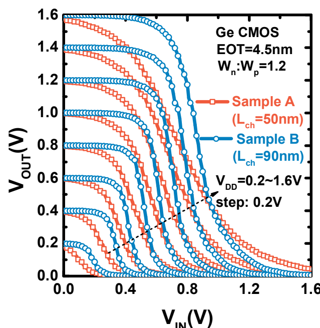

Fig. 10 V_{OUT} versus V_{IN} of the same two CMOS inverters shown in Fig. 7-8 in *sample A and B* with a V_{DD} from 0.2 V to 1.6 V in 0.2 V step.

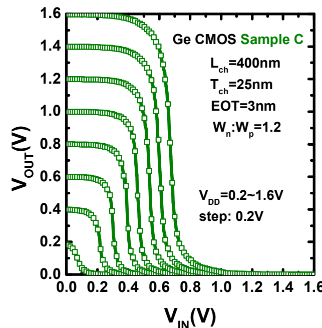

Fig. 11 V_{OUT} versus V_{IN} of a 400 nm long channel inverter in *sample C* with a V_{DD} from 0.2 V to 1.6 V in 0.2 V step.

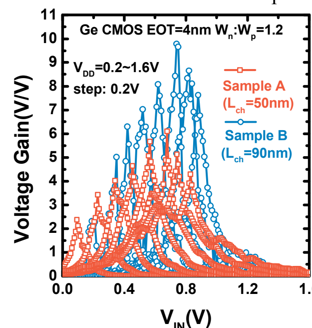

Fig. 12 Voltage gain versus V_{IN} of the same two inverters in *sample A and B* shown in Fig. 10 with a V_{DD} from 0.2 V to 1.6 V in 0.2 V step.

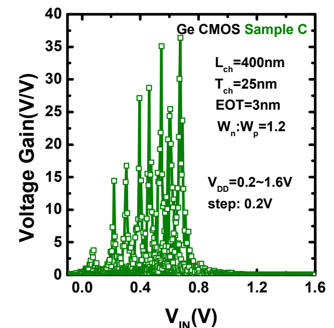

Fig. 13 Voltage gain versus V_{IN} of the same long channel inverter in *sample C* shown in Fig. 11 with a V_{DD} from 1.6 V to 0.2 V in 0.2 V step.

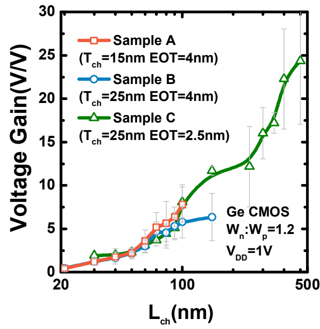

Fig. 14 Channel length dependence of the maximum voltage gain of CMOS inverters in *sample A, B and C* with a V_{DD} of 1 V.

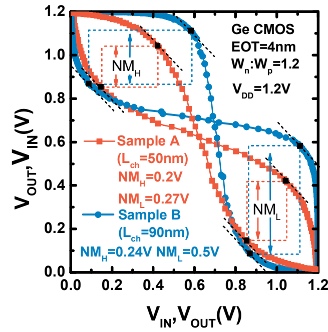

Fig. 15 Noise margin of the same two CMOS inverters in *sample A and B* shown in Fig. 10 with a V_{DD} of 1.2V.

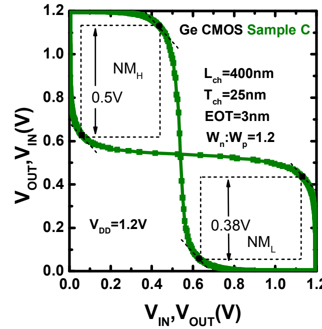

Fig. 16 Noise margin for the same long channel inverter in *sample C* shown in Fig. 11 with a V_{DD} of 1.2 V.

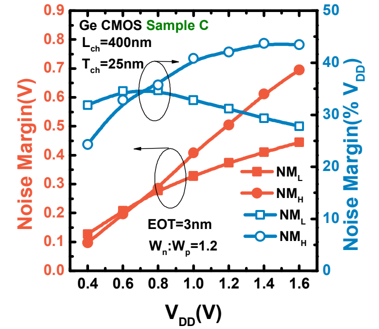

Fig. 17 Noise margin in absolute and percentage value to V_{DD} plotted against V_{DD} of the same long channel inverter in *sample C* shown in Fig. 11

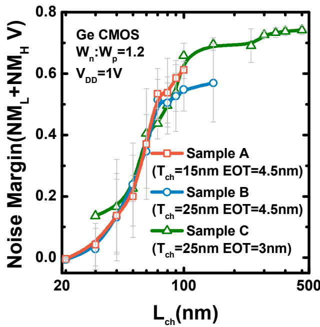

Fig. 18 Noise margin (NM_L+NM_H) scaling metrics of CMOS inverters in *sample A, B and C* with a V_{DD} of 1V.

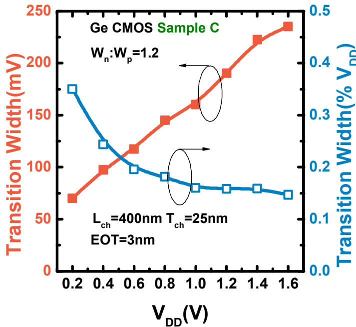

Fig. 19 Transition width in absolute and percentage value to V_{DD} plotted against V_{DD} of the same long channel inverter in *sample C* shown in Fig. 11.

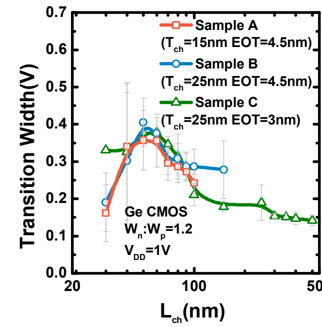

Fig. 20 Channel length dependence of transition width of CMOS inverters in *sample A, B and C* at V_{DD} of 1 V.

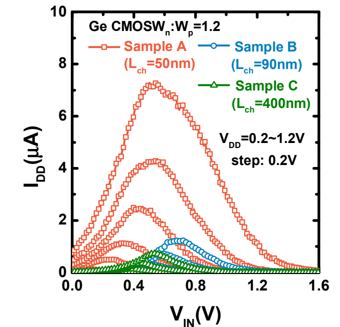

Fig. 21 Transient current versus V_{IN} curves of the same three CMOS inverters in *sample A, B and C* shown in Fig. 10-11 with a V_{DD} from 1.2 V to 0.2 V.

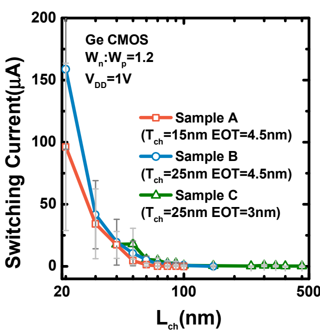

Fig. 22 Channel length dependence of switching current (maximum transient current) of CMOS inverters in *sample A, B and C* with a V_{DD} of 1 V.

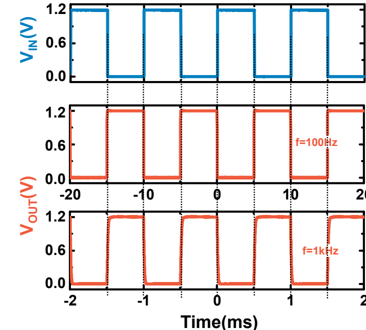

Fig. 23 Response signals of a 100 nm L_{ch} CMOS inverter in *sample B* to square-wave input signals with different time periods.

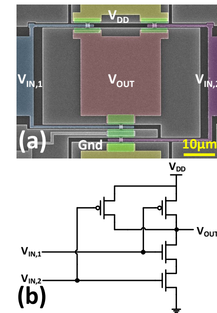

Fig. 24 (a) Top-down SEM image of a NAND logic gate. (b) Circuit diagram of the NAND logic gate.

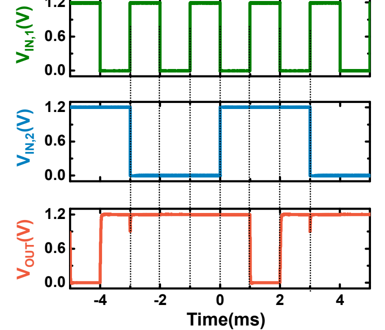

Fig. 25 Response signals of a 100 nm L_{ch} NAND logic gate in *sample B* to two square-wave input signals in the time domain.

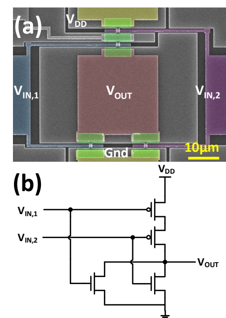

Fig. 26 (a) Top-down SEM image of a NOR logic gate. (b) Circuit diagram of the NOR logic gate.

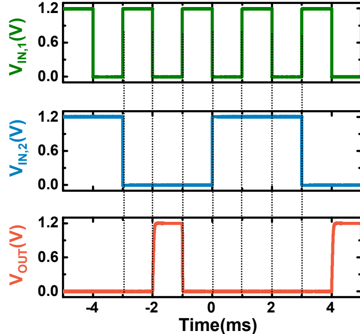

Fig. 27 Response signals of a 100 nm L_{ch} NOR logic gate in *sample B* to two square-wave input signals in the time domain.

Publication	Channel Material	Gate Dielectric	Fabrication Method	L_{ch}	Voltage Gain
NL 2012 UC Berkley[8]	InAs n-Channel InGaSb p-Channel	10 nm ZrO_2	PDMS transferred Nano-ribbon on SiO_2	2.85 μm (nFET) 2.6 um (pFET)	14V/V (V_{DD}=1V)
NL 2012 Lund[9]	InAs n-channel GaSb p-channel	4 nm Al_2O_3	Bottom-up nanowire on SiO_2	2.7 μm	10 V/V (V_{DD}=1V)
PNAS 2009 Harvard[10]	InAs n-channel SiGe p-channel	20 nm HfO_2	Bottom-up nanowire on SiO_2	1.5 μm	45V/V (V_{DD}=4V)
EDL 2006 Stanford[11]	Si n-channel Ge p-channel	SiO_2 (EOT=10nm, nFET) GeN_x(EOT=20nm, pFET)	Top-down on Si substrate with RMG GeOI layer	1 μm (nFET) 1.5 μm (pFET)	4V/V (V_{DD}=5V)
EDL 2011 Samsung[12]	α-IGZO n-channel Poly Si p-channel	SiO_2 /SiN_x	Top-down on Si substrate with multiple channel layer	40 μm (nFET) 10 μm (pFET)	18V/V (V_{DD}=7V)
VLSI 2014 Purdue[13]	GaAs (111)A n-channel GaAs (111)A p-channel	4 nm La_2O_3 / 4 nm Al_2O_3	Top-down on common GaAs(111)A substrate	1 μm	12V/V (V_{DD}=3V)
VLSI 2014 AIST[14]	InGaAs n-channel SiGe p-channel	4.5 nm HfO_2 (nFET) 7.8 nm Al_2O_3 (pFET)	Top-down on SGOI substrate with InGaAs layer by wafer-bonding	10 μm	26V/V (V_{DD}=1V)
IEDM 2013 IBM[15]	InGaAs n-channel SiGe p-channel	10 nm Al_2O_3	Top-down on SiGeOI substrate with InGaAs layer by wafer-bonding	500 nm	14V/V (V_{DD}=1V)
VLSI 2014 Renesas[16]	α-IGZO n-channel α-SnO p-channel	30 nm SiN / 20 nm SiO_2	Top-down on Wafer with IGZO and SnO	0.8 μm	12V/V (V_{DD}=5V)
THIS WORK	Ge n-channel Ge p-channel	8 nm Al_2O_3 (Sample A) 5 nm Al_2O_3 (Sample C)	Top-down on common GeOI substrate	50 nm -C 400 nm -A	5 V/V (V_{DD}=1.2V)-A 36 V/V (V_{DD}=1.2V)-C

Table 1. Comparison of the Ge CMOS logic gates in this work with other non-silicon CMOS inverter results in literature.