Low-Frequency Noise and RTN on Near-Ballistic III-V GAA Nanowire MOSFETs

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Abstract

In this work, we report the first observation of RTN in highly scaled InGaAs GAA MOSFETs fabricated by a top-down approach. RTN and low frequency noise were systematically studied for devices with various gate dielectrics, channel lengths and nanowire diameters. *Mobility fluctuation* is confirmed to be the source of low-frequency noise, showing 1/f characteristics. Low-frequency noise was found to decrease as the channel length scaled down from 80 nm to 20 nm, indicating the near-ballistic transport in highly scaled InGaAs GAA MOSFET.

Introduction

InGaAs has been considered as one of the promising channel materials for CMOS logic circuit beyond 10 nm node because of its large electron injection velocity [1]. InGaAs gate-all-around (GAA) MOSFETs have been demonstrated to offer large drive current and excellent immunity to short channel effects down to deep sub-100 nm channel length [2]. On the other hand, classical theories suggest that low-frequency noise increases inversely with decreasing channel length. If it is true, this may negate some of the performance gain of short channel transistors [3-5]. Meanwhile, traditional oxide characterization methods, such as C-V and charge pumping, cannot be used for ultra-small devices without a body contact. Therefore, noise and RTN characterizations can be used as alternative probes to quantitatively analyze performance, variability and reliability of highly scaled devices [6-10]. Several groups have recently reported RTN of bottom-up synthesized *long-channel* InAs nanowire MOSFETs [11-13]. However, there is no report on RTN and low-frequency noise studies of highly scaled III-V GAA MOSFETs by top-down approach. In this work, we (i) report the first observation of RTN on top-down fabricated InGaAs GAA MOSFETs, (ii) examine the origin of low-frequency noise on highly scaled InGaAs GAA MOSFETs, (iii) systematically study the low-frequency noise and RTN characteristics of near-ballistic InGaAs GAA nanowire MOSFETs.

Experiments

Fig. 1(a) shows the schematic diagram and cross-sectional view of an InGaAs GAA MOSFET. The top-down fabrication process is shown in Fig. 1(b), which is the same as reported in Ref. [2]. The samples used for noise characterizations and device dimensions are summarized in Table 1. Samples A and B have a 0.5 nm Al_2O_3/4 nm $LaAlO_3$ stack (EOT = 1.2 nm), where Al_2O_3 was grown before $LaAlO_3$ for sample A and reverse order for sample B. Sample C has 3.5 nm Al_2O_3 as gate dielectric (EOT = 1.7 nm). The RTN and low-frequency characterization setup is shown in Fig. 2. The gate voltage (V_{gs}) is supplied by a digital controllable voltage source. A Stanford SR570 battery-powered current amplifier is used as source voltage supply and monitor for the source current (I_s). I_s is used due to the relatively large junction leakage current in drain current (I_d). I_s shows more clearly the fundamental transport properties inside the nanowire. The amplifier output is directly connected to a Tektronix TDS5032B oscilloscope to record RTN signal and an Agilent 35670A dynamic signal analyzer to obtain the power spectrum density (PSD) of the noise of I_s. All noise measurements were performed at V_{ds} =50mV and at room temperature unless otherwise specified.

Results and Discussion

Figs. 3-4 show the well-behaved output and transfer characteristics of a GAA MOSFET with $L_{ch}=W_{NW}=20$ nm. PBTI measurement at V_{gs}=0.6, 0.8V on Sample A and B is shown in Fig. 5. PBTI measurement on Sample C can be found in [14]. V_T shifts less than 10 mV during noise measurements is ensured under maximum V_{gs}=0.4 V conditions. Fig. 6(a) and (b) show the RTN signals of an InGaAs GAA MOSFET, with L_{ch}=20 nm, W_{NW}=80 nm and 3.5 nm Al_2O_3 as gate dielectric, in time domain at V_{gs}=-0.025 V and V_{gs}=-0.075 V at 15°C. The histogram and lag plot at V_{gs}=-0.025 V of the same device are shown in Fig. 7(a) and (b). Two distinct current switching levels are observed, which clearly indicates the existence of a single active trap. Fig. 8 shows 'PSD of I_s' normalized by I_s^2 (i.e., S_{Is}/I_s^2) of the RTN signal shown in Fig. 6(a). A typical Lorentzian spectrum is shown in the noise spectrum with $1/f^2$ characteristics. Clear RTN signals are observed on about 1/3 of devices measured on Sample A, B and C, but only when V_{gs} is near threshold voltage (V_T). Fig. 9 shows the comparison of noise spectrum between a device with RTN signal and a device without RTN. The two devices share the same device dimension with L_{ch}=20 nm, W_{NW}=25 nm and 3.5 nm Al_2O_3 as gate dielectric. It is clear that the noise spectrum of the device without RTN shows 1/f characteristics, while the noise spectrum of the device with RTN is the superposition of 1/f noise spectrum and a Lorentzian spectrum. Fig. 10 shows (a) I_s histogram and (b), (c) RTN signals in time domain on a L_{ch}=20 nm, W_{NW}=25 nm device of Sample B, showing the superposition of RTN signal and mobility fluctuation (1/f) noise. This phenomenon suggests the fact that mobility fluctuation (rather than carrier number fluctuation) is the origin of low-frequency noise on devices without RTN signal. Fig. 11 shows S_{Is}/I_s^2 as a function of I_s on Sample A, B and C with L_{ch}=20nm and W_{NW}=20nm at f=10Hz which are weakly dependent on the different interfaces. All the three selected devices show 1/f spectrum

without RTN. That S_{Is}/I_s^2 can be modulated by I_s indicates that the noise source is from channel rather than series resistance. In addition, S_{Is}/I_s^2 depends only weakly on the gate oxide, suggesting that oxide trapping and de-trapping induced carrier number fluctuation is not the source of low-frequency noise in this work. Fig. 12 shows the scaling metrics of S_{Is}/I_s^2 versus L_{ch} at f=10 Hz and W_{NW}=20 nm for Sample B. Normalized I_s noise is reduced as L_{ch} scaling down, which is opposite to the conventional noise L_{ch} scaling characteristic ($S_{Is}/I_s^2 \sim 1/L_{ch}$). This phenomenon leads to the main conclusion of this work: that near-ballistic transport of electrons in the channel is achieved, as determined through noise studies. As electrons from the source cannot equilibrate to lattice temperature immediately at drain contact, the conventional mobility fluctuation model, which assumes diffusive transport, can no longer be applied. In our near-ballistic InGaAs GAA MOSFETs, electrons encounter less scattering at smaller L_{ch} during transport from source to drain. Therefore, scattering induced mobility fluctuation decreases at small L_{ch} so that normalized I_s noise is reduced at small L_{ch}. This further confirms that mobility fluctuation is the origin of low-frequency noise for highly scaled InGaAs MOSFETs. Fig. 13 shows the relation between S_{Is}/I_s^2 and V_{ds} at V_{gs}=0V. Smaller normalized I_s noise is obtained at high V_{ds} because ballistic efficiency is higher at high V_{ds} than low V_{ds}. Fig. 14 shows the thermo-reflectance image of an InGaAs GAA MOSFET with L_{ch}=80 nm, W_{NW}=30 nm at V_{gs}=1 V. The drain side is heated at high V_{ds} by ballistic electrons, indicating that electrons travel substantial distance into the contact before reaching equilibrium with the lattice. This supports the conclusion of Fig. 13 that InGaAs GAA MOSFETs in this work are near-ballistic. Hot Carrier Injection measurement also confirms the near-ballistic transport in the devices as we reported in [15]. Fig. 15 shows the relation between normalized I_s noise with W_{NW}. S_{Is}/I_s^2 shows weak dependence on W_{NW}. Figs. 16-21 show the property of RTN in the same condition as in Fig. 6 from V_{gs}=-0.15V to 0V. Capture/emission time constants (τ_c/τ_e) are extracted and τ_c/τ_e distributions exactly follow Poisson distribution as predicted theoretically, as shown in Fig. 16. Fig. 17 shows the relation between τ_c, τ_e and V_{gs}. Fig. 17 studies the relation between τ_c/τ_e and V_{gs}. The positive correlation between τ_c/τ_e and V_{gs} indicates that electrons trapping and de-trapping occur between channel and gate oxide, as suggested in Ref. [10]. Fig. 19 shows the relation between time constants and the reciprocal of temperature (1000/T). τ_c and τ_e are extracted at 15°C, 30°C and 45°C and the activation energy (E_a) is also extracted. Fig. 21 shows the I_s histogram at different V_{gs}. A single peak at both low V_{gs} and high V_{gs} are obtained. Between -0.15V to 0.05V, double peaks are observed indicating the existence of RTN. At low V_{gs}, it is hard to observe the RTN signal because τ_e is longer than the measurement time. At high V_{gs}, RTN is negligible comparing with noise induced by mobility fluctuation because carrier number fluctuation induced noise drops faster than mobility induced noise with I_s increases. ΔI_d and $\Delta I_d/I_d$ relation with different V_{gs} of RTN signals is shown in Fig. 20, which confirms RTN signals are hard to be observed at high V_{gs}. Two-trap RTN signals are also observed on some of the devices, as shown in Fig. 22.

Conclusion

For highly scaled InGaAs GAA MOSFETs, mobility fluctuation is the source of low-frequency noise, showing 1/f characteristics. Low-frequency noise is suppressed at shorter channel length due to the near-ballistic transport at deep sub-100nm. RTN is for the first time observed on top-down InGaAs GAA MOSFETs only around threshold voltage because RTN is negligible compared to mobility fluctuation induced noise at high V_{gs}.

Acknowledgement

The authors would like to thank X. W. Wang, X. Lou, R. G. Gordon for the valuable discussions and technical supports. The work is partly supported by AFOSR Task project.

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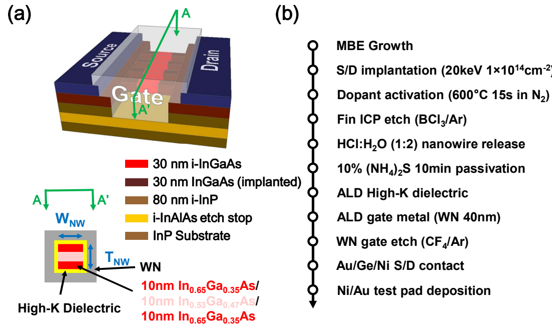

Fig. 1 (a) Schematic diagram, cross-section view and (b) fabrication process of an InGaAs GAA MOSFET.

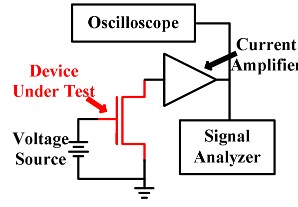

Fig. 2 Noise characterization setup diagram.

	Sample A (Al_2O_3 first)	Sample B ($LaAlO_3$ first)	Sample C (Al_2O_3 only)
Channel Material	10 nm $In_{0.65}Ga_{0.35}As$/ 10 nm $In_{0.53}Ga_{0.47}As$/ 10 nm $In_{0.65}Ga_{0.35}As$	10 nm $In_{0.65}Ga_{0.35}As$/ 10 nm $In_{0.53}Ga_{0.47}As$/ 10 nm $In_{0.65}Ga_{0.35}As$	10 nm $In_{0.65}Ga_{0.35}As$/ 10 nm $In_{0.53}Ga_{0.47}As$/ 10 nm $In_{0.65}Ga_{0.35}As$
L_{ch} (nm)	20	20,30,50,80	20
W_{NW} (nm)	20	20,25,30,35	20
T_{NW} (nm)	30	30	30
Gate oxide	0.5nm Al_2O_3/ 4nm $LaAlO_3$	4nm $LaAlO_3$/ 0.5nm Al_2O_3	3.5nm Al_2O_3
EOT (nm)	1.2	1.2	1.7

Table 1 Description of samples and device dimensions used in this work.

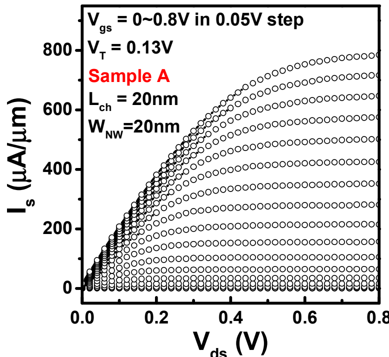

Fig. 3 Output characteristics of a 20nm L_{ch} GAA MOSFET with $Al_2/O_3/LaAlO_3$ gate dielectric (Sample A, EOT=1.2nm) and W_{NW}=20nm. I_s is used due to relatively large junction leakage current in I_d.

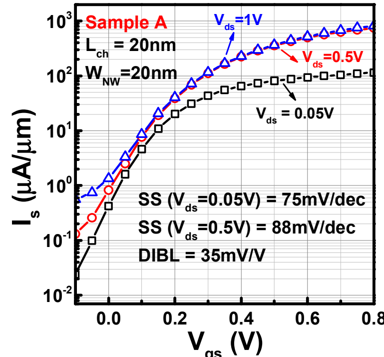

Fig. 4 Transfer characteristics of the same device shown in Fig. 3.

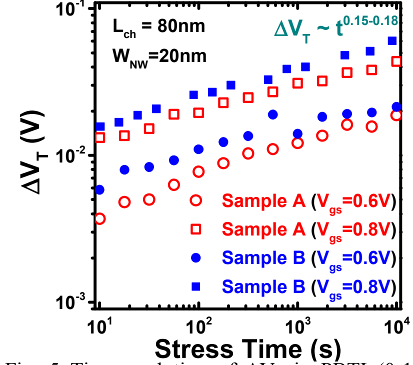

Fig. 5 Time evolution of ΔV_T in PBTI (0-10^4s) under stress of 0.6V and 0.8V for Sample A and Sample B devices with L_{ch}=80nm and W_{NW}=20nm.

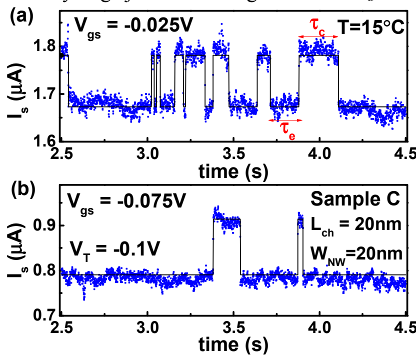

Fig. 6 I_s fluctuation due to RTN in (a) V_{gs}=-0.025 V, (b) V_{gs}=-0.075 V on InGaAs GAA MOSFETs measured at 15°C.

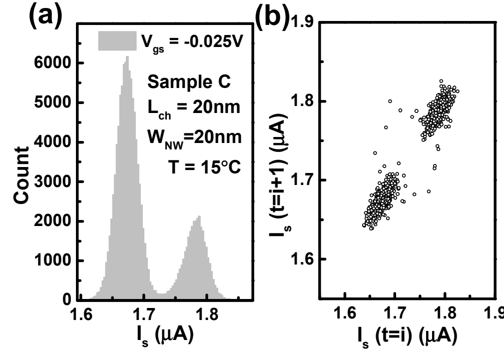

Fig. 7 (a) Histogram and (b) lag plot of a typical RTN signal shown in Fig. 6(a). The histogram and lag plot show two RTN levels.

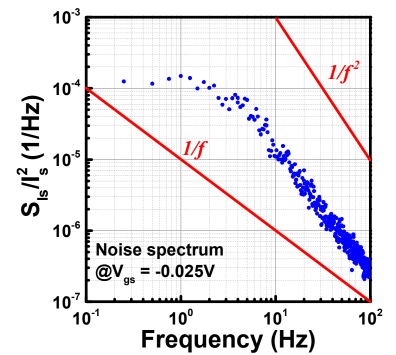

Fig. 8 Normalized I_s noise of RTN signal shown in Fig. 6(a), showing $1/f^2$ characteristics.

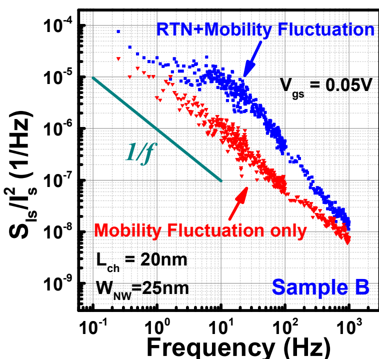

Fig. 9 Normalized I_s noise of Sample B devices with RTN signal and without RTN signal. Noise spectrum of device without RTN is attributed to mobility fluctuation.

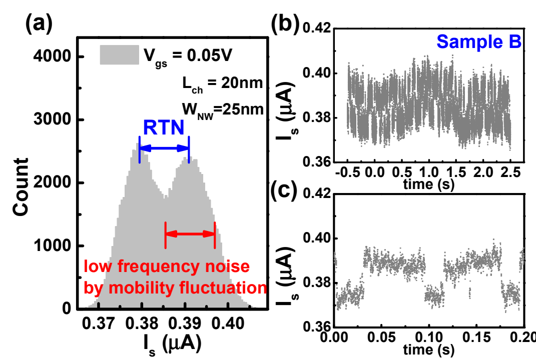

Fig. 10 (a) Histogram of a RTN signal of sample B with L_{ch}=20nm and W_{NW}=25nm. (b) and (c) RTN signals in time domain of the same signal as (a). (c) is a time segment inside (b).

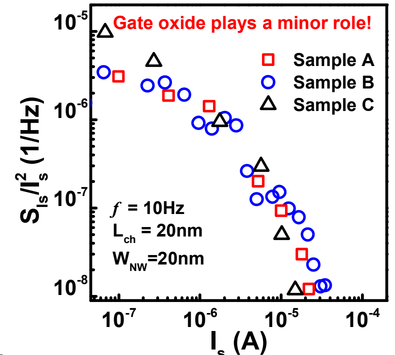

Fig. 11 Normalized I_s noise at f=10 Hz for Sample A, B and C devices with L_{ch}=20 nm and W_{NW}=20 nm. Devices with different gate oxides exhibit similar noise level showing weakly dependent on interfaces.

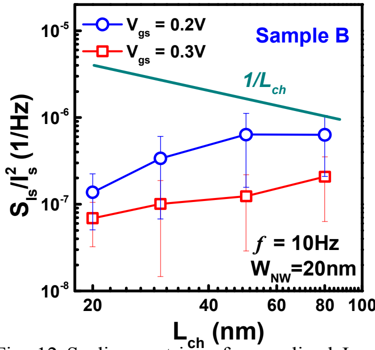

Fig. 12 Scaling metrics of normalized I_s noise at f=10 Hz and W_{NW}=20 nm for Sample B. Normalized I_s noise reduces as L_{ch} scaling down which is opposite to the conventional 1/L_{ch} scaling, indicating near-ballistic transport at small L_{ch}.

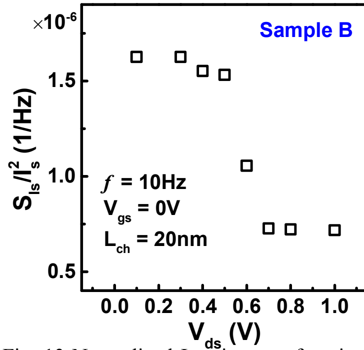

Fig. 13 Normalized I_s noise as a function of V_{ds}. Normalized I_s noise is reduced at high V_{ds} due to the increasing ballistic efficiency at high V_{ds}.

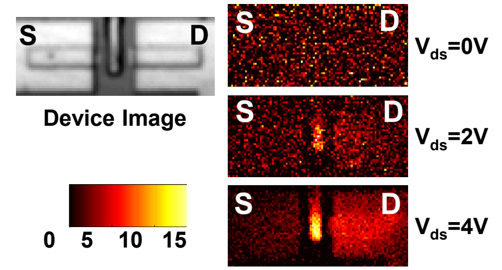

Fig. 14 Thermo-reflectance image on an InGaAs GAA MOSFET with L_{ch}=80 nm, W_{NW}=30 nm at V_{gs}=1 V. The drain side is heated far beyond the end of channel at high V_{ds}, which clearly indicates near-ballistic transport.

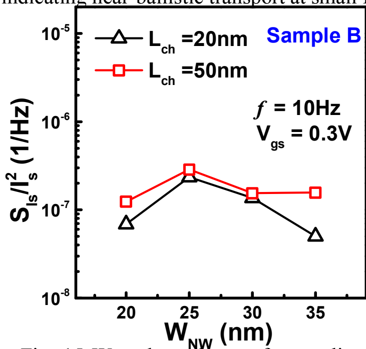

Fig. 15 W_{NW} dependence of normalized I_s noise at f=10 Hz and L_{ch}=20, 50 nm for Sample B. Normalized I_s noise shows weak W_{NW} dependence.

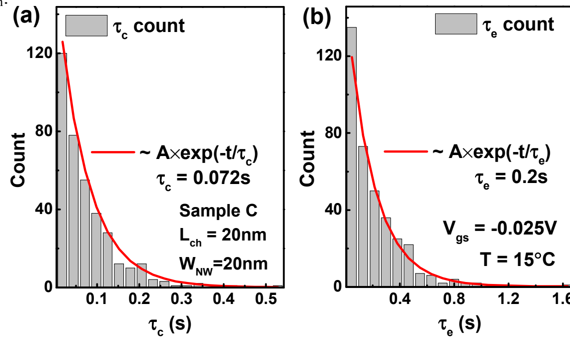

Fig. 16 Distribution of (a) capture and (b) emission time constant of RTN signal shown in Fig. 4.

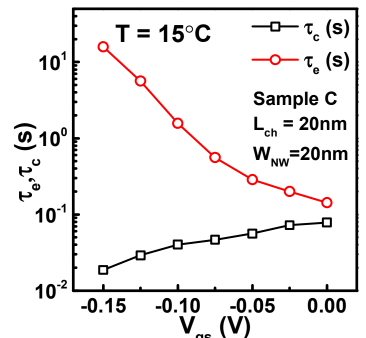

Fig. 17 Mean capture and emission time constant corresponding to different gate voltages.

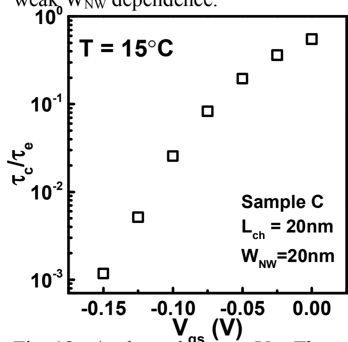

Fig. 18 τ_c/τ_e dependence on V_{gs}. The positive correlation indicates electron trapping happens between channel and gate oxide.

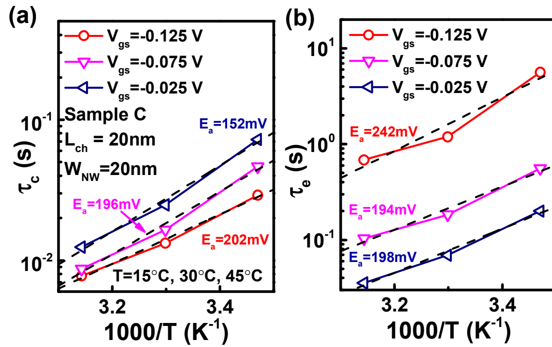

Fig. 19 Temperature dependent (a) capture and (b) emission time constant of RTN in device shown in Fig. 4.

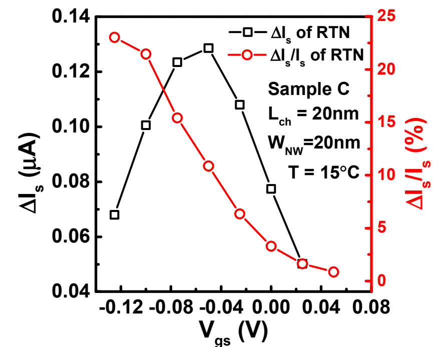

Fig. 20 ΔI_s and $\Delta I_s/I_s$ relation with different V_{gs} of RTN signals shown in Fig. 6.

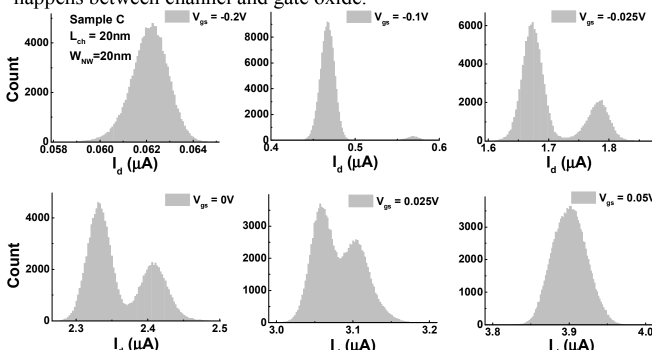

Fig. 21 Relation between I_s histogram and V_{gs} of RTN signals shown in Fig. 4. RTN signals are observed around V_T in most of devices of Samples A, B and C. This characteristic confirms that carrier number fluctuation induced I_s fluctuation is negligible under high V_{gs} and mobility fluctuation is the dominant noise source at on-state.

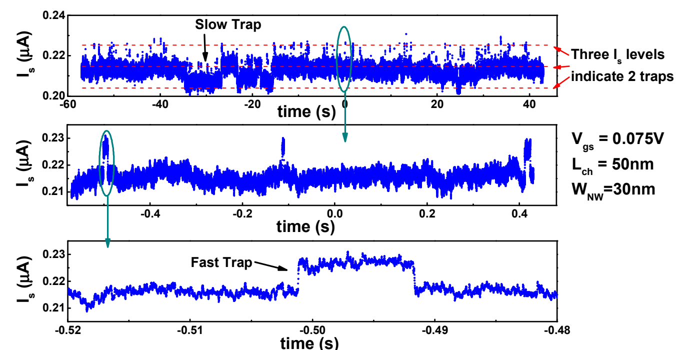

Fig. 22 RTN with 2 level trap response measured on Sample B at L_{ch}=50 nm, W_{NW}=30 nm and V_{gs}=0.075 V. (a) RTN signal in 100 s time length. A slow trap with τ_e~3 s can be observed. (b) and (c) show the RTN signals in 1s and 0.04 s time length. A fast trap with τ_c=10 ms is observed.